TELEPHONE SET

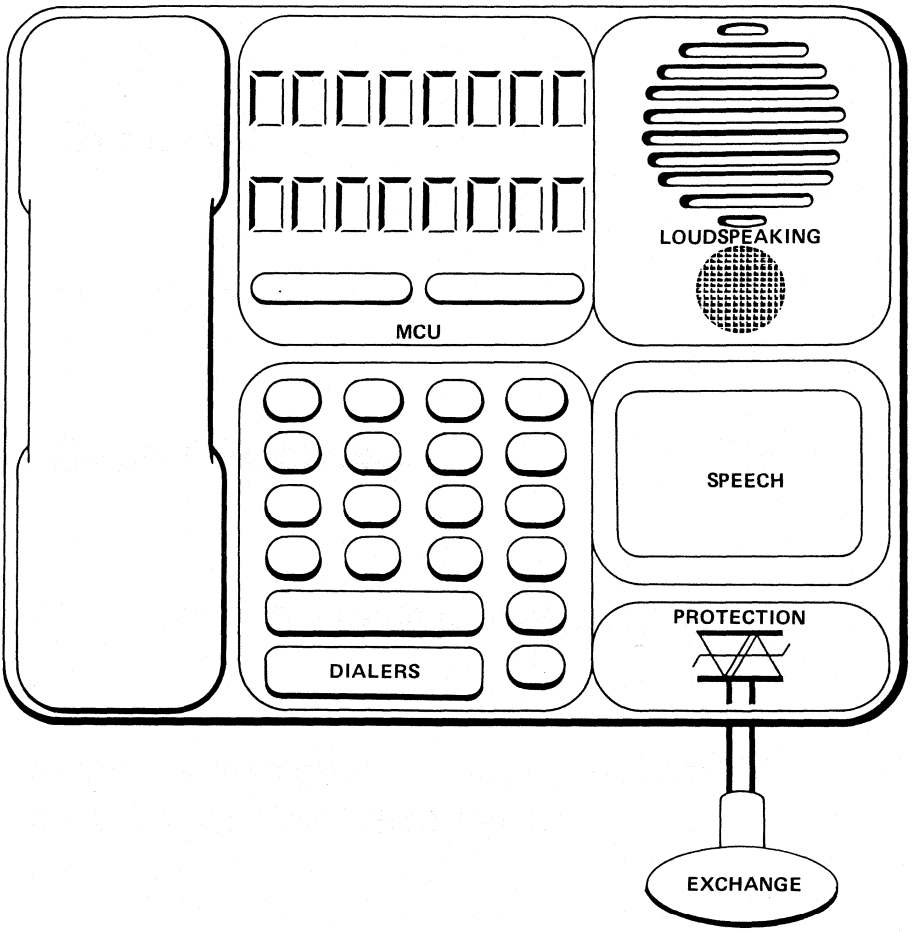
DATA BOOK

NEW NAME

SGS-THOMSON MICROELECTRONICS

THOMSON COMPONENTS SEMICONDUCTEURS

TELEPHONE SET


LOUDSPEAKING
MCU
SPEECH
PROTECTION
DIALERS
EXCHANGE

THOMSON SEMICONDUCTEURS has developped a complete strategy for Telephone Set using its best technologies in MOS, bipolar and discretes.

DIALERS (MOS)
A full range of tone and mixed dialers offering additional features as LND, flashing, memories.

SPEECH (Bipolar)
Speech circuits provide very good quality for 2 to 4 wires conversion, AC/DC current discrimination, antisidetone, DTMF on board, interface for MCU.

LOUDSPEAKING (Bipolar)
Monitor amplifiers are designed for complete monitoring: on/hook and also speech monitoring with anti-howling (anti-Larsen) system, antidistorsion. Use of loudspeaker for ringing is possible.
Handsfree circuit for high range sets.
Loudspeaking IC's are line fed.

MCU (MOS)
Wide range of 4-bit and 8-bit microcontrolers adapted to handsets applications.
8-bit MCU with DTMF on board is in development.

PROTECTION (Discretes)
Famous range of protection diodes, transils and trisils, are particularly adapted to Telephone Set.

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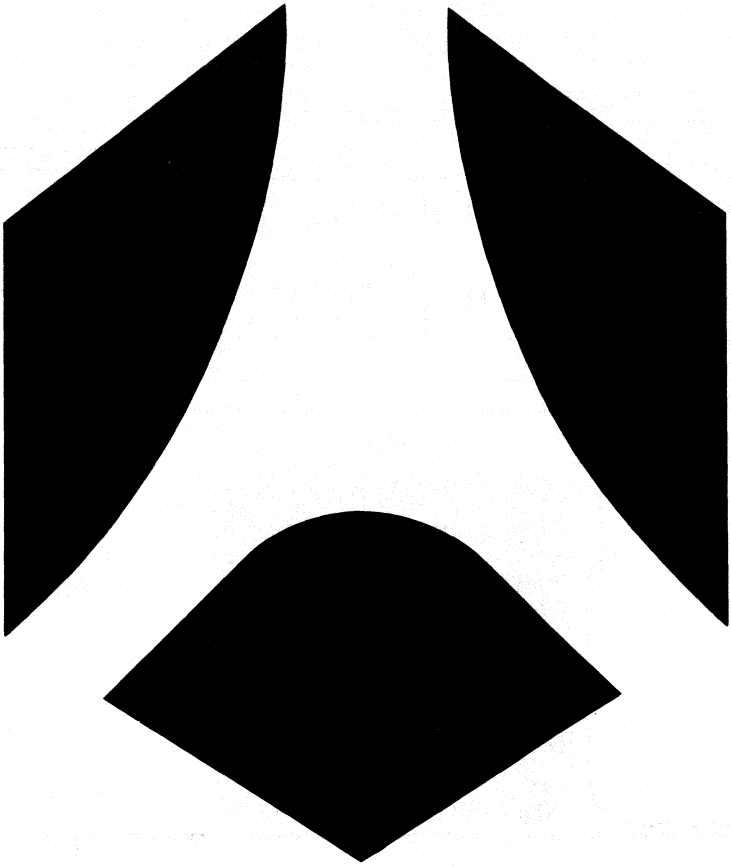
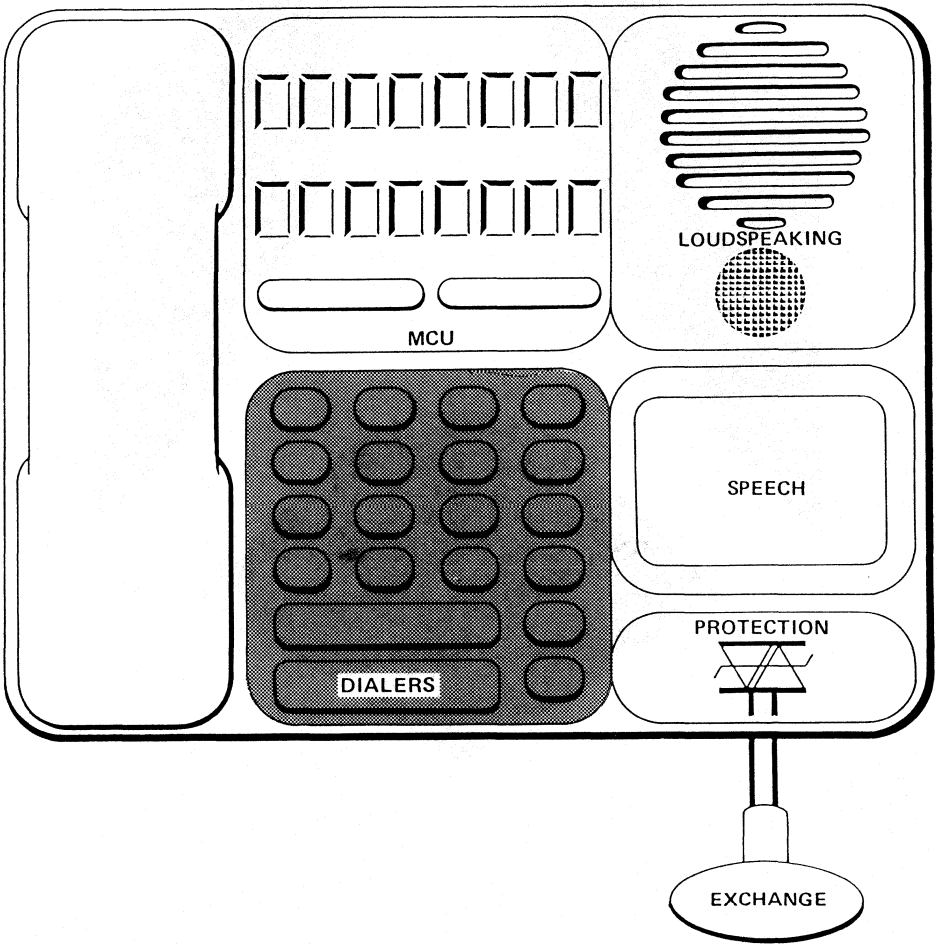


Dialers ICs


LOUDSPEAKING
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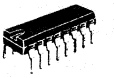
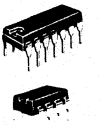
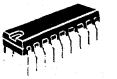
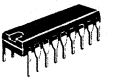
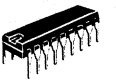
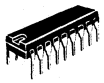
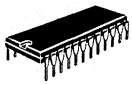
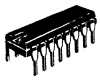
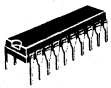
TONE DIALERS

Function	Part number	Characteristic		Package	Page
Integrated tone dialer	MK5380	Designed specifically for integrated tone-dialer applications that require : wide-supply operation with regulated output, scanned keyboard inputs, auxiliary switching functions, and a Chip Disable input.	DIL 16		1-5
DTMF generator for binary coded hexadecimal data	EFG7189	Low-cost DTMF dialer for microprocessor-controlled telephone sets operating in accordance with existing standards.	DIL 14 DIL 8		1-15

MIXED DIALERS

Function	Part number	Characteristic		Package	Page
Single number pulse tone switchable dialers	MK5370	Stand-alone DTMF and pulse signalling usable with keyboard including * and ≠ keys and special functions with single key entries . Last number re-dialed (up to 28 digit long).	DIL 18		1-27
	MK5371		DIL 18		1-39
	MK5372		DIL 24		1-39
	MK53721		DIL 20		1-55
	MK53731		DIL 18		1-63

MIXED DIALERS

Function	Part number	Characteristic		Package	Page
Ten-number repertory tone/pulse dialers	MK5375	Converts push-button inputs to both DTMF and loop-disconnect signals. Allows for the storage of ten telephone numbers, including as many as 16 digits each.	DIL 18		1-65
	MK5376	Converts push-button inputs to both DTMF and pulse signals. Ten telephone numbers of up to 16 digits each may be stored. Manual and auto-dialed numbers may be cascaded in any order.	DIL 24		1-77
	MK53761	Single chip DTMF and pulse dialer which stores ten 18-digit telephone numbers (including last number dialed). Usable with keyboard including special functions with single key entries : Last Number Dialed, Softswitch, Flash, and Pause.	DIL 18		1-87
	MK53762	Same as MK53761, usable with keyboard including special functions with single key entries : Last Number Dialed, Softswitch, Flash, Pause, and 9 memories.	DIL 20		1-89

TONE DECODERS

Function	Part number	Characteristic		Package	Page
Integrated tone decoder	MK5102	Detects and decodes the 8 standard DTMF frequencies used in telephone dialing.	DIL 16		1-93
	MK5103				1-99

THOMSON COMPONENTS MICONDUCTEURS

MK5380

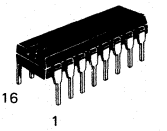
INTEGRATED TONE DIALER

FEATURES

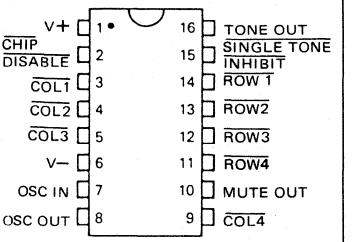
- Low standby power
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- Improved loop compensation
- Distortion lower than industry standards
- Low voltage operation - 2.5 volts
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- Auxiliary switching functions on chip
- Multiple key entry pin-selectable to either single tone or no tone

CMOS

CASE



PIN ASSIGNMENT



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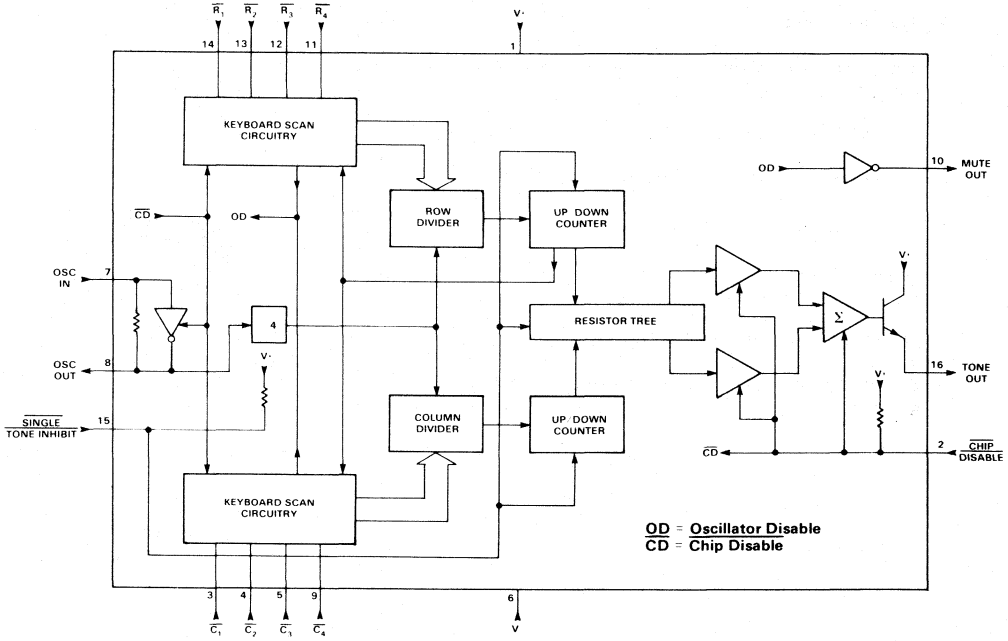
BLOCK DIAGRAM



DESCRIPTION

The MK5380 is a monolithic, integrated circuit fabricated using Mostek's Silicon Gate CMOS process. A member of the Tone III* family of integrated tone dialers, the MK5380 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

The MK5380 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, scanned keyboard inputs, auxiliary switching functions, and a $\overline{\text{Chip Disable}}$ input.

Keyboard entries to the MK5380 integrated tone dialer cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator.

D-to-A conversion for synthesis of the tones is accomplished on chip by a sinusoidally tapped resistor tree.

FUNCTIONAL DESCRIPTION

V+, Pin 1

Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 2.5 and 10.0 volts, measured relative to V- (Pin 6).

$\overline{\text{CHIP DISABLE}}$, Pin 2

When the $\overline{\text{Chip Disable}}$ input is connected to the V- supply, tone generation will be inhibited, the keyboard inputs will go to a high impedance state, and the amplifiers and oscillator will be powered down. The $\overline{\text{Chip Disable}}$ input has a pull-up resistor to the V+ supply and when floating or tied to V+, the MK5380 will operate normally.

$\overline{\text{COL}}$-$\overline{\text{ROW}}$ INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5380 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic input. Figure 1 shows how to connect to the two keyboard types and Figure 2 shows waveforms for electronic input.

The internal structure of the MK5380 $\overline{\text{Row}}$ and $\overline{\text{Column}}$ inputs is shown in Figure 3. These inputs are designed to sense a connection between $\overline{\text{Row}}$ and $\overline{\text{Column}}$, or an electronic input as shown in Figure 2. Table 1 is a functional truth table for these inputs. Note that at least one $\overline{\text{Row}}$ and one $\overline{\text{Column}}$ input must be active to generate a valid output.

When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone operation when more than one button in the same row or column is pushed. Activation of two or more diagonal buttons will result in no tones being generated.

V-, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

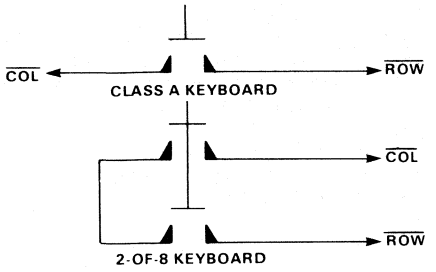
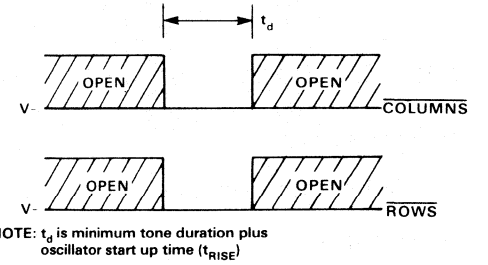


FIGURE 1 – KEYBOARD CONFIGURATION



NOTE: t_d is minimum tone duration plus oscillator start up time (t_{RISE})

FIGURE 2 – ELECTRONIC INPUT

*Trademark of Mostek Corporation

ACTIVE LOW INPUTS		
$\overline{\text{ROW}}$	$\overline{\text{COLUMN}}$	OUTPUT
One	One	Dual Tone
Two or More	One	Column Tone
One	Two or More	Row Tone
Two or More	Two or More	No Tone

NOTE: $\overline{\text{STI}}$ is floating.
$\overline{\text{CD}}$ is floating.

TABLE 1 – FUNCTIONAL TRUTH TABLE

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5380 contains an on-board inverter with sufficient loop gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 2. The oscillator is disabled whenever a keyboard input is not sensed.

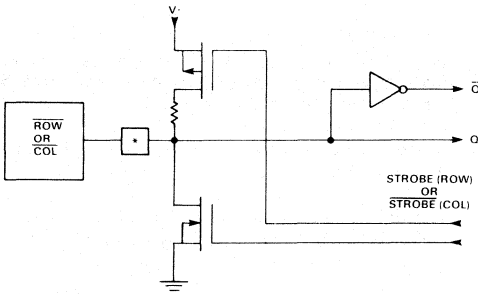
Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

	Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
$\overline{\text{ROW}}$ f_1	697	699.1	+0.31	Low Group
f_2	770	766.2	-0.49	
f_3	852	847.4	-0.54	
f_4	941	948.0	+0.74	
$\overline{\text{COL}}$ f_5	1209	1215.9	+0.57	High Group
f_6	1336	1331.7	-0.32	
f_7	1477	1471.9	-0.35	
f_8	1633	1645.0	+0.73	

TABLE 2 – OUTPUT FREQUENCY DEVIATION

MUTE OUT, Pin 10

The Mute output is a conventional CMOS inverter that pulls to V- with no keyboard input and pulls to the V+ supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The Mute Output switches regardless of the state of the $\overline{\text{Single Tone Inhibit}}$ input. Mute output is not affected by keyboard inputs when $\overline{\text{CD}}$ is tied to V-.



*STATIC PROTECTION CIRCUITRY

NOTE: $\overline{\text{Chip Disable}}$ is floating.
When $\overline{\text{CD}}$ is tied to V-, $\overline{\text{Row}}$ and $\overline{\text{Column}}$ inputs go to a high impedance state.

FIGURE 3 – $\overline{\text{ROW}}$ AND $\overline{\text{COLUMN}}$ INPUTS

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull-up to the V+ supply and, when floating, single or dual tones may be generated as described in the paragraph under $\overline{\text{Row-Column}}$ inputs.

When forced to the V- supply, any time two or more rows (or columns) are activated, no tone will result.

TONE OUT, Pin 16

The Tone output pin is connected internally in the MK5380 to the emitter of an npn transistor whose collector is tied to V+. The base of this transistor is the output of the on-chip operational amplifier which mixes the row and column tones together.

The level of a dual tone output is the sum of the levels of a single row and a single column output. This level is controlled by an on-chip reference which is not sensitive to variations in the supply voltage.

A typical single-tone sine wave output is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

A simple measurement of distortion may be made directly from the screen of a spectrum analyzer by comparing any component to one of the fundamentals.

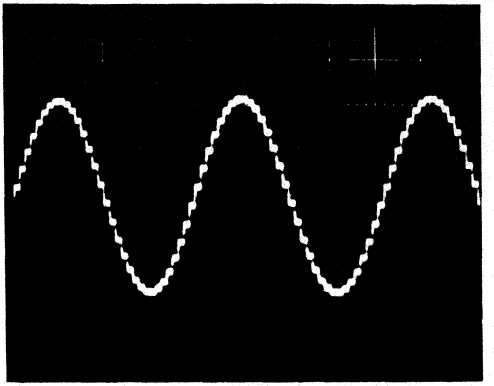


FIGURE 4 – TYPICAL SINE WAVE OUTPUT - SINGLE TONE

Figures 5 and 6 show a typical dual-tone waveform and its spectral analysis.

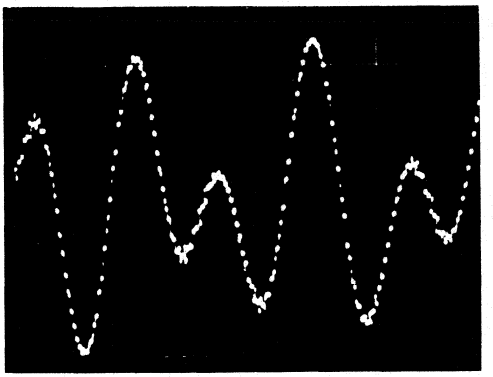


FIGURE 5 – TYPICAL DUAL-TONE WAVEFORM (Row 1', Col1)

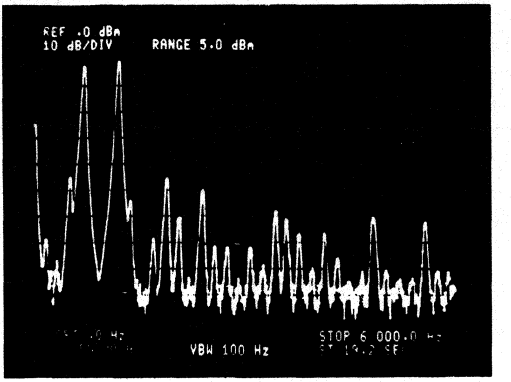
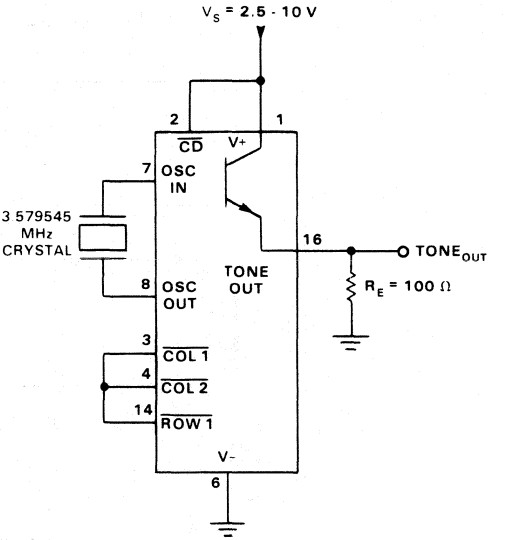


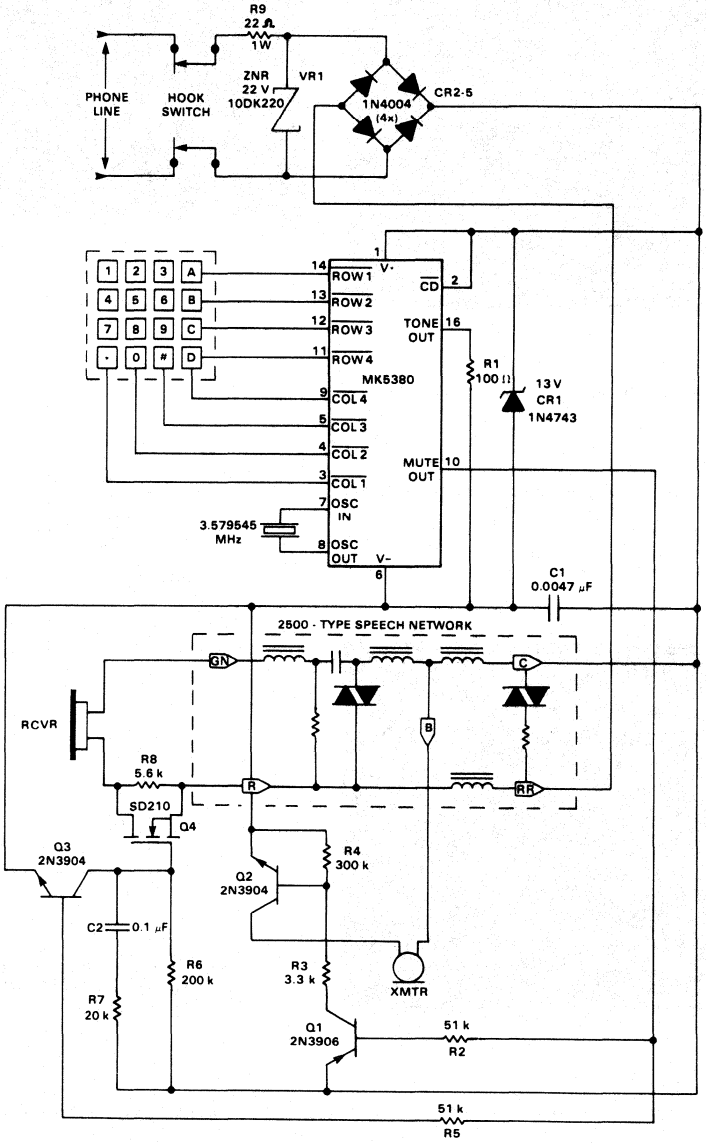
FIGURE 6 – SPECTRAL ANALYSIS OF WAVEFORM IN FIG.5
(VERT-10dB/div. HORIZONTAL - 600Hz/div.)



NOTE: The above circuit connections are for a Row 1 single tone test. For a Col 1 single-tone test, connect Row 1 (Pin 14) and Row 2 (Pin 13) to Col 1 (Pin 3).

FIGURE 7 – TONE LEVEL TEST CIRCUIT

TYPICAL APPLICATION
IN 2500-TYPE TELEPHONE



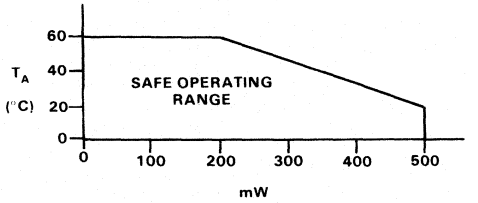
MAXIMUM RATINGS*

DC Supply Voltage V+ ..... 10.5 volts
Any Input Relative to V+ ..... +0.30 volts
Any Input Relative to V- ..... -0.30 volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +125°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CHARACTERISTICS

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/ C
WHEN SOLDERED INTO
PC BOARD.

ELECTRICAL OPERATING CHARACTERISTICS

DC CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	2.5		10.0	V	1, 2
V_{IL}	Input Voltage Low - "0"	V-		30% of V+	V	1
V_{IH}	Input Voltage High - "1"	70% of V+		V+	V	1
R_{IP}	Input Pull-Up Resistance, $\overline{STI}$, $\overline{CD}$	20		125	kΩ	
I_{SSB}	Supply Current - Standby and $\overline{CD}$ floating or tied to V+. (TA = 25°C)		0.1	2.0	μA	3,4,6
			2.0	10.0		3,4,7
I_{SO}	Supply Current - Operating ($\overline{CD}$ floating or tied to V+)		1.0	2.0	mA	3,5,6
			5.0	10		3,5,7
R_{KPU}	Keyboard Pull-Up Resistance $\overline{CD}$ tied to V+		100		kΩ	8
	$\overline{CD}$ tied to V-		10		MΩ	
R_{KPD}	Keyboard Pull-Down Resistance $\overline{CD}$ tied to V+		4.0		kΩ	8
	$\overline{CD}$ tied to V-		10		MΩ	
I_{OLM}	Output Drive, MUTE - No Entry	0.5	2.0		mA	9
		1.0	4.0			10
I_{OHM}	Output Drive, MUTE - Valid Entry	0.5	2.0		mA	11
		1.0	4.0			12

AC CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$; $2.5\ V \leq V+ \leq 10.0\ V$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{RISE}	Tone Output Rise Time			5.0	ms	13,14
$TONE_{NKD}$	Tone Output-No Key Down or $\overline{CD}$ tied to V–			-80	dBm (600 Ω)	
$TONE_{OUT}$	Tone Output Voltage (Key Down and $\overline{CD}$ floating or tied to V+)	200	245	330	mV_{rms}	15, 16, 17
			155		mV_{rms}	15,18,19
PE_{HB}	Pre-Emphasis, High Band		2.0		dB	16
DIS	Output Distortion		5.0	10.0	%	16
f_{KBS}	Keyboard Scan Frequency	699		948	Hz	8

NOTES

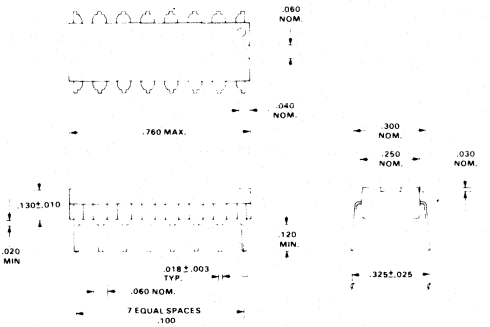
1. All voltages referenced to V– (Pin 6).
2. 2.5 V minimum instantaneous in loop applications.
3. All outputs unloaded.
4. Current out of Pin 6, no key depressed.
5. Current out of Pin 6, one key depressed.
6. V+ = 2.5 V.
7. V+ = 10.0 V.
8. When $\overline{Row}$ or $\overline{Column}$ inputs are sensed, the keyboard inputs are alternately strobed. When a $\overline{Row}$ is strobed, the $\overline{Row}$ pull-down and $\overline{Column}$ pull-up resistances are enabled. This strobing alternates in the frequency range of 699 to 948 Hz depending on which row is selected. When no inputs exist, either a $\overline{Row}$ or a $\overline{Column}$ input will be statically sensed.
9. V+ = 2.5 V, V_{OLM} = 0.5 V.
10. V+ = 10.0 V, V_{OLM} = 0.5 V.
11. V+ = 2.5 V, V_{OHM} = 2.0 V.
12. V+ = 10.0 V, V_{OHM} = 9.5 V.
13. Time from a valid keystroke with no bounce to allow wave to go from minimum to 90% of final magnitude of either frequency.
14. Crystal parameters: R_S = 100 Ω, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, C_L = 18 pF.
15. Single-tone, low-group T_A = 25°C.
16. 2.5 V ≤ V+ ≤ 10.0 V, R_E = 100 Ω (See Figure 7).
17. $TONE_{OUT}$ measured at Pin 16 (See Figure 7).
18. $TONE_{OUT}$ (measured at Pin 16 in loop applications) = 155 mV_{rms} (typical). R_E = 100 Ω. **(See typical application)**
19. The tone level, when used in a subscriber set, is a function of the output resistor R_E and the telephone ac resistance (R_L). The low-group single-tone output amplitude is a function of R_E and R_L by the relationship:

$$\frac{V_o}{TONE_{OUT}} = \frac{1}{0.2 + \frac{R_E}{R_L}}$$

where V_o is the tone output amplitude at the phone line, and R_L is the equivalent ac impedance in shunt with the tone generator (R_L typically varies with loop current). R_E is the resistor value from $TONE_{OUT}$ to V–. In a 2500-Type application R_L will typically vary from 200 to 500 Ω. Thus, at the phone line tone output levels will range from 200 to 400 mV_{rms}, depending on loop current.

PHYSICAL DIMENSIONS

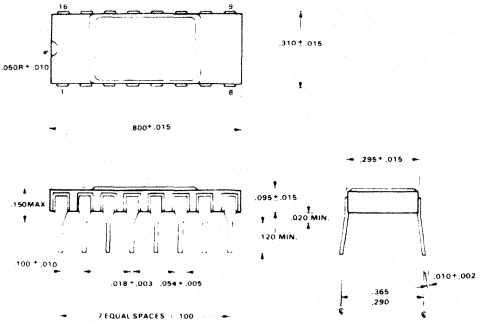
MK5380N



NOTE: Dimensions are in inches.

Plastic Dual-In-Line (N)
16-Pin

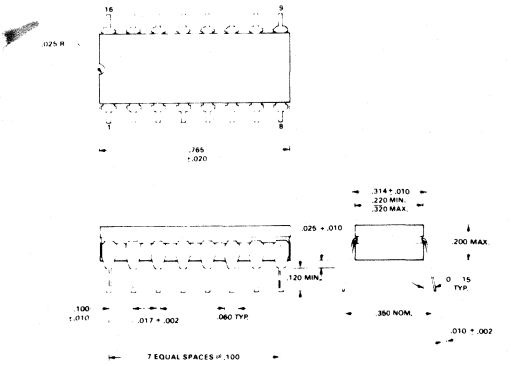
MK5380P



NOTE: Dimensions are in inches.

Side-Braze Ceramic (P)
16-Pin

MK5380J



NOTE: Dimensions are in inches.

Cerdip (J)
16-Pin

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THOMSON COMPONENTS SEMICONDUCTEURS

EFG7189

DTMF GENERATOR FOR BINARY CODED HEXADECIMAL DATA

This CMOS circuit is designed specifically to provide, with a minimum number of external components, a low cost DTMF dialer for microprocessor-controlled telephone sets operating in accordance with existing standards. The 4 bits identifying the frequency pair to be generated may be supplied via either 5 connections between the EFG7189 and the microprocessor in parallel format or in serial format through 3 connections linking the EFG7189 to the microprocessor. This feature eliminates the necessity to simulate keyboard-type inputs normally required by standard DTMF generators. Input data is stored on trailing edge of ISA signal. The tone pair selected by this code is generated while ISA remains low. With ISA high, the oscillator is inhibited and the device is in standby mode. SA pin is connected to V^- while device is outputting any tone pair.

- Generates 16 standard DTMF tone pairs
- Uses low cost 3,579 MHz crystal
- Direct microprocessor interface
- Accepts 4-bit data in serial or parallel format
- Data is stored during transmission period
- Low harmonic distortion
- High group pre-emphasis
- Low power consumption in standby mode
- Pull-up to V^+ on all logic inputs.

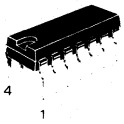
CMOS

CASES

EFG7191
CB-98

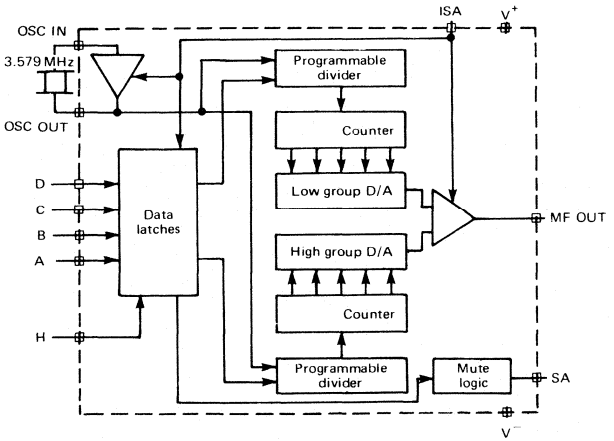
P SUFFIX
PLASTIC PACKAGE

EFG7189
TO-116
(CB-2)



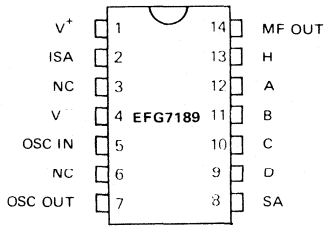
P SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM

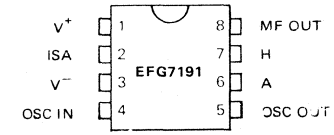


PIN ASSIGNMENTS

TO-116
(CB-2)



CB-98



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PIN DESCRIPTION

NAME	FUNCTION	N°	DESCRIPTION
V^+ V^-	Supply voltage Supply voltage	1 4	Positive supply. 0 V
B C D	Logic input Logic input Logic input	11 10 9	Parallel input for hexadecimal code allowing the selection of 2 frequencies constituting the DTMF signal (see attached table).
A	Logic input	12	Serial or parallel input for hexadecimal code.
H	Serial input clock	13	Clock input for hexadecimal code serial input register on pin A. Furthermore, it allows for the selection of the serial or parallel operating mode of this code. When ISA input goes low, the validated code is : • the parallel input code if input H is high, • the serial input code if input H is low.
ISA	Logic input	2	This pin allows for the inhibition of the analog output MFOUT : • When ISA is high, output MFOUT is idle and connected to V^-. • When ISA is low, the hexadecimal code is validated and MFOUT output is activated.
SA	Logic output	8	This pin indicates the state of the analog output : • if ISA is low, SA is a low impedance output at V^-. • if ISA is high, SA is a high impedance output.
MFOUT	Analog output	14	This pin is the DTMF signal output.
OSCIN	Oscillator input	5	This pin corresponds to the input of the inverter of the oscillator. The nominal frequency of the oscillator is 3.579 MHz.
OSCOUT	Oscillator output	7	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.

FUNCTIONAL DESCRIPTION

With ISA input at logic level "1", the device is in low power mode. The oscillator is inhibited and analog output MF OUT is at ground level. DTMF input data is detected on trailing edge of ISA. This transition enables both the oscillator and the analog output - then the data is stored and corresponding DTMF pair is generated during the low state interval of the ISA signal. Any modification to H, A, B, C and D signals during this period will not have any further effect on DTMF pair generated.
The device accepts input data in two different formats :

- Parallel format : this requires 4 connections (A,B,C,D) between the microprocessor and the circuit.
- Serial format : in this case data is supplied to the circuit by the microprocessor via 2 connections A and H (see typical application diagram).

Pre-emphasis is applied to high group tone and both tones of DTMF pair are supplied through analog output pin.

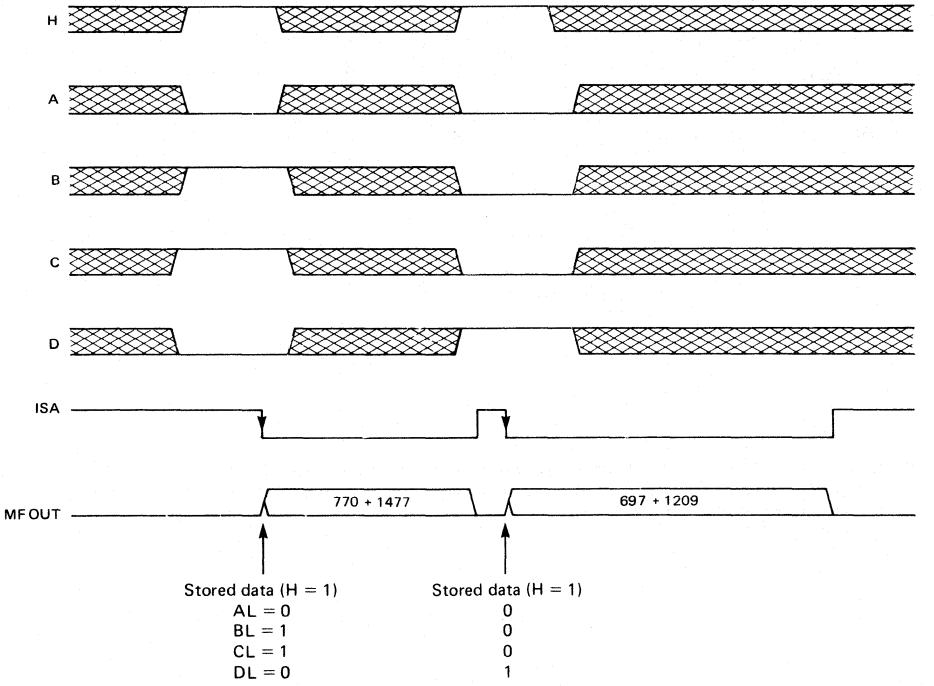
DATA ACQUISITION LOGIC

This section includes : A 4-bit shift register, an 8-line to 4-line multiplexer and a 4-bit storage register.

- The 4-bit shift register has its input connected to pin A and is enabled by the signal applied to pin H. Its outputs are AS, BS, CS and DS signals.
- The multiplexer is enabled by signal H and operates according to the following law : $AI = H.AP + \overline{H}.AS$
- The 4-bit storage register operates on trailing edge of ISA signal. AI, BI, CI, DI and AL, BL, CL, DL are its inputs and outputs respectively.

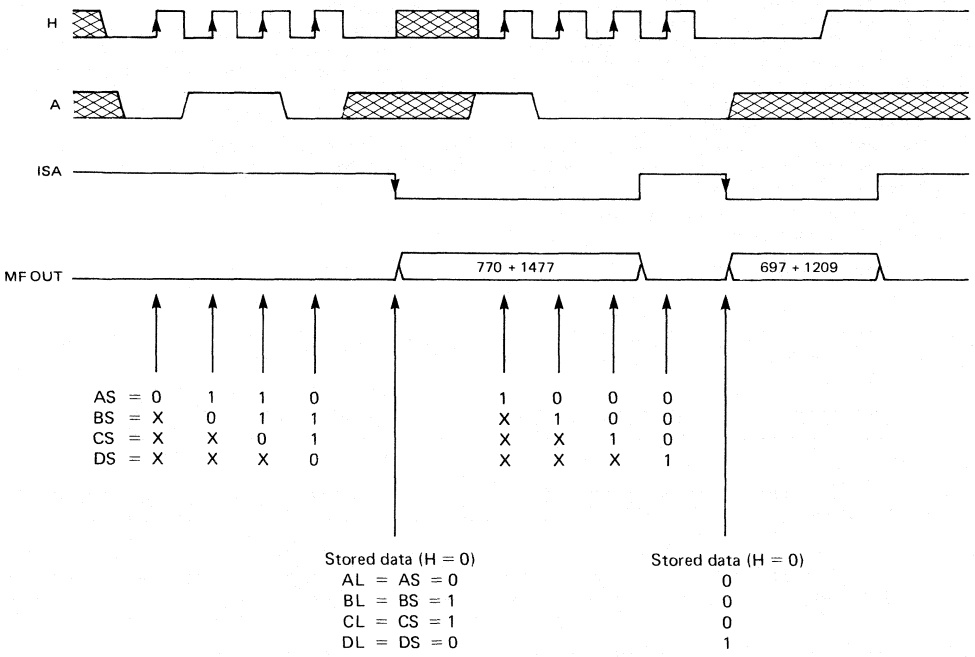
During the low state period of ISA input, AL, BL, CL and DL signals determine the DTMF pair to be generated.

Example of parallel operating mode :



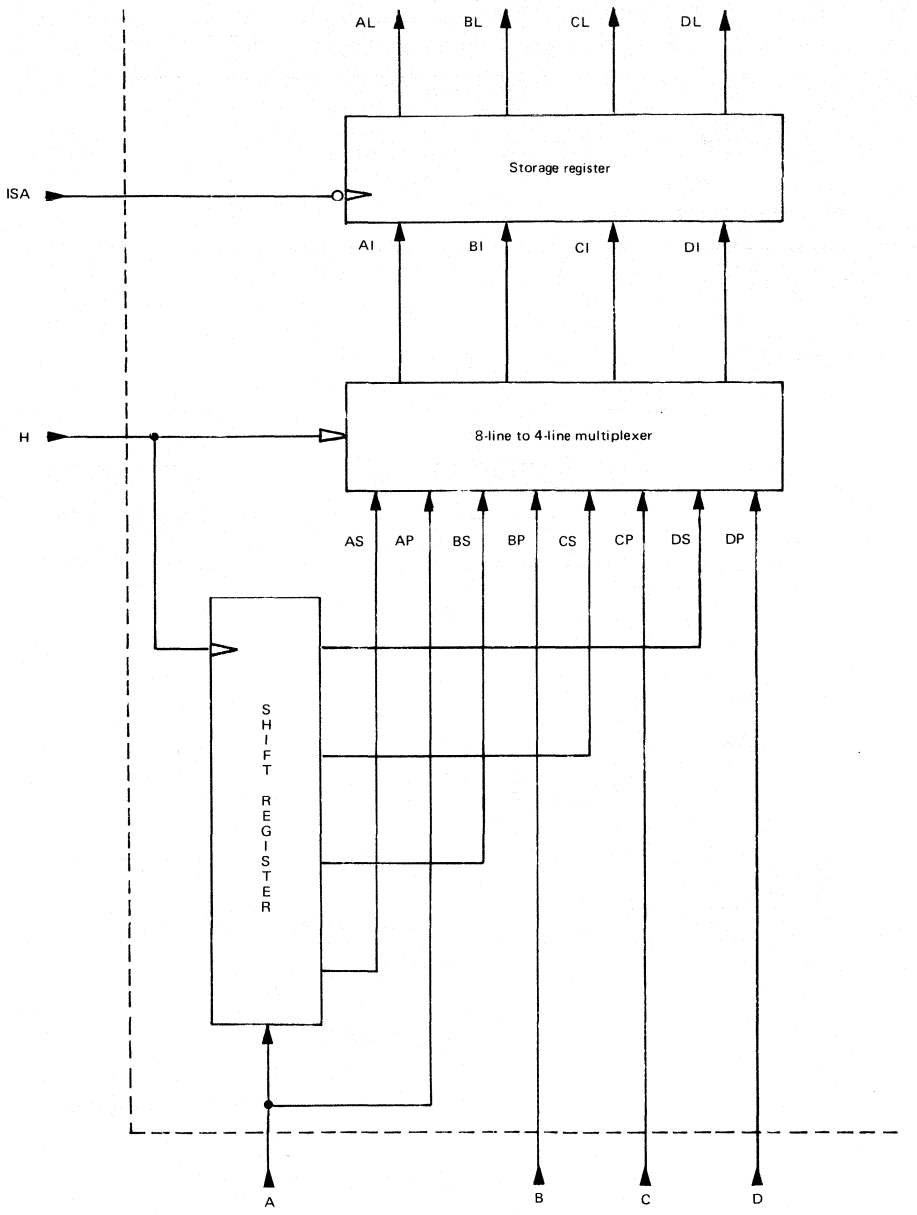
Note : If the circuit operates permanently in parallel mode, then the H input may be left floating (internally pulled-up to V^+) or tied to logic 1.
With ISA at logic 0, H,A,B,C and D inputs cannot modify the generated DTMF pair.

Example of serial-operating mode :



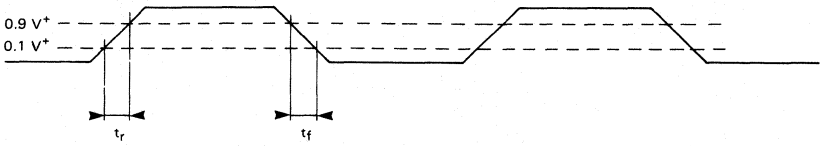
Note : • With ISA at logic 0, H,A,B,C and D signals cannot modify the generated DTMF pair. As a result, in serial operating mode, it is possible to enter AS, BS, CS and DS data while another DTMF pair is being generated.
• First data to be entered is DS.

DATA ACQUISITION LOGIC

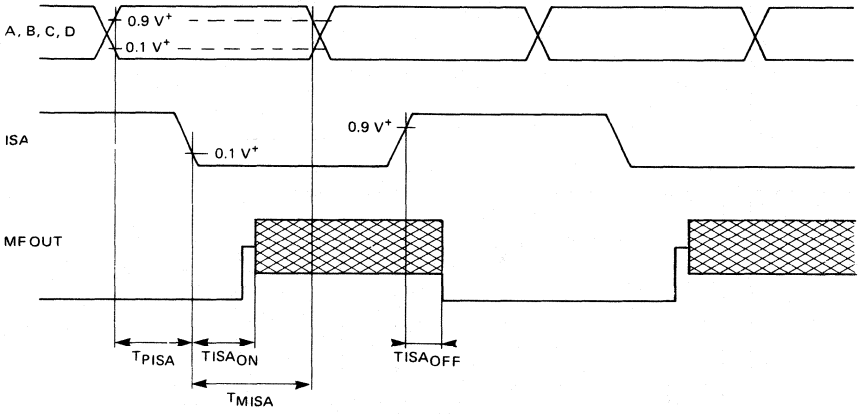


TIMING DIAGRAMS

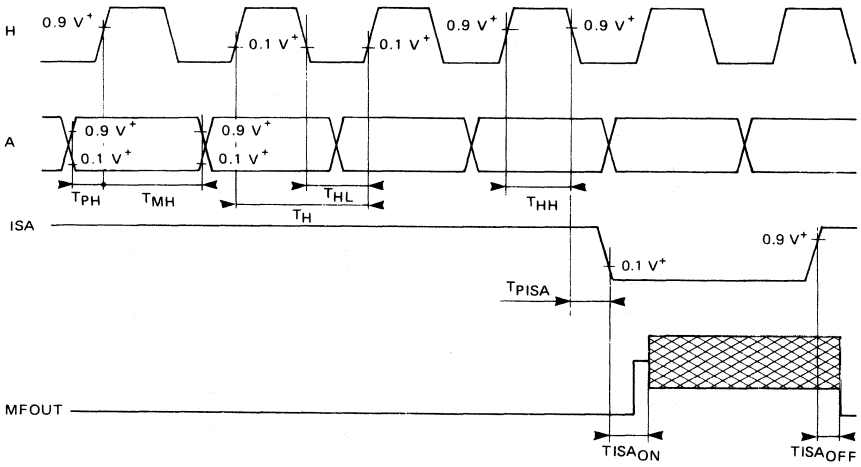
RISE/FALL TIME ON INPUT SIGNALS



PARALLEL OPERATING MODE (H = "1")



SERIAL OPERATING MODE



	DTMF specification (Hz)	Frequencies derived from a 3.579 MHz quartz (Hz)	Division rank	% deviation from standard
f1	697	701.3	5104	0.62
f2	770	771.4	4640	0.19
f3	852	857.2	4176	0.61
f4	941	935.1	3828	−0.63
f5	1209	1215.9	2944	0.57
f6	1336	1331.7	2688	−0.32
f7	1477	1471.9	2432	−0.35
f8	1633	1645	2176	0.74

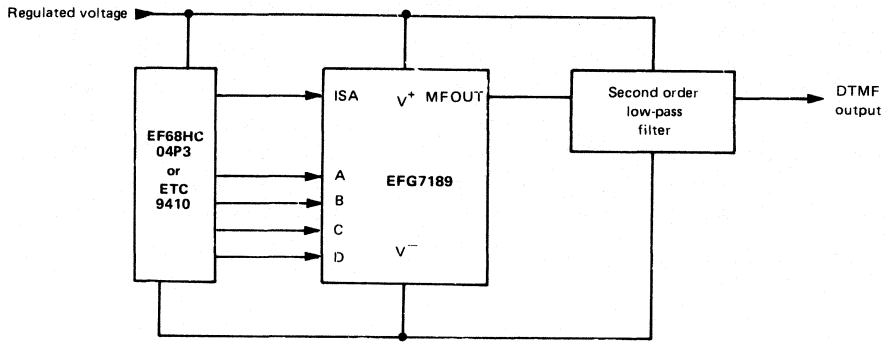
TABLE 1

Keyboard code	Hexadecimal code				ISA	Generated frequencies	
	A	B	C	D		f (Hz)	f (Hz)
X	X	X	X	X	1		
1	0	0	0	1	↓	697	1209
2	0	0	1	0	↓	697	1336
3	0	0	1	1	↓	697	1477
4	0	1	0	0	↓	770	1209
5	0	1	0	1	↓	770	1336
6	0	1	1	0	↓	770	1477
7	0	1	1	1	↓	852	1209
8	1	0	0	0	↓	852	1336
9	1	0	0	1	↓	852	1477
0	1	0	1	0	↓	941	1336
*	1	0	1	1	↓	941	1209
#	1	1	0	0	↓	941	1477
A	1	1	0	1	↓	697	1633
B	1	1	1	0	↓	770	1633
C	1	1	1	1	↓	852	1633
D	0	0	0	0	↓	941	1633

TABLE 2

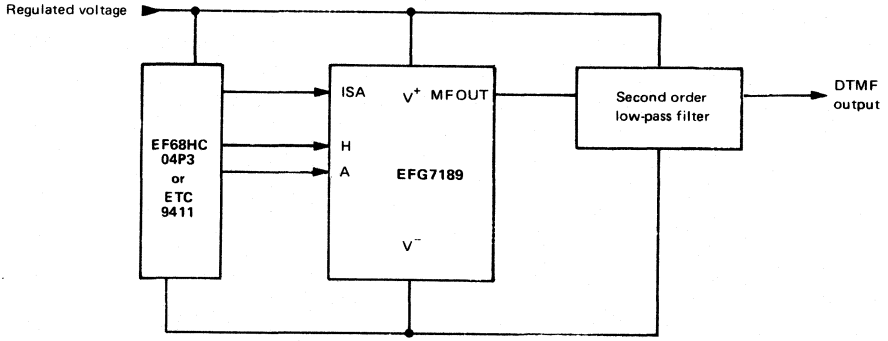
TYPICAL APPLICATION (EUROPEAN STANDARDS)

PARALLEL CONNECTION



Note : H may be left open or connected to logic 1.

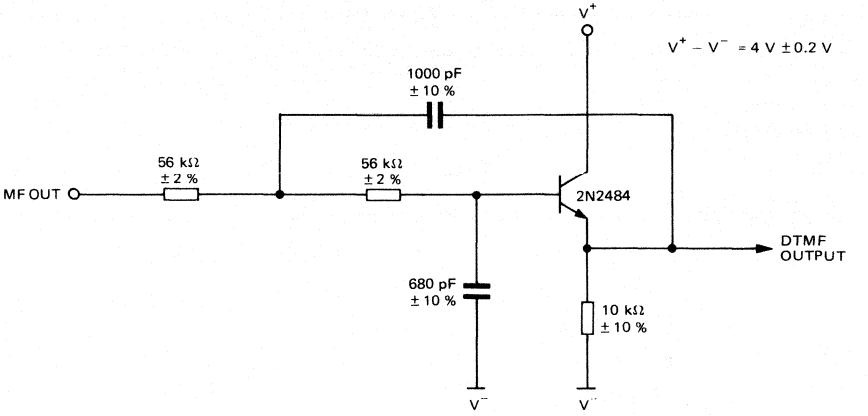
SERIAL CONNECTION



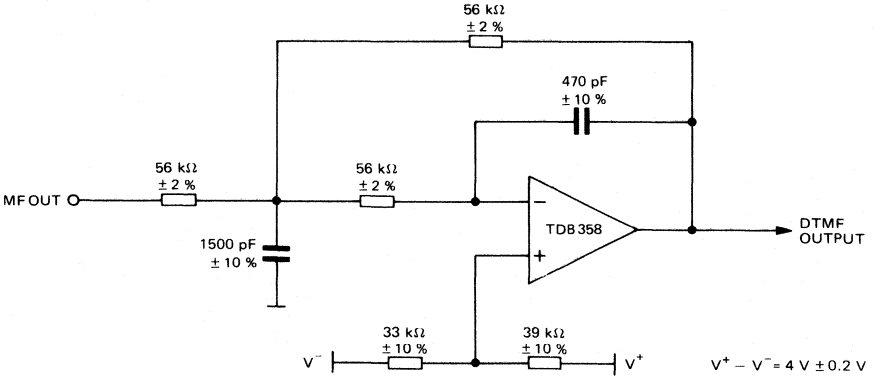
Note : B, C and D may be left floating or connected to logic 1.

SECOND ORDER LOW-PASS FILTER

Gain 1



Gain – 1



TRANSMISSION CHARACTERISTICS

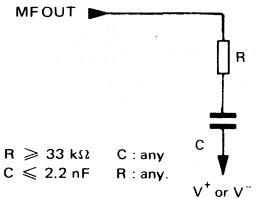
$T_{amb} = -25°C$ to $70°C$, $V^+ = 3$ V to 5.25 V, $f_c = 3.579$.

Characteristic	Symbol	Min	Typ	Max	Unit
High and low frequency precision	DFH - DFB	–	–	1	%
Low frequency transmission level ($V^+ = 4$ V) - Note 1	AFB	- 8	- 7	- 6	dBm
High band pre-emphasis	GBH	2.4	2.7	3	dB
Output distortion	D	–	–	- 20	dB

Note 1 : 0 dBm = 0.775 V_{rms}.

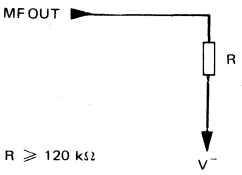
These specifications are related to the following loads.

Mixed load :

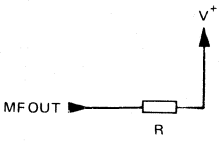


$R \geqslant 33$ kΩ C : any
$C \leqslant 2.2$ nF R : any.

Resistive load :



$R \geqslant 120$ kΩ



$R \geqslant 33$ kΩ

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V^+	− 0.3 to + 5.5	V
Digital input range	V_{in}	− 0.3 to V^+ + 0.3	V
Storage temperature range	T_{stg}	− 55 to + 125	°C

ELECTRICAL OPERATING CHARACTERISTICS

All voltages referenced to V^-.

Characteristic	Symbol	Min	Typ	Max	Unit
Positive supply voltage	V^+	3	–	5.25	V
Operating temperature range	T_{oper}	− 25	–	70	°C
Crystal frequency	f_c		3.579545		MHz

DC ELECTRICAL CHARACTERISTICS

T_{amb} = − 25°C to 70°C, V^+ = 3 to 5.25 V, f_c = 3.579 (all voltages are referenced to V^-).

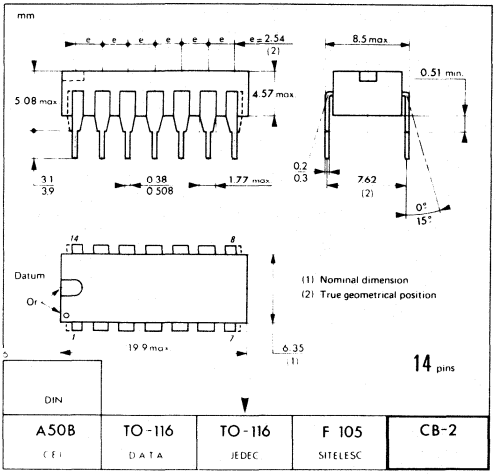
Characteristic	Symbol	Min	Typ	Max	Unit
Operating current in transmission mode (V^+ = 4 V, output not loaded)	I_{DD}	–	0.6	1	mA
Standby current (ISA,H,A,B,C,D open circuit or connected to V^+)	ISB	–	–	1	µA
Input low voltage	V_{IL}	0	–	0.3 V^+	V
Input high voltage	V_{IH}	0.7 V^+	–	V^+	V
Pull-up resistor on logic inputs ISA,H,A,B,C,D	R_T	100	–	–	kΩ
SA output current (V_{OLSA} = 0.5 V)	I_{OLSA}	500	–	–	µA
SA leakage current, open current (V_{OHSA} = 5 V)	I_{FSA}	–	–	2	µA

A.C. ELECTRICAL CHARACTERISTICS

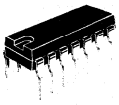
T_{amb} = − 25°C to 70°C, V^+ = 3 V to 5.25 V, f_c = 3.579

Characteristic	Symbol	Min	Typ	Max	Unit
Rise/fall time on input signals	t_r - t_f	–	–	50	ns
Transmission delay	$TISA_{ON}$	–	–	5	ms
Blocking delay	$TISA_{OFF}$	–	–	5	ms
Clock period	T_H	10	–	–	µs
High level clock width	T_{HH}	5	–	–	µs
Low level clock width	T_{HL}	5	–	–	µs
Set-up time of A related to clock	T_{PH}	1	–	–	µs
Hold time of A related to clock	T_{MH}	7	–	–	µs
Set-up time of the code or clock related to ISA	T_{PISA}	1	–	–	µs
Hold time of code related to ISA	T_{MISA}	2	–	–	µs

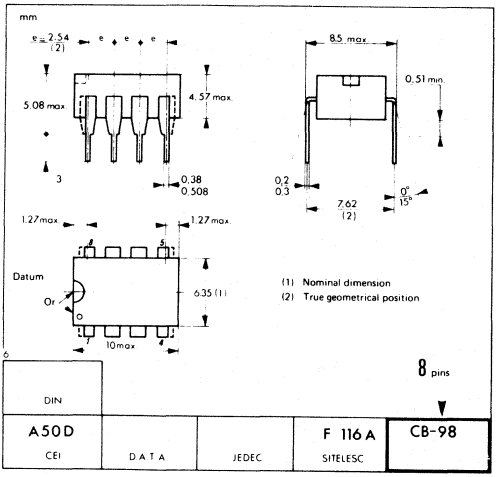
PHYSICAL DIMENSIONS



TO-116
(CB-2)



P SUFFIX
PLASTIC PACKAGE



CB-98

P SUFFIX
PLASTIC PACKAGE

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Ref. DSEFG7189

THOMSON COMPONENTS MICONDUCTEURS

MK5370

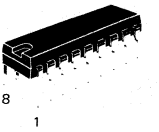
SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

FEATURES

- Stand-alone DTMF and pulse signaling
- Recall of last number dialed (up to 28 digits long)
- Form-A and 2-of-7 keyboard interface
- Pacifier tone
- Powered from telephone line, low operating voltage for long loop applications

CMOS

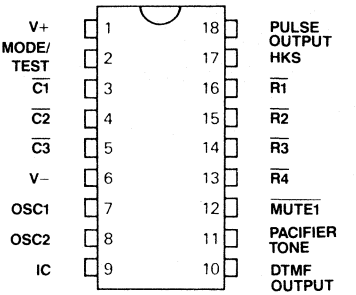
CASE



KEYPAD CONFIGURATION

1	2	3
4	5	6
7	8	9
* LND	0	# LND

PIN ASSIGNMENT



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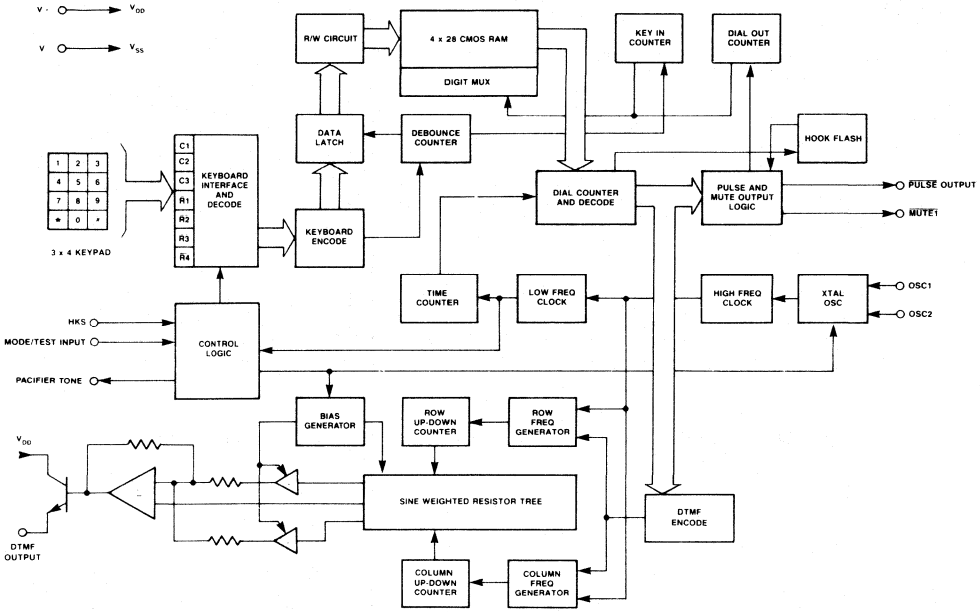
BLOC DIAGRAM



DESCRIPTION

The MK5370 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK5370 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and redial them using either the * or # as the first key entry after going off-hook.

A * or # key input automatically redials the last number dialed if it is the first key entered after a transition from on-hook to off-hook (HKS input switched from a high to low logic level). Auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed, however these inputs are not stored into memory.

FUNCTIONAL DESCRIPTION

V+
Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (See Electrical Specifications.)

MODE/TEST
Input. Pin 2. MODE/TEST determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook (V+) to off-hook (V−) the default determines the signaling mode. A V+ connection selects to tone mode operation and a V− connection selects to pulse mode operation.

Pin 2 also forces the device into test mode. Further information on this operation can be obtained from Mostek.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$
Keyboard Input. Pins 3, 4, 5, 13, 14, 15, 16. The MK5370 interfaces with either the standard 2-of-7 with negative common or the inexpensive single-contract (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V- simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator to begin scanning the keypad. Scanning consists of Rows and Columns alternately switching high through on-chip pull-ups.

After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (Tdb) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs all pull high through on-chip pull-up resistors.

IC
Input. Pin 9. Internal connection. This pin should be left floating for normal operation.

V−
Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Input/Output. Pins 7, 8. OSC1 and OSC2 are inputs to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions.

DTMF OUTPUT
Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 4 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 1. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

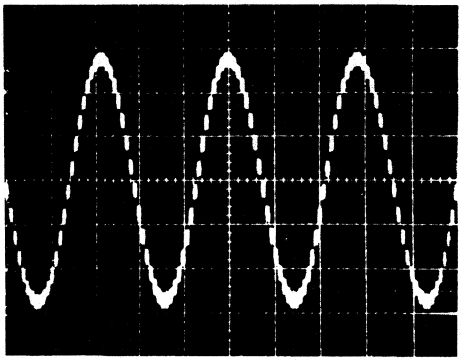


FIGURE 1 – SINGLE TONE

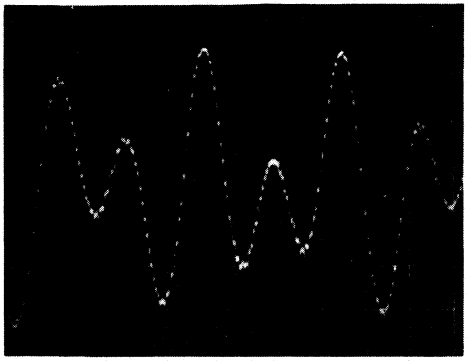


FIGURE 2 – DUAL TONE

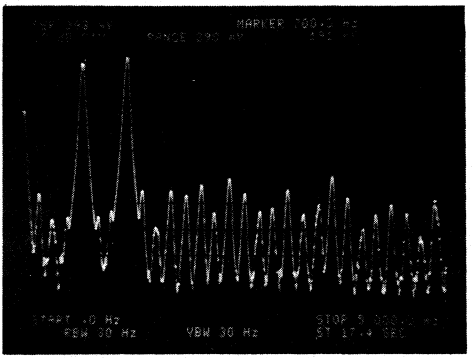


FIGURE 3 – SPECTRAL RESPONSE

The MK5370 is designed to operate from a regulated supply and the row (low group) TONE LEVEL is related to this supply by either of the following equations:

$$T_{O1} = 20 \text{ LOG } [(0.0776V+)/0.775] \text{ dBm}$$

$$T_{O1} = 0.0776(V+) \text{ VRMS}$$

The DC component of the DTMF output while active is described by the following equation:

$$V_{DC_1} = 0.66\ V+ - 0.6 \text{ Volts}$$

PACIFIER TONE OUTPUT
Output. Pin 11. A 500 Hz square wave is activated on pin 11 upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, only a redial entry activates the pacifier tone. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted.

MUTE1
Output. Pin 12. This pin is the Mute Output for both tone and pulse modes. Timing is dependent upon mode.

The output consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pull-up resistor to the positive supply.

In tone mode, $\overline{\text{MUTE1}}$ removes the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE1}}$ is active continuously until dialing is completed.

In pulse mode, $\overline{\text{MUTE1}}$ removes the receiver or the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE1}}$ timing is shown in Figure 5 for pulse mode signaling and Figure 4 for tone mode signaling.

HKS
Input. Pin 17. Pin 17 is the hookswitch input to the MK5370. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2.

KEY INPUT		STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW	1	697	699.1	+0.31
	2	770	766.2	−0.49
	3	852	847.4	−0.54
	4	941	948.0	+0.74
COL	1	1209	1215.9	+0.57
	2	1336	1331.7	−0.32
	3	1477	1471.9	−0.35

TABLE 1 – DTMF OUTPUT FREQUENCY

$\overline{\text{PULSE}}$ OUTPUT

Output. Pin 18. This pin has a dual function determined by the dialing mode selected. In Pulse Mode, the pin is an output consisting of an open drain N-channel device with zener protection. The break timing at this output meets Bell Telephone and EIA specifications for loop disconnect signaling. Figure 4 shows this timing.

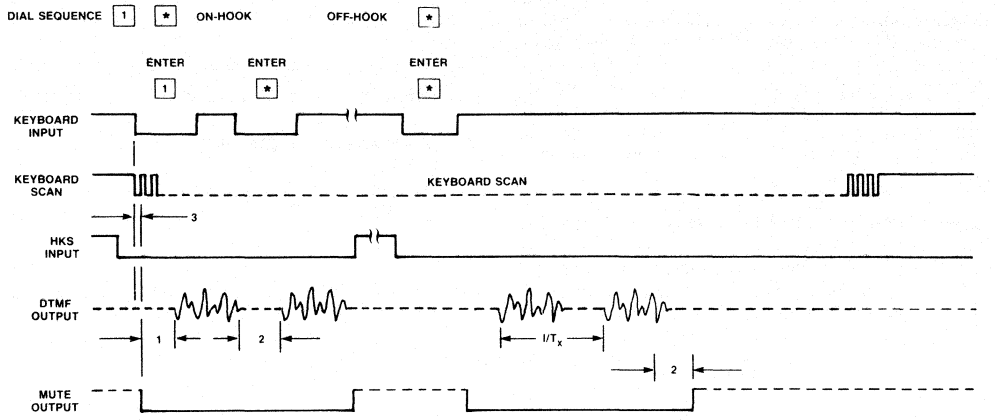


FIGURE 4 – TONE MODE TIMING

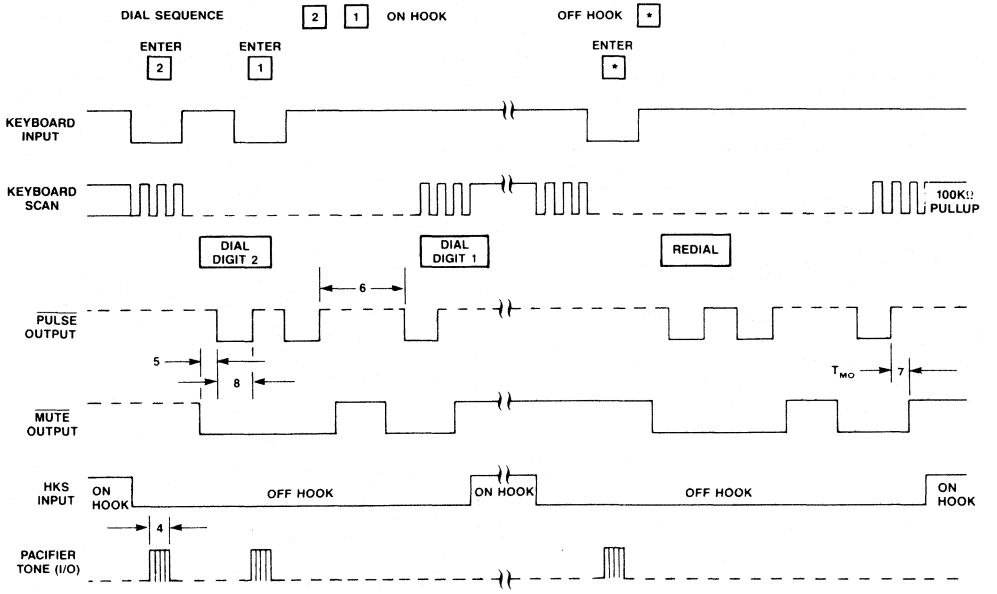


FIGURE 5 – PULSE MODE TIMING

DEVICE OPERATION (Tone Mode)

When the MK5370 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are pulled high. Key entries are not recognized unless they utilize a keypad common connection to force the respective Row and Column inputs low. These inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of 100 ms. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an intersignal time of 102 ms.

One important feature of the dialer is its ability to buffer data into the RAM before signaling. This feature allows less expensive keyboards to be used because signal distortion and double digit entry caused by bouncing and bounding of the keypad are eliminated. This design also ensures that data stored in the buffer exactly matches the digits actually dialed.

NORMAL DIALING (Off-Hook)

Digit 1 | Digit 2 | Digit 3 . . . . ETC

Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

LND

Last number dialing is accomplished by entering the * or # key as the first entry after coming off-hook..

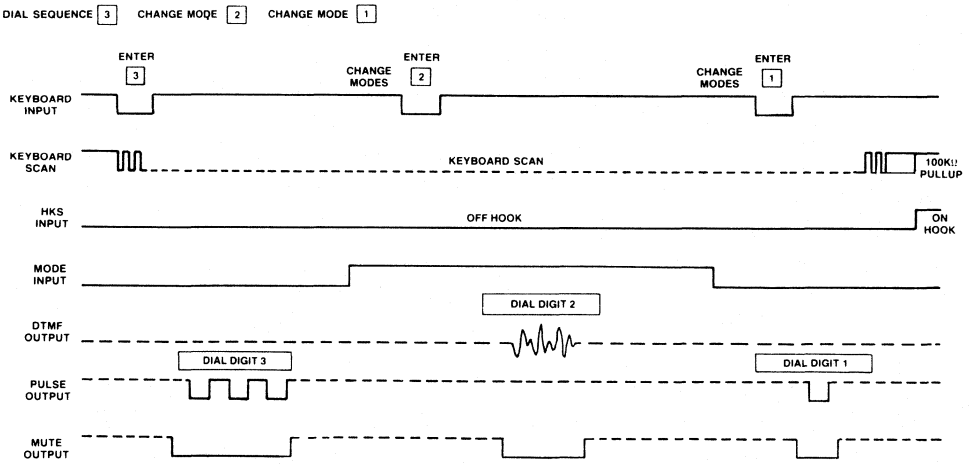


FIGURE 6 – PULSE AND TONE MODE TIMING

MAXIMUM RATINGS*

DC Supply Voltage	6.5 Volt
Operating Temperature	−30 °C to +60 °C
Storage Temperature	−55 °C to +125 °C
Maximum Power Dissipation (25 °C)	500 mW
Maximum Voltage on any Pin	(V+)+.3, (V−)−.3

ELECTRICAL OPERATING CHARACTERISTICS

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage (all functions)	2.5		6.0	Volts	
V_{MR}	Memory Retention Voltage	1.5	1.3		Volts	1, 6
I_s	Standby Current		0.2	1.0	μA	1
I_{MR}	Memory Retention Current		0.1	0.75	μA	5, 6
V_{MUTE}	Mute Output Operating Voltage	1.8			Volts	7
I_T	Operating Current (Tone)		300	600	μA	2
I_P	Operating Current (Pulse)		225	350	μA	2
I_{ML}	Mute Output Sink Current (V+ = 2.5 V)	1.0	2.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pull-up Resistance		100		kohm	
K_{RD}	Keypad Pull-down Resistance		750		ohm	
V_{IL}	Keypad Input Level-Low	0		0.3V+	Volt	
V_{IH}	Keypad Input Level-High	0.7V+		V+	Volt	

NOTES

1. All inputs unloaded. Quiescent Mode (oscillator off)
2. All outputs unloaded. single key input
3. V_{OUT} 0.4 Volts
4. Sink Current for V_{OUT} 0.5 volts. Source Current for V_{OUT} 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum supply voltage where activation of mute output with key entry is ensured.

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
3	T_{KD}	Keypad Debounce Time		32		ms	1
—	F_{KS}	Keypad Scan Frequency		250		Hz	1
—	T_{RL}	Two Key Rollover Time		4		ms	1
—	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1

NOTES
1. Crystal oscillator accuracy directly affects these times.

AC CHARACTERISTICS – PULSE MODE OPERATION

NO.	SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
—	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		40		ms	2
6	IDP	Interdigital Pause		940		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2

NOTES
1. 10 PPS is the nominal rate.
2. Figure 5 illustrates this relationship.

AC CHARACTERISTICS – TONE MODE

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
—	T_{NK}	Tone Output No Key Down			−80	dBm	1
—	T_{Od}	Tone Output (dependent)	−13 173	−12 194	−11 218	dBm mV_{rms}	1, 2 5
—	PE_d	Pre-Emphasis, High Band	2.3	2.7	3.1	dB	
—	DC_d	Tone Output DC Bias (V+ = 2.5)	1.0	1.2		Volts	
—	R_E	Tone Output Load			10	kohm	5
—	T_{RIS}	Tone Output Rise Time		0.1	1.0	ms	6
—	DIS	Output Distortion		5.0	8.0	%	3
—	T_X	Tone Signaling Rate		5.0		1/sec	
1	T_{PSD}	Pre-Signal Delay		100		ms	7
2	T_{ISD}	Inter-Signal Delay		100		ms	

NOTES

1. O dBm equals 1 mW power into 600 ohms or 775 mVolts.
   Important Note: The MK5370 is designed to drive a 10 kohm load. The 600 ohm load is only for reference.
2. Single tone (low group), varies when used in subscriber set.
3. Supply voltage 2.5 to 6 Volts, R_E 10 kohms.
4. R_E 10 Kohms
5. Supply voltage 2.5 Volts. These specifications are supply-dependent
6. Time from beginning of tone output waveform to 90% of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_S: 1000 ohms, L_m 96 mH, C_m 0.2 pF, C_o 5pF, f 3.579545 MHz, and C_1 18 pF.
7. Time from initial key input until beginning of signaling

TYPICAL APPLICATION

The MK5370 Mostek Pulse Tone dialer provides both cost-effective telephone-line interface and the logic required for DTMF (Tone) and Loop Disconnect (Pulse) signaling.

Pulse dialing originated with the rotary dial telephone. The Mostek Pulse Tone dialer provides the same capability as the rotary dial telephone and the convenience of pushbutton entry. The subscriber set (telephone) is powered by loop current supplied by the telephone company. Signaling, in Pulse Mode, is accomplished by repeatedly interrupting the loop current. The central office senses, times, and counts each line "break"; the number of breaks corresponds to the digit dialed. The duration of the break period, the dialing rate, and the separation between consecutive digits (IDP time) are controlled by the Pulse Tone dialer IC. Loop disconnect dialing is nearly a world-standard concept.

DTMF signaling consists of modulating the telephone line with a signal comprised of two fundamental frequencies. Each frequency pair represents one of sixteen possible digit (or key) entries. Twelve of these frequency pairs are commonly used (0, 1, 2, ..., *, #). The Mostek Pulse Tone dialer provides DTMF signalling capability controlling signal duration, separation, level, and rate.

The typical application circuit in Figure 7 illustrates one way the Pulse Tone dialer can be used. The pulse output provides the signal to break the line to transistor Q3. Q3 switches off, eliminating the base current to Q4, which also switches off. The majority of the loop current is then eliminated, resulting in a break condition. The IC dialer must be protected from large voltage fluctuations, such as that caused by interrupting the loop current. Transistor Q1 along with R2, C1, and Z1 regulate the voltage to the dialer. The Mute Output signal is active while signalling each digit to mute popping noises at the receiver (earpiece or speaker).

The DTMF tone output drives the base of Q8, which modulates the line. The tone level at tip and ring is determined by the effective impedance of the telephone line and the speech network.

Mode of operation is controlled by switch S1 (which sets the default dialing mode).

Resistor R1 provides a small memory-retention bias current to prevent the device from powering down while on hook. The current required for long term memory retention is less than 1μA.

A ceramic sounder can also be interfaced to pin 11 (PACIFIER TONE) of the device. A pacifier tone signal is activated for each key entry in pulse mode. This feature provides an audible indication for each valid key entry. Keys may be entered faster than the maximum signalling rate allows. Audible feedback confirms proper key entry.

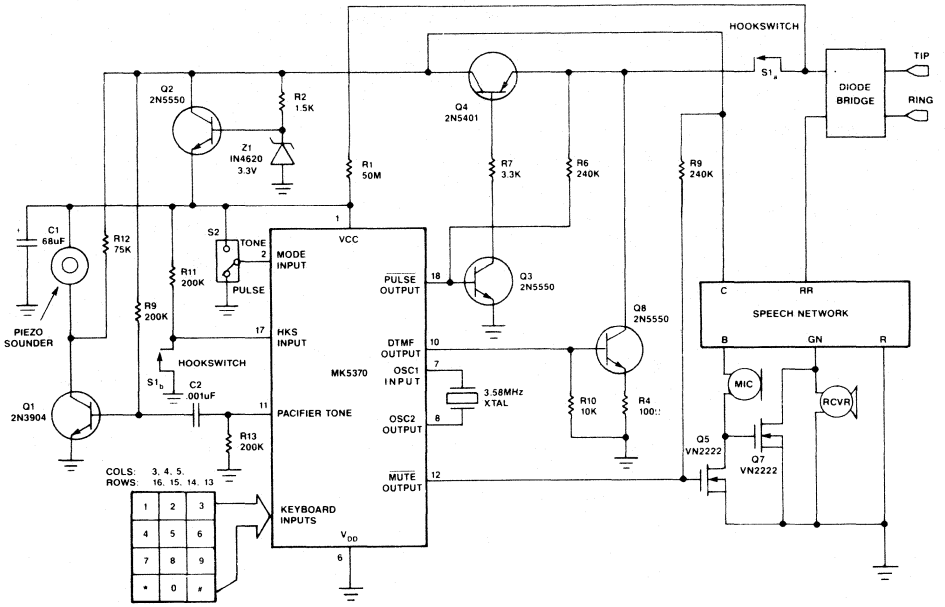
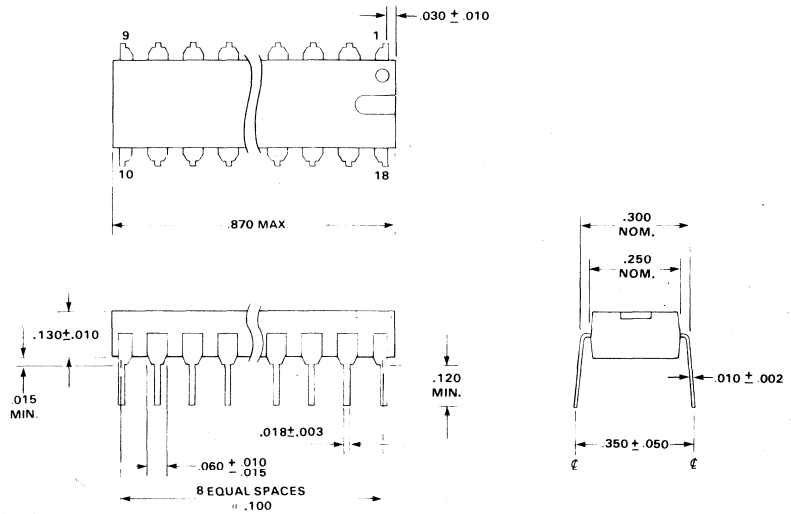


FIGURE 7 – MK5370 TYPICAL APPLICATION

PHYSICAL DIMENSIONS

MK5370



NOTE: Overall length includes .010 flash on either end of package

18-Pin DIP (N) (.300)
Plastic

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.:DSMK5370

THOMSON COMPONENTS MICONDUCTEURS

MK5371•MK5372

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

FEATURES

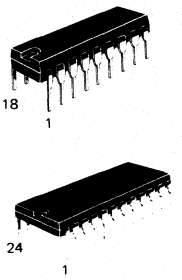
- Stand-alone DTMF and pulse signaling
- Softswitch automatically switches signaling mode
- Recall of last number dialed (up to 28 digits long)
- Flash key input initiates timed hook flash
- Microprocessor interface (BCD inputs) for smart telephones
- Timed PABX pause
- 10/20 PPS select option
- Form-A and 2-of-8 keyboard interface
- Pacifier tone
- Powered from telephone line, low operating voltage for long loop applications

KEYPAD CONFIGURATION

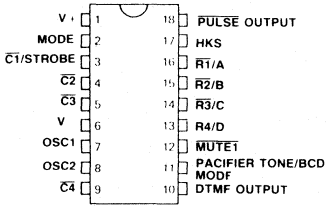
1	2	3	FLASH
4	5	6	MODE
7	8	9	PAUSE
*	0	#	LND

CMOS

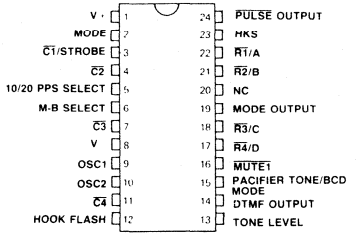
CASES



PIN ASSIGNMENTS



MK5371



MK5372

FEBRUARY 1987 1/16

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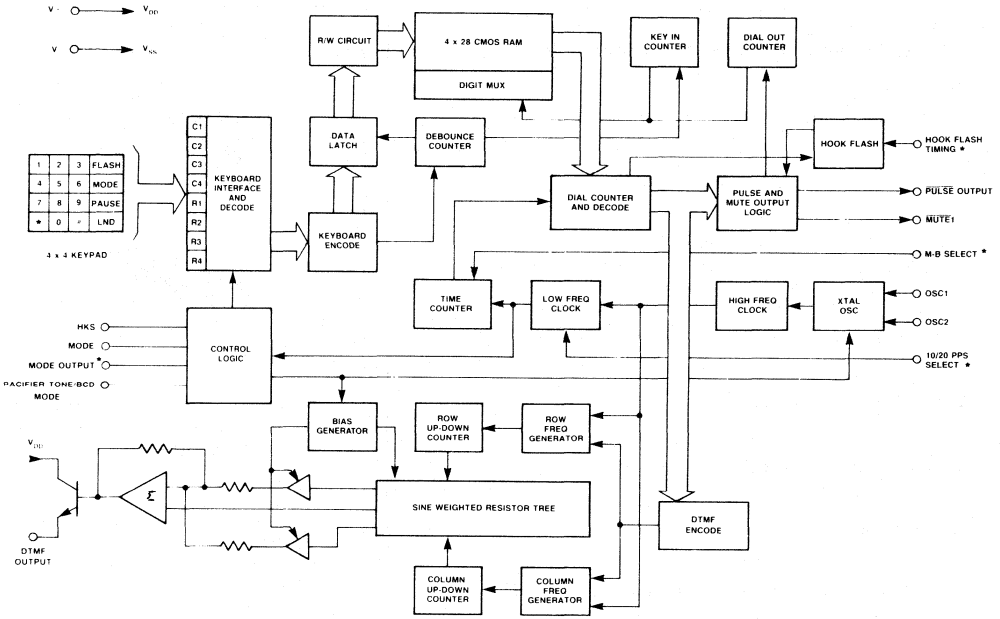
BLOCK DIAGRAM



DESCRIPTION

The MK5371 is a monolithic, integrated circuit manufactured using Mostek's Silicon Gate CMOS process. These circuits provide necessary signals for either DTMF or loop disconnect (Pulse) dialing. The MK5371 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and access several unique special functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch (Mode), Flash, and Pause.

A LND key input automatically redials the last number dialed. Keys entered during auto-dialing sequence will not be stored or dialed. However, auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed.

The Mode key simplifies the process of alternating dialing modes. This input automatically toggles the immediate dialing mode. The function is also stored in memory. During auto-redial, the signaling mode is toggled each time the Mode code appears in the digit sequence. The signaling mode always defaults to the mode selected (hardwire or switch) at Pin 2 (MODE) after a Power-Up-Clear initialization or a transition from on-hook to off-hook (HKS input switched from a high to low logic level). Switching modes through Pin 2 toggles the immediate dialing mode and changes the default, but it is not stored in memory.

Two features simplify PABX dialing. The pause key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signaling resumes. The Flash key simulates a hook flash to transfer calls or to activate other special features provided by the PABX or a central office. The MK5371 ensures exact timing for the hook flash.

In addition to interfacing with standard keypads, the MK5371 also accepts parallel BCD inputs. This feature simplifies interfacing a microprocessor-based design to the telephone line. The MK5371 buffers 28 bytes of information, including special functions.

All of the preceeding features are provided by the MK5371 in an 18-pin package. The same features are provided by the MK5372 in a more versatile 24-pin version. Additionally, the MK5372 includes RC programmable hook-flash timing, selectable tone levels, and both Make-Break (M-B) and 10/20 pulses-per-second selection in the pulse mode.

FUNCTIONAL DESCRIPTION

The following pin descriptions are numbered according to the 24-pin package. Pin numbers for the 18-pin version are listed in parenthesis under each pin name.

V+
Pin 1 (1). V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (See Electrical Specifications.)

MODE
Input. Pin 2 (2). MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V−), the default determines the signaling mode. A V+ connection defaults to Tone Mode operation and a V− connection defaults to Pulse Mode operation.

A Softswitch (Mode) code entered in a number sequence can temporarily modify the signaling mode. After encountering a first Softswitch code in a number sequence, the Signaling Mode toggles and is opposite the default determined by Pin 2. A second Softswitch code toggles the Signaling Mode a second time, returning the mode back to the default condition. Note that the Softswitch code performs a toggle function on the default state; switching the state of Pin 2 while dialing changes the default state as well as the immediate signaling mode.

$\overline{C1}$/STROBE, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$
Keyboard Input. Pins, 3, 4, 7, 11, 17, 18, 21, 22 (3, 4, 5, 9, 13, 14, 15, 16). The MK5371 interfaces with standard keypads as well as a microprocessor-driven 4-bit bus.

A valid keypad entry is either a single Row connected to a single Column or V- simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (Tdb) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information is valid, the information is buffered into the LND location. If switched on-hook, the keyboard inputs all pull high

through on-chip pull-up resistors. Information may still be entered into memory but it is not signaled and the keyboard scan is disabled. If users desire to enter data while on-hook, a 2-of-8 keypad with negative common is required.

A key entry during LND interrupts the sequence when it reaches the redial period until the key is released. Dialing then resumes. The key entered is not stored or dialed.

The keyboard inputs become high impedance when the Binary Input Mode is selected. As shown in Table 1, Row pins become inputs for the Binary codes from a microprocessor in this mode. Table 1 equates the Binary Codes to the keyboard digits and special functions. The $\overline{C1}$ input pin now provides an input for a strobe strobe used to clock the valid codes into the LND buffer. Dialing proceeds at the specified rates. The strobe duration must be active for at least 2 μs to ensure proper acceptance of the information. If the strobe remains high for longer than 96 ms false dialing may occur. A minimum of 8 ms must separate each strobe. Figure 1 illustrates the required strobe/data timing. Valid encoded signaling information must be present until the strobe goes low. Information entered during an on-hook operation is stored but signaling is inhibited. Changing between BCD and keyboard mode can only occur when the HKS input is high, or upon power-up. Caution, a power supply transient may be interpreted as a power-up condition, and the logic level on pin 15 (11) at that time will be interpreted as a valid BCD/Keyboard selection.

D	C	B	A	KEYBOARD FUNCTION	D	C	B	A	KEYBOARD FUNCTION
0	0	0	0	0	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	*
0	0	1	1	3	1	0	1	1	#
0	1	0	0	4	1	1	0	0	MODE
0	1	0	1	5	1	1	0	1	PAUSE
0	1	1	0	6	1	1	1	0	FLASH
0	1	1	1	7	1	1	1	1	LND

TABLE 1 – BINARY INPUT CODES

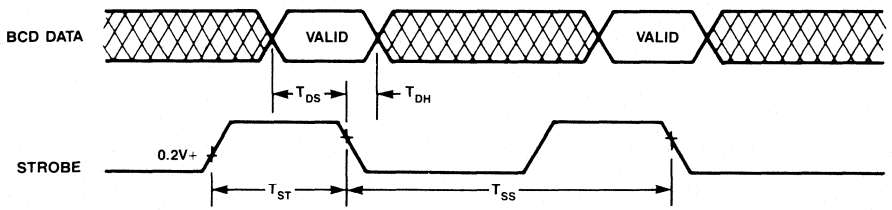


FIGURE 1 – BCD MODE STROBE INTERFACE TIMING

10/20 PPS SELECT
Input. Pin 5. In Pulse Mode, 10/20 PPS (pulses per second) SELECT allows users to double the dialing rate (20 PPS) by tying this pin high. If this input is left floating or is tied low, the dialing rate is 10 PPS. This input has no effect in Tone Mode.

M-B SELECT
Input. Pin 6. This pin is used to select the Make-Break ratio for pulse dialing. Table 2 shows the make and break timings obtained with either a logic 1 or logic 0 on this input. The 18-pin package has a predetermined Make-Break ratio of 40 to 60.

PIN 6 INPUT	MAKE TIME	BREAK TIME
V+	32	68
V−	40	60

TABLE 2 – MAKE-BREAK SELECT

V−
Input. Pin 8 (6). Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Input/Output. Pins 9, 10 (7, 8). OSC1 and OSC2 are inputs to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions.

HOOK FLASH
Input. Pin 12. HOOK FLASH lets users control the Flash signal duration. An external resistor and capacitor determine the exact duration of the Flash. Tying this input low results in a default Flash time period (600 ms), eliminating the need for an external RC. The RC values may be fixed or variable components may be used to ensure compatibility with all systems.

The component values required may be calculated using the following equation:

$$T_{FLASH} = 1.45\ RC$$

The capacitor should be no larger than 1μF. The time period may be made long enough to disconnect the telephone from the line. This may prove particularlly useful in microprocessor applications. The recommended range for the T_{FLASH} period is from 100 ms minimum to a maximum of two seconds.

TONE LEVEL

Input. Pin 13. The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 2. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK5372 is programmable between two methods for referencing the TONE LEVEL. The first method, selected by tying this pin low, is the supply-dependent TONE LEVEL where the TONE LEVEL is a linear function of the supply voltage (compatible with the MK5089). The second method, selected by tying this pin high, is the independent TONE LEVEL determined by an on-chip reference independent of the supply voltage (compatible with the MK5380). See Table 3.

Method 1 is designed to operate from a regulated supply and the TONE LEVEL is related to this supply by either of the following equations:

$$T_{O1} = 20\ LOG\ [(0.0776V+)/0.775]\ dBm$$

$$T_{O1} = 0.0776(V+)\ VRMS$$

TONE LEVEL SELECT INPUT	TONE REFERENCE	COMPATIBLE WITH
V− (Method 1)	Supply	MK5089
V+ (Method 2)	On-Chip Reference	MK5380

TABLE 3 – TONE LEVEL SELECT

The DC component of the DTMF (Method 1) output while active is described by the following equation:

$$V_{DC_1} = 0.66\ V+ - 0.6\ \text{Volts}$$

Method 2 provides a constant tone output and modulates its own supply in a minimum parts count configuration. The minimum instantaneous voltage level required for proper operation is 2.5 volts with the device modulating its own supply. This version may also be operated on a regulated supply, but users should be aware that operation below 3.0 volts could cause excessive distortion.

The TONE LEVEL, when used in a subscriber set without a regulated supply, is a function of the output resistor R_E and the telephone AC impedance Z_L. The low-group single tone output amplitude is a function of R_E and Z_L by the relationship:

$$V_O / T_O = 1/[0.2 + R_E/Z_L]$$

where V_O is the tone output amplitude at the phone line, and Z_L is the equivalent AC impedance in shunt with the tone generator. Z_L typically varies with loop current. R_E is the resistor value from DTMF OUTPUT to V−. In a 2500-type application, Z_L varies from 200 to 500 ohms. Thus, at the phone line, tone output levels range from 200 to 400 mVRMS, depending on loop current.

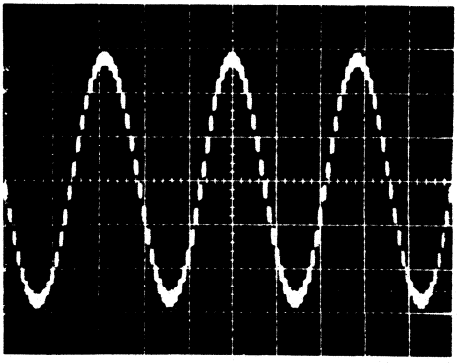


FIGURE 2 – SINGLE TONE

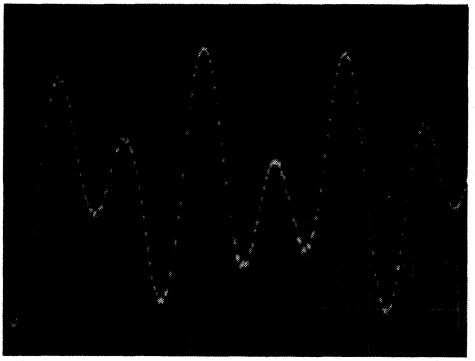


FIGURE 3 – DUAL TONE

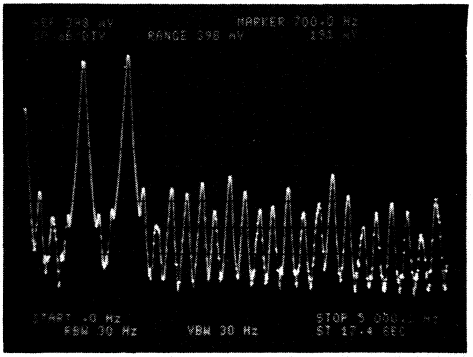


FIGURE 4 – SPECTRAL RESPONSE

The DC component of the DTMF output while active is described by the following equation:

$$V_{DC_2} = 0.3\ V+ + 0.5\ \text{Volts}$$

MODE OUTPUT

Output. Pin 19. MODE OUTPUT is driven by an open drain N-channel device. It provides an active low level in Pulse Mode only and is high impedence during Tone Mode and when the device is switched on-hook. It provides a means for indicating the active dialing mode.

DTMF OUTPUT

Output. Pin 14 (10). An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column Tones together. Figure 4 shows the timing at this pin.

PACIFIER TONE OUTPUT/BCD MODE

Input/Output. Pin 15 (11). A 500 Hz square wave is activated at this pin upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In the Pulse mode the PACIFIER TONE is activated for all key entries. The PACIFIER TONE provides audible feedback, confirming that the key has been properly entered and accepted. In Tone mode, only the LND key activates the PACIFIER TONE.

This pin is normally high impedance until a key is entered. Connecting this pin high through a resistor causes the circuit to accept BCD inputs through the ROW pins. In Binary Mode, as mentioned in the keyboard interface description, the keyboard inputs are all high impedance. Keypad inputs in this mode are not recognized. Connecting this pin low enables the keyboard scan circuitry, which allows entries. The mode of operation is selected upon power-up, and thereafter may only occur when HKS pin 23 (17) is high.

KEY INPUT	STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW 1	697	699.1	+0.31
2	770	766.2	−0.49
3	852	847.4	−0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	−0.32
3	1477	1471.9	−0.35

TABLE 4 – DTMF OUTPUT FREQUENCY

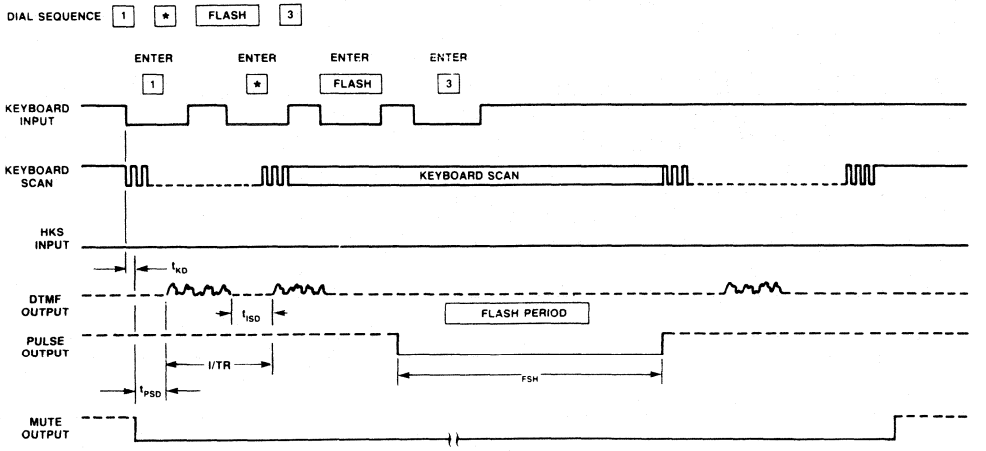


FIGURE 5 – TONE MODE TIMING

MUTE1
Output. Pin 16 (12). This pin is the Mute Output for both Tone and Pulse Modes. Timing is dependent upon mode.

The output consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In Tone Mode, $\overline{\text{MUTE1}}$ removes the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE1}}$ is active continuously until dialing is completed.

In Pulse Mode, $\overline{\text{MUTE1}}$ removes the receiver or the network from the line. Different circuitry is required for Tone and Pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE1}}$ timing is shown in Figure 6 for Pulse Mode signaling and Figure 5 for Tone Mode signaling.

HKS
Input. Pin 23 (17). Pin 23 is the hookswitch input to the MK5372. This is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at Pin 2.

$\overline{\text{PULSE}}$ OUTPUT
Output. Pin 24 (18). This pin has a dual function determined by the dialing mode selected. In Pulse Mode, the pin is an output consisting of an open drain N-channel device with zener protection. The break timing at this output meets Bell Telephone and EIA specifications for loop disconnect signaling. The Make/Break ratio is not user selectable in the 18-pin version. $\overline{\text{PULSE}}$ OUTPUT also provides the break timing for the hook flash function. Figure 6 shows this timing.

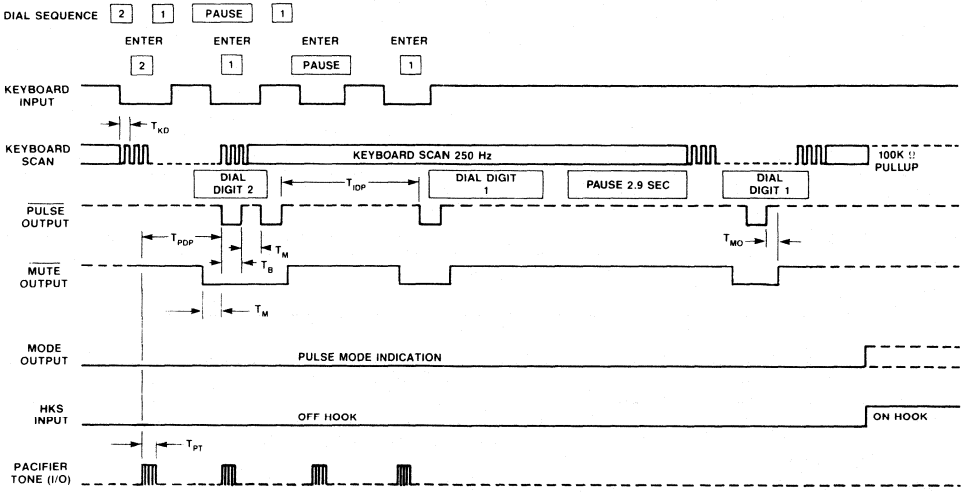


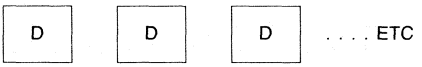
FIGURE 6 – PULSE MODE TIMING

DEVICE OPERATION (Tone Mode)

When the MK5371 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are pulled high. Key entries are not recognized unless they utilize a keypad common connection to force the respective Row and Column inputs low. These inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, the Mute Output is activated, and dialing begins after a pre-signal delay of 100 ms. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an intersignal time of 102 ms.

One important feature of the dialer is its ability to buffer data into the RAM before signaling. This feature allows less expensive keyboards to be used because signal distortion and double digit entry caused by bouncing and bounding of the keypad are eliminated. This design also ensures that data stored in the buffer exactly matches the digits actually dialed.

NORMAL DIALING (Off-Hook)

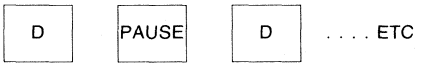


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

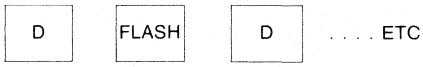
Last Number Dialing is accomplished by entering the LND key.

PABX PAUSE



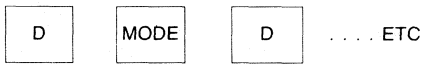
A pause may be entered into the dialed sequence at any point by keying in the special function key, Pause. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 5.

HOOK FLASH



HOOK FLASH may be entered into the dialed sequence at any point by keying in the function key, Flash. The flash function is stored in the LND buffer just like any other digit, but it will not be redialed, and acts much like Pause. Flash consists of a timed Break whose period is determined by the RC value used on Pin 12 (MK5372). Tying this input low will set HOOK FLASH to the chip default time of 600 ms. The MK5371 has a HOOK FLASH time of 600 ms.

SOFTSWITCH



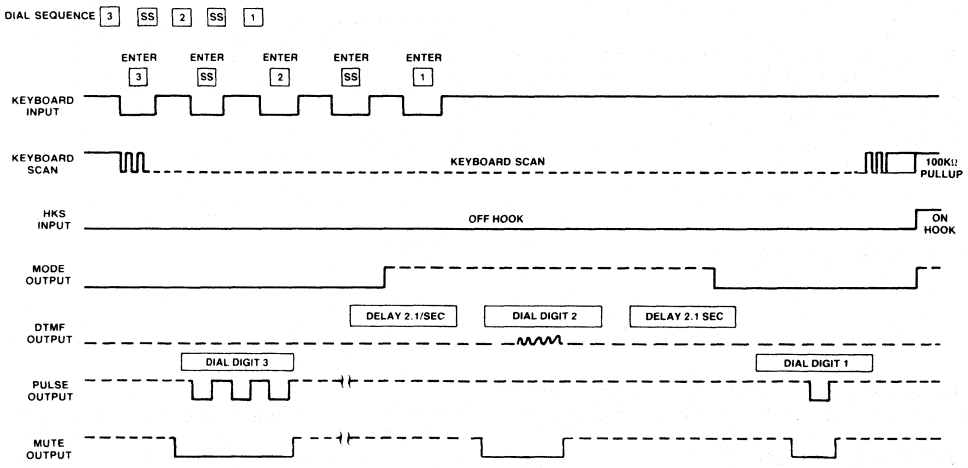
Softswitch allows the user to easily switch from Pulse to Tone Mode while dialing a number sequence. For example, the first digits may be entered in Pulse Mode. Signaling will proceed in Pulse Mode until a Softswitch (Mode) entry is encountered. Any subsequent digits are dialed using DTMF signals. A hookswitch transition or a second Softswitch entry returns dialing to the original Default Mode.

Each special function provides a built-in delay before auto-dialing resumes. The fixed delay introduced by the function is 1.1 seconds. In addition, the fixed delay is preceded and followed by the standard interdigital pause period that depends on the selected signaling mode. Table 5 lists the actual delays produced by each function.

FUNCTION	DELAY	PULSE MODE	TONE MODE
PAUSE	IDP + 1.1 + IDP	2.9 sec	1.3 sec
SOFTSWITCH	IDP + 1.1 + IDP	2.1 sec	2.1 sec
FLASH (RC)	.6 + IDP	1.5 sec	0.7 sec
(V−)	IDP	0.9 sec	0.1 sec

NOTE:
The Flash delay times do not include the break interval, only the time following break.

TABLE 5 – SPECIAL FUNCTION DELAY PERIODS



NOTE: SS = Softswitch

FIGURE 7 – PULSE AND TONE MODE TIMING

MAXIMUM RATINGS*

DC Supply Voltage ..... 6.5 Volt
Operating Temperature ..... −30°C to +60°C
Storage Temperature ..... −55°C to +125°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+)+0.3, (V−)−0.3 volt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage	2.5		6.0	Volt	
V_{MR}	Memory Retention Voltage	1.5	1.3		Volt	1, 6
I_S	Standby Current		0.2	.750	μA	1
I_{MR}	Memory Retention Current		0.10	0.75	μA	5, 6
I_T	Operating Current (Tone)		300	600	μA	2
I_P	Operating Current (Pulse)		225	350	μA	2
I_{ML}	Mute Output Sink Current	1.0	2.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pullup Resistance		100		kohm	
K_{RD}	Keypad Pulldown Resistance		750		ohm	
V_{IL}	BCD/Keypad Input Level-Low	0		0.2V+	V	
V_{IH}	BCD/Keypad Input Level-High	0.7V+		V+	V	

NOTES:
1. All inputs unloaded. Quiescent Mode (oscillator off). V · 2.5 V
2. All outputs unloaded, single key input
3. V_{OUT} 0.5 Volts. V · 2.5 V
4. Sink Current for V_{OUT} 0.5. Source Current for V_{OUT} 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_{KD}	Keypad Debounce Time		32		ms	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		ms	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone Duration		30		ms	1
T_{HFP}	Hookflash Timing		600		ms	1, 3
F_{SR}	BCD Strobe Rate			124	1/sec	1
T_{DS}	Data Setup	2			μs	1, 2
T_{DH}	Data Hold	1			μs	1, 2
T_{ST}	Strobe Width	2		96000	μs	1, 2
T_{SS}	Strobe Separation	9			ms	

NOTES:
1. Crystal oscillator accuracy directly affects these times.
2. Figure 1 illustrates this timing relationship.
3. HOOK FLASH pin input must be tied to V on the 24-pin version, otherwise this time is described by external RC values.

AC CHARACTERISTICS – PULSE MODE OPERATION

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
P_R	Pulse Rate		10	20	PPS	1
T_{PDP}	Predigital Pause		140		ms	2
T_{IDP}	Interdigital Pause		940		ms	2
T_{MO}	Mute Overlap Time		4		ms	2
T_B	Break Time (MK5371) (MK5372 Pin 6 to V+) (MK5372 Pin 6 to V−)		60 68 60		ms	2

NOTES:
1. 10 PPS is the nominal rate; 20 PPS is available on the 24-pin version.
2. Figure 6 illustrates this relationship.

AC CHARACTERISTICS – TONE MODE

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_{NK}	Tone Output No Key Down			−80	dBm	1
T_{Od}	Tone Output (dependent)	−13 173	−12 194	−11 218	dBm mV_{rms}	1, 2 5
PE_d	Pre-Emphasis, High Band	2.3	2.7	3.1	dB	
DC_d	Tone Output DC Bias	1.0	1.2		V	4
T_{Oi}	Tone Output (independent)	−13	−12 194	−11	dBm mV_{rms}	2, 3
PE_i	Pre-Emphasis, High Band		2.0		dB	3
DC_i	Tone Output DC Bias		1.2		V	4
R_E	Tone Output Load		10		kohm	5
T_{RIS}	Tone Output Rise Time		0.1	1.0	ms	6
DIS	Output Distortion		5.0	8.0	%	3
TR	Tone Signaling Rate		5.0		1/sec	
T_{PSD}	Pre-Signal Delay		100		ms	7
T_{ISD}	Inter-Signal Delay		100		ms	

NOTES:

1. O dBm equals 1 mW power into 600 ohms (775 mVolts).
   Important Note: The MK5371/MK5372 are designed to drive a 10k ohm load. The 600 ohm load is only for reference.
2. Single tone (low group).
3. Supply voltage = 2.5 to 6 Volts, R_E = 10k ohms.
4. R_E = 10k ohms, V+ = 2.5 Volts
5. Supply voltage = 2.5 Volts. These specifications are supply-dependent
6. Time from beginning of tone output waveform to 90% of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_s < 100 Ω, L_m = 96 mH, C_m = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, and C_L = 18 pF.
7. Time from Mute active to beginning of signaling.

TYPICAL APPLICATION

The MK5371 Mostek Pulse Tone dialer provides both cost-effective telephone-line interface and the logic required for DTMF (Tone) and Loop Disconnect (Pulse) signaling.

Pulse dialing originated with the rotary dial telephone. The Mostek Pulse Tone dialer provides the same capability as the rotary dial telephone and the convenience of pushbutton entry. The subscriber set (telephone) is powered by loop current supplied by the telephone company. Signalling, in Pulse Mode, is accomplished by repeatedly interrupting the loop current. The central office senses, times, and counts each line "break"; the number of breaks corresponds to the digit dialed. The duration of the break period, the dialing rate, and the separation between consecutive digits (IDP time) are controlled by the Pulse Tone dialer IC. Loop disconnect dialing is nearly a world-standard concept.

DTMF signalling consists of modulating the telephone line with a signal comprised of two fundamental frequencies. Each frequency pair represents one of sixteen possible digit (or key) entries. Twelve of these frequency pairs are commonly used (0, 1, 2, ..., *, #). The Mostek Pulse Tone dialer provides DTMF signalling capability controlling signal duration, separation, level, and rate.

The typical application circuit in Figure 8 illustrates one way the Pulse Tone dialer can be used. The pulse output provides the signal to break the line to transistor Q3. Q3 switches off, eliminating the base current to Q4, which also switches off. The majority of the loop current is then eliminated, resullting in a break condition. The IC dialer must be protected from large voltage fluctuations, such as that caused by interrupting the loop current. Transistor Q1 along with R2, C1, and Z1 regulate the voltage to the dialer. The Mute Output signal is active while signalling each digit to mute popping noises at the receiver (earpiece or speaker).

The DTMF tone output drives the base of Q8, which modulates the line. The tone level at tip and ring is determined by the effective impedance of the telephone line and the speech network.

Mode of operation is controlled by switch S1 (which sets the default dialing mode) and the keypad. A change of dialing mode with a Mode (Softswitch) key input is stored in memory and will be repeated when the LND (last number dialed) feature is activated.

Resistor R1 provides a small memory-retention bias current to prevent the device from powering down while on hook. The current required for long term memory retention is less than 1μA.

A ceramic sounder can also be interfaced to pin 11 (BCD/PACIFIER TONE) of the device. A pacifier tone signal is activated for each key entry. This feature provides an audible indication for each valid key entry. Keys may be entered faster than the maximum signalling rate allows. Audible feedback confirms proper key entry.

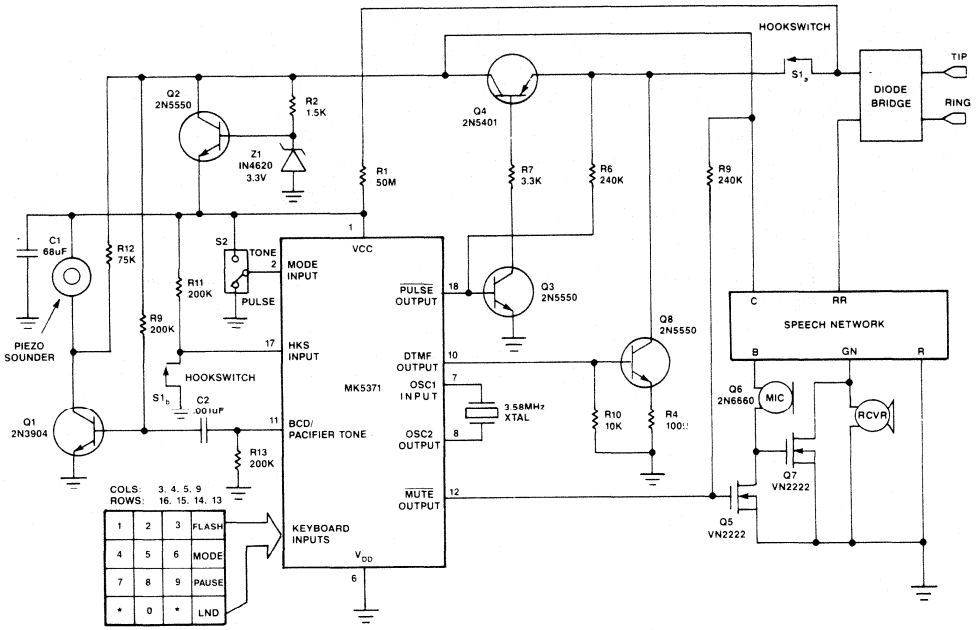
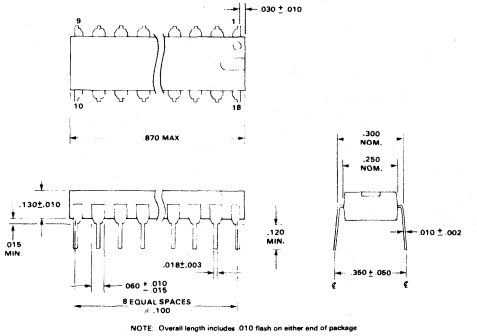


FIGURE 8 – MK5371 TYPICAL APPLICATION

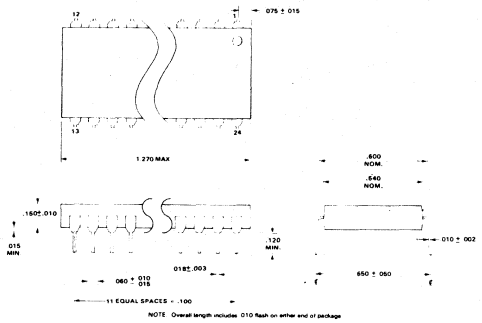
PHYSICAL DIMENSIONS

MK5371



18-Pin DIP (N) (.300)
Plastic

MK5372



24-Pin DIP (N) (.600)
Plastic

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSMK53715372

MK53721

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

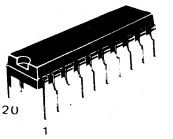
PRODUCT PREVIEW

CMOS

FEATURES

- Options tailored for specific countries selectable through single pin.
- Single chip mixed mode dialer allows dialing in either tone or pulse modes. A * or « SOFTSWITCH » key input can also be used to switch from Pulse to Tone mode operation and is stored in memory.
- 28 digit storage with LNR (last number redial).
- P.I.N. (personal identity number) protection method.
- Sliding cursor method to simplify PABX dialing.
- Hookswitch debounce, transients due to line reversals and drop-outs can be masked for a period determined by external resistor.
- Powered from telephone line, low standby current and operating voltage.
- DTMF signal consistent with key entry period.
- Minimum DTMF signal duration/separation guaranteed.
- Timed PABX pause may be stored in Memory.
- Timed FLASH for extended timed Break recall.

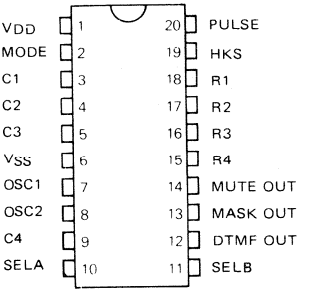
CASE



KEYPAD CONFIGURATION

1	2	3	FLASH
4	5	6	SS
7	8	9	PAUSE
★	0	#	LNR

PIN ASSIGNMENT



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PIN DESCRIPTIONS

Name	No	Pin Type	Description
V_{DD}	1	S	Positive Supply
V_{SS}	6	S	Negative Supply (ref. for all voltages)
OSC1	8	1	Oscillator input for 3.579545 MHz crystal
OSC2	9	0	Oscillator input
MODE	2	1	Selects TONE or PULSE default operation
SELA	10	1	Selects Option group C1-C5 by connecting this pint to -Col1, -Col2, .. -Col4 or
SELB	11	1	Selects Option Group R1-R5
HKS	19	1	Hookswitch detect, logic 1-"off-hook"
DTMF OUT	12	0	DTMF output NPN emitter follower
MASK OUT	13	0	Mask output for Pulse mode operation, Nch open drain, active high
MUTE OUT	14	0	Mute output for Tone mode operation, Nch open drain, active high
PULSE OUT	20	0	PULSE output for precise break timing, Nch open drain, active high
-COL1-	3	1	Column keypad connections
-COL2-	4	1	
-COL3-	5	1	
-COL4-	9	1	
-ROW4-	18	1	Row keypad connections
-ROW3-	17	1	
-ROW2-	16	1	
-ROW1-	15	1	

DESCRIPTION

The MK53721 is a 20 pin CMOS mixed mode dialer IC designed and manufactured by Thomson Components Mostek Corporation (TCMC). This dialer provides signalling for both TONE (MF, DTMF) and PULSE (LD) modes of operation. All digits entered are stored in a 28-digit buffer and can be recalled with a single LNR (last number redial) command entry.

The MK53721 can be switched from PULSE to TONE mode operation through the keypad with a * key input of softswitch (SS) key input. All inputs following a softswitch command will generate DTMF signals. The softswitch command is stored in memory but P.I.N. (personal identity number) protection does not allow information stored in the buffer following a softswitch (SS or *) in pulse mode or, * and = in tone mode, to be redialed.

A PAUSE command introduces a timed delay into the dial sequence. This is entered manually and the delay time is determined by the options selected. A timed break recall (FLASH) command produces a timed break at the PULSE OUTPUT pin.

A sliding cursor has been included to allow redial of the buffer contents after digits have been manually entered. If the new sequence matches the previous memory contents an LNR input will redial the remaining digits. If there is an error in matching the LNR is inhibited.

On hook, the keypad inputs are disabled eliminating possible current draw in this state. Off hook, the keypad inputs are enabled. A key entry, connecting a single column pin to a single row pin, is detected and the oscillator is activated. The keypad is scanned and debounced to verify the key input and the data in then stored into the LNR buffer (if storable).

In Tone mode operation the DTMF OUT becomes active after the debounce period (32 ms) and remains active as long as a valid key input remains. If the key input is shorter than the debounce period the input is ignored. Internal timing circuitry also guarantees a minimum DTMF burst duration and separation. Key entries may proceed faster than the signalling rate without introducing errors. The Mute Output is provided to attenuate the tone level at the receiver and remove the transmitter during DTMF dialing.

In Pulse mode operation the PULSE OUT becomes active following the debounce period and a short predigital pause period. A Mask Output is provided to remove the speech network from the line or to attenuate the current spikes which reach the receiver when PULSE dialing.

Two select pins (SELA, SELB) have been provided which allow the part to be customized for various markets. Rather than selecting and modifying individual parameters which would take many pins or mask options each select pin will select groups of options which have been identified for particular markets.

FUNCTIONAL DESCRIPTION

DTMF OUTPUT

The DTMF OUTPUT is driven by a bipolar (NPN) emitter follower with the collector tied to VDO. The DTMF OUT signal is a summation of the keyboard selected High group (column) and Low group (row) tones. The amplitude of these tones is determined internal to the chip and is independent of supply and temperature.

The tones are synthesized using a resistor tree with sinusoidally weighted taps. The frequency and accuracy of the synthesized tones is listed in the following table. Note, variations in the oscillator frequency (using the 3.579545 MHz crystal) will be reflected in the frequency of the synthesized tones.

Key input	Standard frequency	Actual frequency	% deviation
ROW 1	697	699.1	+ 0.31
2	770	766.2	− 0.49
3	852	847.4	− 0.54
4	941	948.0	+ 0.74
COL 1	1209	1215.9	+ 0.57
2	1336	1331.7	− 0.32
3	1477	1471.9	− 0.35

KEYBOARD INTERFACE

The MK53721 has eight keyboard interface pins which are to connected to a 4x4 keypad with FORM A (SPST) switches. A 2-of-8 keyboard with negative common may also be used if the common is left unconnected (do not connect common to VSS).

The keyboard is disabled while "on-hook". Off-hook, the column and row keys assumed opposite scan states. Keyboard scan is enabled when a valid input is detected. The scan frequency is 250 Hz.

HOOKSWITCH INPUT

The MKS INPUT (HOOKSWITCH) informs the MK53721 of the state of the telephone. A logic "1" (connected to VDO) indicates the telephone set is in the "off-hook" state and dialing is enabled. A logic "O" (connected to VSS) indicates the telephone set is "on-hook", dialing is disabled, and the chip will not draw extra current if keys are pressed. This ensures that only the memory retention current is required while on hook.

The MKS INPUT is level sensitive which simplifies the implementation of hookswitch debounce. Transients caused by interruptions in loop current during exchange operations will not cause inadvertent "on-hook" detection. The length of debounce is determined by the value of the pullup resistor and capacitor connected externally. The suggested debounce periods range from 50 ms to 500 ms. A valid hookswitch transition will terminate signalling in progress and reset the dialing mode to the default mode determined by the MODE INPUT (pin 2). The MKS debounce time is determined by the following equation:

$$T(HSDS) = 1.5 * REXT * CEXT$$

EARTH LOOP RECALL (ELR)

Earth loop recall is not generated by the MK53721 but can be detected by applying a logic "0" level directly to the hookswitch. The hookswitch debounce is bypassed by applying logic levels directly to the MKS pin (input not connected through external resistor). The ELR detect is identical to a hookswitch input without the debounce.

LAST NUMBER REDIAL

LNR (last number redial) command causes the contents of the LNR buffer to be dialed. Numbers which include a softswitch are limited by P.I.N. protection described below. LNR does not have to be the initial key input since the MK53721 features a "sliding cursor" as described below.

The LNR buffer can store 28 digits but any number of digits may be dialed manually. The memory storage will wrap-around after the first 28 digits have been entered and the additional inputs will be stored beginning in the first memory location. After wrap-around has occured the LNR command will be disabled to prevent misdials.

FLASH

The FLASH command is stored in the LNR buffer and when signaled it initiates a times break. This timing is determined by the options selected. Some options will reset the memory after a flash and additional inputs will begin a new number sequence. If this option is selected new digits will not be accepted until the FLASH is completed.

Other options will continue accepting inputs and storing these sequentially in the buffer. These digits cannot be redialed. This method is standard unless stated otherwise in the options listing.

In both cases, signalling will revert to the default dialing mode determined by the MODE INPUT following the FLASH command execution and the FLASH itself is never redialed.

P.I.N. PROTECTION

The P.I.N. (Personal Identity Protection) feature of the MK53721 will protect numbers which are likely to be used in confidential transactions. Digits entered after a * or = key in TONE mode, or "softswitch" command (either a * input or SS input while in PULSE mode) are considered private. These digits cannot be redialed and therefore the users privacy is not compromised. The exception to this is a * or = key at the beginning of a sequence, in this case radial of the entire sequence is allowed. Some options available have this feature disabled.

SLIDING CURSOR

The sliding cursor feature simplifies PABX access and redial. The MK53721 will compare all digits as they are entered to the previous memory contents. If all digits entered equal the memory contents the LNR command can be activated at any point in the dialing sequence.

PAUSE

The PAUSE command is used to insert a fixed time delay into a number sequence, so that the dialer will delay a fixed time when redialing the number. The delay is programmable with the SELB option pin.

An AUTO-PAUSE INSERTION (API) feature is also available as an option. The pause is inserted automatically into a number sequence if manual dialing is interrupted by a delay of more than one second following the signalling of the last digit entered. Not more than two APIs' will be entered for each number sequence.

A-OPTIONS

The SELA pin is used to select groups of parameters and modify the operation of some of the special features. These groups are tailored for specific users. A major benefit of this approach simplifies the design of telephones for the international market. The option groups are selected by connecting the SELA pin (number 10) to one of the row or column pins for a total of eight possible choices. Following the first key entry after switching "off-hook" the option cannot be changed.

Option	Pin	M/B	PDP	IDP	FLSH	Tone	Functions
A1	-COL1-	32/68	940	940	100	80/80	API (auto-pause insertion)
A2	-COL2-	32/68	240	840	100	98/98	Flash only in tone mode
A3	-COL3-	32/68	240	840	200	80/80	*GEN DTMF tone both modes
A4	-COL4-	32/68	240	840	100	98/98	
A5	-ROW1-	40/60	240	840	600	98/98	16FPS in pulse mode
A6	-ROW2-	32/68	240	840	100	80/80	New Zealand dial 9, 8, 7 ... 0
A7	-ROW3-	40/60	240	840	100	80/80	Swedish dial 0, 1, 2 ... 9
A8	-ROW4-	40/60	240	840	600	80/80	Reset first key after flash

A1: GERMANY
A2: UK
A3: FRANCE
A4:
A5: PANAMA (OTHER S. AMERICAN COUNTRIES)
A6: NEW ZEALAND
A7: SWEDEN
A8: USA

B-OPTIONS

SELB pin is used to select a default pulse rate and also determine the fixed delay time used for the PAUSE command. As with the A-Option there are eight alternatives to choose from. Following the first key entry after switching the HKB input from 0-1 the option cannot be switched.

Option	Pin	Pulse rate (FPS)	Pause Duration (SEC)
B1	-COL1-	10	1.1 · IDP
B2	-COL2-		3.0 · IDP
B3	-COL3-		6.0 · IDP
B4	-COL4-		INDEFINITE
B5	-ROW1-	20	1.1 · IDP
B6	-ROW2-		3.0 · IDP
B7	-ROW3-		6.0 · IDP
B8	-ROW4-		INDEFINITE

MAXIMUM RATING

Rating	Symbol	Value	Unit
DC supply voltage	V_{CC}	6.5	V
Operating temperature	T_{oper}	0 to 60	°C
Storage temperature	t_{stg}	− 55 to + 125	°C
Maximum power dissipation (25°C)	P_{tot}	500	mW
Maximum voltage on any pin	V_I (max)	$(V_{DD})+0.3$, $(V_{SS})-0.3$	V

ELECTRICAL OPERATING CHARACTERISTICS
DC CHARACTERISTICS

Characteristic	Sym.	Min.	Typ.	Max.	Unit.	Note
DC operating voltage tone mode	V_{DDT}	2.5	—	6.0	V	—
DC operating voltage pulse mode	V_{DDP}	2.0	—	6.0	V	—
Memory retention voltage	V_{MR}	1.5	1.3	—	V	4, 5
Mute operation	V_{MT}	1.8	—	—	V	—
Operating current pulse mode	I_{DDP}	--	150	250	μA	2
Operating current tone mode	I_{DDT}	—	300	600	μA	2
Standby current	I_{SS}	—	0.4	1.0	μA	1
Memory retention current	I_{MR}	—	0.2	0.8	μA	1, 5
Pulse/mute/mask output sink current	I_{SINK}	1.0		—	μA	3
Output low voltage (I_{SINK})	V_{OL}	—	—	0.5	V	—
Keyboard pullup resistance	K_{XU}	50	100	200	kΩ	—
Keyboard pulldown resistance	K_{RD}	100	500	1000	Ω	—
Input level low	V_{IL}	—	—	.2VDD	V	—
Input level high	V_{IH}	8VDD	—	—	V	—

AC CHARACTERISTICS

Characteristic	Sym.	Min.	Typ.	Max.	Unit.	Note
Tone output no key down	T_{NK}	—	—	80	dBm	6
Tone output (low group)	T_O	−13 173	−12 194	11 218	dBm mVrms	6, 7, 8, 9
Pre-emphasis 20 log (V_{CCL}/V_{ROW})	V_{PE}	2.0	—	2.75	dBm	
Tone DC bias	T_{DC}	—	1.6		V	—
Tone output load	T_{LOAD}			10	kΩ	
Tone output rise time	T_{RIS}	—	1.0	—	ms	10
Tone distortion	T_{DIS}	—	5.0	8.0	%	8

NOTES:

1. All inputs unloaded, quiescent mode (oscillator off).
2. All outputs unloaded, single key input.
3. $V_{OUT} = 0.4$ volts.
4. Memory retention voltage is the point where memory is guaranteed but circuit operation is not.
5. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. Both are not needed simultaneously.
6. 0 dBm equals 1 mW into 600 Ω or 775 mV. The MK53721 is designed to drive a 10 kΩ load. The 600 Ω load is only for reference.
7. Single tone (low group), as measured at pin 10.
8. Supply voltage from 2.5 to 6 V $R_{LOAD} = 10$ kΩ.
9. $R_{LOAD} = 10$ kΩ.
10. Time from beginning of tone output waveform to 90% of final magnitude.

TIMING CHARACTERISTICS

Parameter	Sym.	Min.	Typ.	Max.	Unit.	Notes
Keyboard debounce time	T_{KD}	—	32	—	ms	—
Keyboard scan frequency	F_{KS}	—	250	—	Hz	—
Hookflash break period	T_{HFP}	—	100	—	—	—
Tone presignal delay	T_{PSD}	—	—	40	ms	—
Tone intersignal delay	T_{ISD}	—	98/80	—	ms	—
Tone burst duration	T_{DOR}	98/80	—	—	ms	—
Pulses per second (pulse rate)	P_{PS}	—	10	—	P_{PS}	—
Predigital pause	P_{DP}	—	240	—	ms	—
Interdigital pause	I_{DP}	—	840	—	ms	—
Mute overlap pulse	T_{MO}	—	32	—	ms	—

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Ref DSMK53721

THOMSON COMPONENTS MICONDUCTEURS

MK53731

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

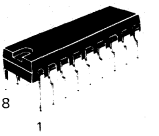
PRODUCT PREVIEW

CMOS

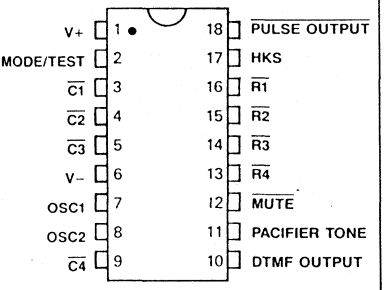
FEATURES

- Single chip DTMF and pulse dialer.
- Softswitch changes signaling mode from pulse to tone.
- Recall of last number dialed (up to 28 digits long).
- Flash key input initiates timed hook flash.
- Timed PABX pause.
- 8 Tones Per Second dialing in tone mode and 10 PPS in pulse mode.
- Continuous Tone.
- Pacifier tone.
- Powered from telephone line, low operating voltage for long loop applications.

CASE



PIN ASSIGNMENT



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DESCRIPTION

The MK53731 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53731 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, Flash, and Pause.

A LND key input automatically redials the last number dialed. Keys entered during auto-dialing sequence will be ignored. However, auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed.

1	2	3	FLASH
4	5	6	
7	8	9	PAUSE
* SOFTSWITCH	0	#	LND

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Printed in France

Ref.:DSMK53731

THOMSON COMPONENTS MICONDUCTEURS

MK5375

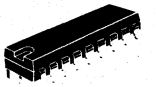
TEN-NUMBER REPERTORY TONE/PULSE DIALER

FEATURES

- CMOS Technology provides low-voltage operation
- Converts push-button inputs to both DTMF and loop-disconnect signals
- Stores ten 16-digit telephone numbers, including last number dialed
- Pacifier tone and PBX pause
- Last-number-dialed (LND) privacy
- Manual and auto-dialed digits may be cascaded
- Ability to store and dial both "*" and "#" DTMF signals
- Variable dialing rate
- On-chip power-up-clear guarantees data integrity

CMOS

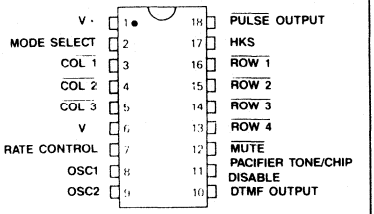
CASE



18

1

PIN ASSIGNMENT



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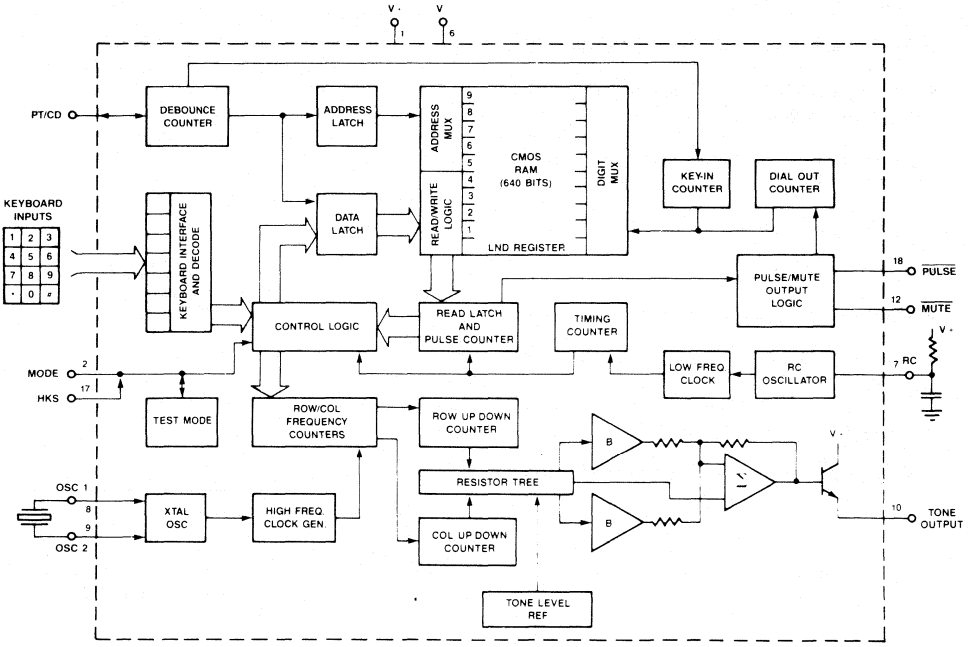
BLOCK DIAGRAM



DESCRIPTION

The MK5375 is a monolithic, integrated circuit manufactured using Mostek's proprietary Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. It also allows for the storage of ten telephone numbers, including as many as 16 digits each, in on-chip memory.

The MK5375 accepts rapid keypad inputs (up to 25 key entries per second) and buffers these inputs in the FIFO (First-In-First-Out) LND (Last-Number-Dialed) register. Each digit entry is accompanied by a pacifier tone, which is activated after the digit has been debounced, decoded, and properly stored. Signaling occurs at a rate determined by externally connected components, allowing the dialing rate to be adjusted for any system.

The flexibility of the dialer makes possible a variety of applications, such as "scratchpad" number storage. In "scratchpad" applications, the MK5375 inhibits signaling during entry, without interrupting a conversation.

Privacy is also an important feature. The MK5375 allows the LND (Last-Number-Dialed) buffer to be cleared following a call, without affecting data stored in other permanent memory locations. The memory in the permanent locations may be easily protected from inadvertent key entries with the addition of a simple "memory lock" switch to the application.

All of these options plus additional features are discussed in more detail in the following sections. The first section contains a brief detailed description of each pin function. The second section describes the device operation. This is followed by the DC and AC Electrical Specifications, and a few application suggestions.

FUNCTIONAL DESCRIPTION

V+ (Pin 1)

Pin 1 is the positive supply for the circuit and must meet the maximum and minimum voltage requirements as stated in the electrical specifications.

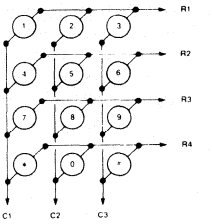
MODE SELECT (Pin 2)

In normal operations, Pin 2 determines the signaling mode used: a logic level 1 (V+) selects Tone Mode operation, while a logic level 0 (V−) selects Pulse Mode operation. This input must be tied to one of the supplies to guarantee proper dialing.

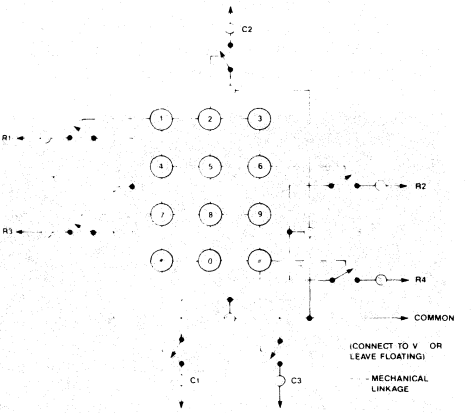
KEYBOARD INPUT: $\overline{COL1}$, $\overline{COL2}$, $\overline{COL3}$, $\overline{ROW4}$, $\overline{ROW3}$, $\overline{ROW2}$, $\overline{ROW1}$ (Pins 3,4,5,13,14,15,16)

The MK5375 keypad interface allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (FORM-A) keyboard to be used (Figure 1). A valid key entry is defined by either a single Row being connected to a single Column or by V− being presented to both a single Row and Column. In standby mode either all the rows will be a logic 1 (V+) and all the columns will be a logic 0 (V−), or vice versa.

The keyboard interface logic detects when an input is pulled low and enables the RC (Rate Control) oscillator and keypad scan. Scanning consists of alternately strobing the rows and columns high through on-chip pullups. After both valid row and column key closures have been detected, the debounce counter is enabled.



1A - CALCULATOR-TYPE KEYPAD



1B - STANDARD TELEPHONE-TYPE KEYPAD

FIGURE 1 – KEYPAD SCHEMATICS

Breaks in contact continuity (bouncing contacts, etc.) are ignored for a debounce period (T_{db}) of 32 ms. At this time the keypad is sampled, and if both row and column information is valid, this information is buffered into the LND location.

RATE CONTROL
(Pin 7)

The Rate Control input is a single-pin RC oscillator. An external resistor and capacitor determine the rate at which signaling occurs in both Tone and Pulse modes. An 8 kHz oscillation provides the nominal signaling rates of 10 PPS (Pulses per second) in Pulse Mode and 5 TPS (Tones per second) in Tone Mode; the Tone duty cycle is 98 ms on, 102 ms off. The RC values on this input can be adjusted to a maximum oscillation frequency of 16 kHz resulting in an effective Pulse rate of 20 PPS and a Tone rate of 10 TPS.

The frequency of oscillation is approximated by the following equation:

$$Fosc = 1/(1.49RC). \quad (1.0)$$

The value suggested for the capacitor (C) should be a maximum of 410 pF to guarantee the accuracy of the oscillator. The resistor is then selected for the desired signaling rate. Nominal frequency (8 kHz) is achieved with component values of 390 pF and 220 kohms. Parasitics must be taken into account.

OSCIN, OSCOUT
(Pins 8,9)

Pins 8 and 9 are the input and output, respectively, of an on-chip inverter with sufficient loop gain to oscillate when used in conjunction with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz, and any deviaton from this standard is directly reflected in the Tone Output frequencies.

This oscillator is under direct control of the repertory dialer and is enabled only when a tone signal is to be transmitted. During all other times it remains off, and the input has high impedance. The input OSCIN may be driven by an external source.

DTMF OUTPUT
(Pin 10)

The DTMF Output pin is connected internally to the emitter of an NPN transistor, which has its collector tied to V+, as shown on the functional block diagram.
The base of this transistor is the output of an on-chip operational amplifier that mixes the Row and Column Tones together.

The level of the DTMF Output is the sum of a single row frequency and a single column frequency. A typical single-tone sine wave is shown in Figure 2. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The tone level of the MK5375 is a function of the supply voltage. The voltage to the device may be regulated to achieve the desired tone level, which is related to the supply by either of the following equations:

$$T(O) = 20 \text{ LOG } [(0.078V+)/0.775] \text{ dBm.} \quad (2.0)$$
$$T(O) = 0.078(V+) \text{ VRMS. (Row tones)} \quad (2.1)$$

PACIFIER TONE OUTPUT / CHIP DISABLE
(Pin 11)

This pin normally has high impedance. Upon acceptance of a valid key input, and after the 32 ms debounce time, a 500 Hz square-wave will be output on this pin. The square-wave terminates after a maximum of 30 ms or when the valid key is no longer present. The purpose of this pacifier tone is to provide to the user audible feedback that a valid key has been entered. This feature is useful particularly for on-hook storage and pulse-mode signaling.

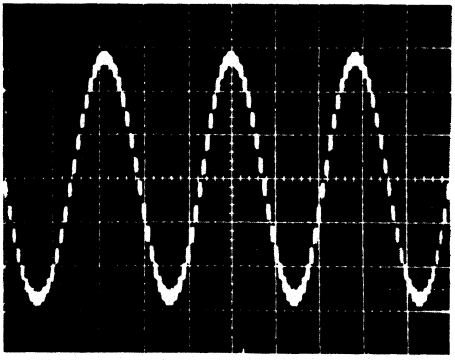


FIGURE 2A – TYPICAL SINE WAVE OUTPUT – SINGLE TONE

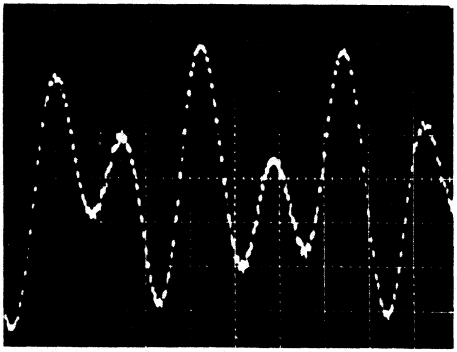


FIGURE 2B – TYPICAL DUAL-TONE WAVEFORM (Row1, Col 1)

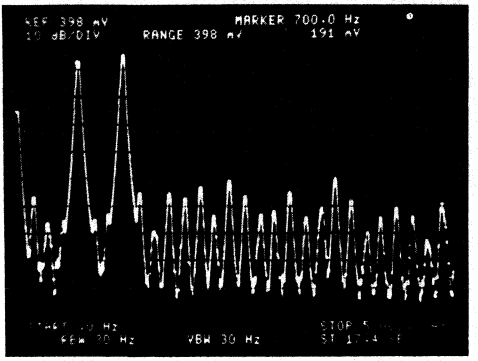


FIGURE 2C – SPECTRAL ANALYSIS OF WAVEFORM IN FIG.5
(Vert-10 dB/div, Horizontal - 600Hz/div.)

KEY INPUT		STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW	1	697	699.1	+0.31
	2	770	766.2	−0.49
	3	852	847.4	−0.54
	4	941	948.0	+0.74
COL	1	1209	1215.9	+0.57
	2	1336	1331.7	−0.32
	3	1477	1471.9	−0.35

TABLE 1 – OUTPUT FREQUENCY

The pacifier tone is not enabled when manually dialing in tone mode. This eliminates any confusion between the audible DTMF feedback and the pacifier tone, and prevents distortion of the DTMF signal by any of the pacifier tone frequency components. In both cases, the tone confirms that the key has been properly entered and accepted; whereas, without the tone, the user will not know if the keys have been properly entered.

IMPORTANT: This pin also serves as a chip-disable pin. Pulling this input high through a resistor will disable the keypad (high impedance) and initialize all counters and flip-flops (memory remains undisturbed). Pulling the input low through the same resistor enables the circuit. For the device to function properly, the resistor to V− (Pin 6) is required.

This feature is useful in several applications, as described in the application notes section.

MUTE OUTPUT
(Pin 12)

This pin is the Mute output for both Tone and Pulse modes of operation. The timing is dependent upon which mode is being used. The output consists of an open-drain, N-channel device. During standby, the output has high impedance and generally requires an external pullup resistor to the positive supply.

In Tone Mode, the Mute output is used to remove the transmitter and the receiver from the network during DTMF signaling. The output will mute continuously while auto-dialing and during manual DTMF signaling until each digit entered has been signaled.

In Pulse Mode of operation, the Mute output is used to remove the receiver or even the entire network from the line. These timing relationships are shown in Figure 4.

HKS INPUT
(Pin 17)

This pin is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input will cause the on-chip logic to initialize, terminating any operation in progress at the time. Signaling is inhibited while on-hook, but key inputs will be accepted and stored in the LND register. The information stored in the LND register may be copied into an alternate location only while on-hook. A logic level may be presented to this input, independent of the position of the hook-switch, allowing on-hook operations, such as storage, to be performed off-hook.

PULSE
(Pin 18)

This is an output driven by an open-drain, N-channel device. In Pulse Mode operation, the timing at this output meets Bell Telephone and EIA specifications for loop-disconnect signaling. The Make/Brake ratio is set to 40/60 on the standard MK5375. The pulse rate is determined by the RC values selected for the Rate Control, Pin 7. Note: The standard make/break ratio may not be suitable if the Pulse dialing rate is accelerated.

DEVICE OPERATION

The MK5375 can be used in low-priced phones with basic 3×4 matrix keypads. The block diagram shows the data and control signal flow between the various functional blocks. The keypad entries are decoded, debounced, and if valid, they are stored into the LND (Last-Number-Dialed) buffer, which acts much like a FIFO (First-In-First-Out) register. Each subsequent entry is stacked in the buffer. Typically, the dialing sequence begins 172 ms after the first digit is accepted in Pulse Mode operation and 132 ms in Tone Mode

operation. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an inter-signal time of 102 ms.

Buffering the data into the RAM prior to signaling is an important feature of the repertory dialer. It allows for the use of less expensive keypads, since the user cannot enter the digits too quickly for the system, and the pacifier tone can be used to provide audible feedback following each key entry not generating a DTMF signal. It also guarantees that the data stored in the RAM matches exactly the digits actually dialed.

Manual dialing and auto-dialing can be executed in any order, consecutively or cascaded. The dialer must complete auto-dialing the previous entry before another key is entered. Digits should not be entered while the device is auto-dialing. Most digits would be ignored unless preceded by a control key; in which case, an error in dialing may occur.

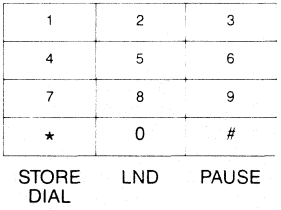


FIGURE 3 – KEYPAD CONFIGURATION

NORMAL DIALING

The "*" (STAR) key is used as the modifier to control repertory functions. All numeric keys will signal normally unless preceded by a modifier. To signal either a "*" or "#", these keys must be entered twice in succession. The first entry is not signaled or stored.

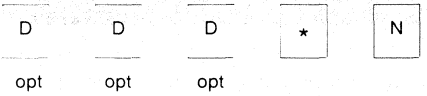
LND PRIVACY

A single "*" input prior to going on-hook or prior to coming off-hook will erase the information stored in the LND buffer.

AUTO DIALING (Off-Hook)

The key sequence "*", followed by any digit, will auto-dial the number sequence stored in the designated address location while off-hook.

STORAGE (On-Hook)



D is any data (telephone numbers) being entered or dialed. N is the address (memory location) in which numbers are stored. The number sequence stored in the LND buffer can be transferred to one of the other nine permanent locations with the simple sequence "*" followed by the address. New digits may be written into the LND buffer while on-hook. To enter either a "*" or "#" signal the digit must be entered twice in succession.

PABX PAUSE (Off-Hook and On-Hook)

An indefinite pause is stored in a number sequence by entering the "*" key modifier, followed by a "#" key input. When the number sequence is redialed, the dialer will pause when it encounters the "#" entry. A key input will cause it to continue.

PULSE DIALING

Most of the Pulse key operations are the same as they were in Tone Mode; PABX Pause is the only exception. In Pulse Mode, the pause may be stored as in tone mode, "* #", or with a single "#" input. Two "#" inputs will store two pauses.

The "*" key exercises the control function; two "*" inputs will be the same as a single input (multiple inputs are not accepted.)

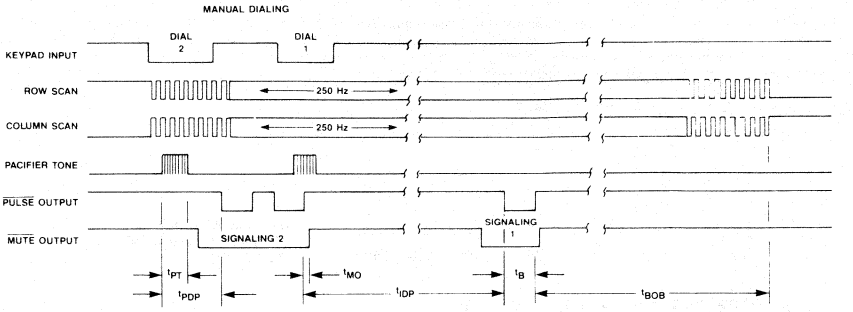


FIGURE 4A – MK5375 TIMING DIAGRAM – PULSE MODE OFF-HOOK OPERATION

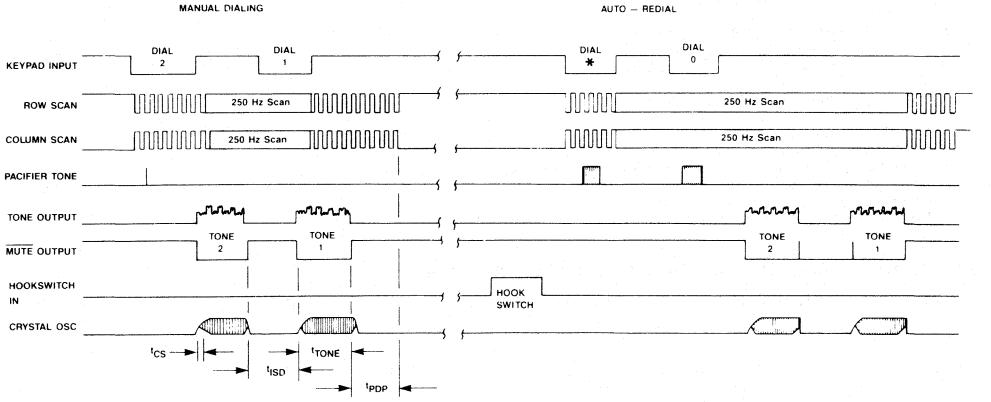


FIGURE 4B – MK5375 TIMING DIAGRAM – TONE MODE

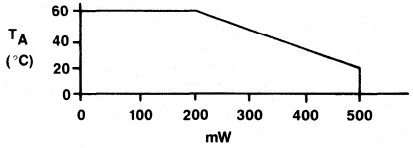
MAXIMUM RATINGS*

DC Supply Voltage V+ . . . . . 6.5 Volts
Operating Temperature . . . . . −30°C to +60°C
Storage Temperature . . . . . −55°C to +85°C
Maximum Power Dissipation (25°C) . . . . . 500 mW
Maximum Voltage on any Pin . . . . . (V+) + 0.3; (V−) − 0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL OPERATING CHARACTERISTICS

DC CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage	2.5		6.0	V	
I_{SB}	Standby Current		0.3	.75	μA	1
V_{MR}	Memory Retention Voltage	1.5	1.3		V	2
I_{MR}	Memory Retention Current	750	200		nA	2
I_T	Operating Current (Tone)		0.5	1.0	mA	3
I_P	Operating Current (Pulse)		50	150	μA	3
I_{ML}	Mute Output Sink Current	1.0	3.0		mA	4
I_{PL}	Pulse Output Sink Current	1.0	3.0		mA	4
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	5
K_{RU}	Keypad Pullup Resistance		100		kOHMS	
K_{RD}	Keypad Pulldown Resistance		500		OHMS	

NOTES:

(All specifications are for 2.5 volt operation, unless otherwise stated. Typical values are representative values at room temperature and are not tested or guaranteed parameters.)

1. All inputs unloaded. Quiescent Mode (Oscillator off)
2. Meeting these minimum supply requirements will guarantee the retention of data stored in memory.
3. All outputs unloaded, single key input
4. V_{OUT} 0.5 Volts
5. Sink current for V_{OUT} 0.5; source current for V_{OUT} 2.0 VOLTS

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
T_{KD}	Keypad Debounce Time		32		mSEC	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		mSEC	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone		30		mSEC	1
F_{RC}	Frequency RC Oscillator	−7.0	±2.5	+7.0	%	2

NOTES:

1. Times based upon 8 kHz RC input for Rate Control
2. Deviation of oscillator frequency takes into account all voltage (2.5 to 6.0 volts), temperature (30° to +60°C), and unit-to-unit variations. The tolerance of the external RC components or parasitic capacitance is not included.

AC CHARACTERISTICS – TONE MODE

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
T_{NK}	Tone Output No Key Down			-80	dBm	1
T_O	Tone Output (Row Tones)	-13 173	-12 194	-11 218	dBm mV (RMS)	1
PE	Pre-emphasis, High Band	2.2	2.7	3.2	dB	1
V_{DC}	Average DC Bias Tone Out		1.7		VOLTS	
DIS	Output Distortion		5.0	8.0	%	1
TR	Tone Signaling Rate		5	10	1/SEC	2
PSD	Pre-signal Delay		132		mSEC	2
ISD	Inter-signal Delay		100		mSEC	2

NOTES:
1. Load 10 kΩ
2. These values are directly related to the RC input to Pin 7, nominally 8 kHz.

AC CHARACTERISTICS – PULSE MODE OPERATION

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
P_R	Pulse Rate		10		PPS	1
PDP	Predigital Pause		172		mSEC	1
IDP	Interdigital Pause		940		mSEC	1
T_{MO}	Mute Overlap Time		2		mSEC	1

NOTES:
1. Typical times assume nominal RC input frequency of 8 kHz. An increase in frequency results in an equal decrease in time values and an equal increase in rate values.

APPLICATION CIRCUIT

The MK5375 integrated circuit provides the ability to convert keypad inputs into either DTMF or loop-disconnect signals compatible with most telephone systems. Both modes of signaling utilize loop currents to transmit the desired signaling information to the central office.

The circuit schematic in Figure 5 illustrates a typical implementation of the MK5375 dialer IC along with the necessary components required to interface with the telephone line in a tone/pulse application.

In loop-disconnect signaling, each digit dialed consists of a series of momentary interruptions of loop current called "breaks" (i.e., a digit "1" consists of a single break, a digit "2" consists of two breaks, and so on. The Pulse output is dedicated to loop-disconnect signaling and controls the flow of loop current through the speech network switching transistors, Q4 and Q5. The Mute output, through transistors Q2 and Q3, removes the receiver and transmitter to eliminate loud pops in the receiver caused by switching current through the network. The Pulse and Mute output signals, as shown in Figure 4A, consist of make, break, and interdigital time intervals.

DTMF signaling requires that the loop current be modulated, producing an analog signal on the telephone line. Transistor Q1 modulates the loop current by amplifying the DTMF signal coupled to its base from the Tone Output. The Mute output removes the receiver and transmitter by switching transistors Q2 and Q3. This eliminates any interference with the DTMF signal from the transmitter and cuts down on the amplitude of the DTMF tone heard at the receiver. The timing diagram in Figure 4B illustrates the time relationship between key entries, Tone Output, and -Mute- Output.

The voltage regulator circuit comprising resistor R2, zener diode Z2, and transistor Q6 serves several purposes. In tone mode operation, it provides the regulated supply voltage to the MK5375 which determines the DTMF signal amplitude at the Tone Output. Varying the supply voltage will vary the DTMF output signal. In pulse mode, it helps provide some isolation from the transients caused by switching the speech network in and out.

During normal off-hook dialing, the MK5375 operates using current from the telephone line. On-hook number storage and memory retention current are supplied by the battery shown in Figure 5. Transistor Q6 prevents the flow of battery current to the speech network.

The rate at which dialing occurs is determined by the values chosen for resistor R1 and capacitor C1. These values can be predetermined using equation (1.0) described above. The 3.5795 MHz crystal is used as a reference for synthesizing the DTMF signals and is activated only for the short periods during which these tones are being generated.

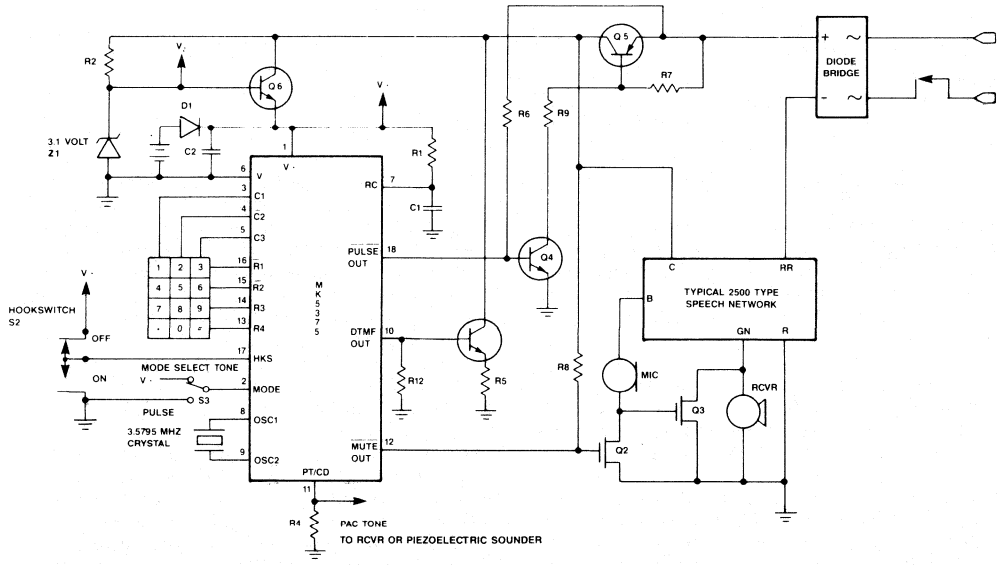
The application circuit schematic in Figure 6 gives an example of the various features which can be utilized with the addition of several switches. The example also shows that multiple devices may be used to increase the effective storage capability of the telephone design.

Much of the circuitry used to modulate and pulse the line, mute the speech network, and regulate the supply voltage is unchanged from the basic tone/pulse switchable telephone described above.

The two devices in Figure 6 are hooked up in parallel with one another except for their oscillator pins and the Chip Disable inputs. A DPDT switch is used to select between the two dialers through the Chip Disable pin; one device is activated while the other is put on standby.

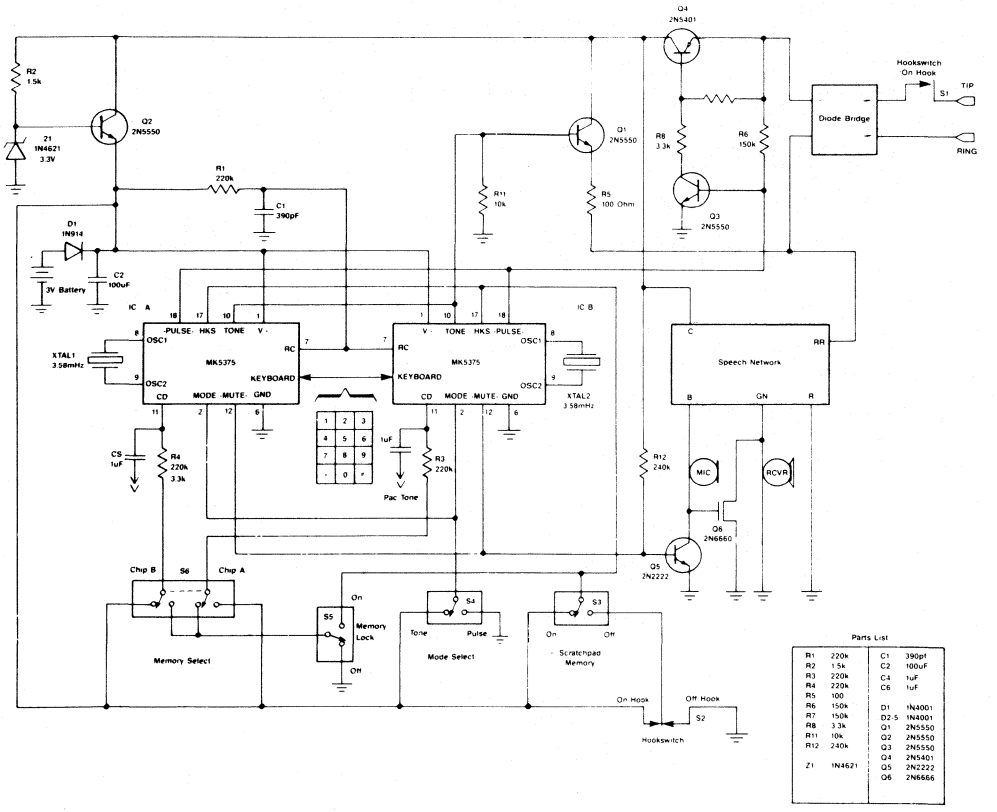
Some applications may include a memory lock switch to prevent any of the data stored to be changed inadvertently. This memory lock switch can take the form of a locking key switch, which would allow only the person with the key to alter data stored in memory.

A scratchpad feature may be implemented to allow off-hook programming of the memory while inhibiting dialing. A switch is added in series with the telephone hook-switch to allow the dialer to be forced into its on-hook key entry mode while the telephone set is off-hook.



R1	220K	Q1	2N5550	C1	390 PF
R2	1.6K	Q2	2N6660	C2	68μF
		Q3	2N6660		
R4	220K	Q4	2N5550	BATTERY 3 VOLT CELL	
R5	100Ω	Q5	2N5401	BRIDGE	
R6	160K	Q6	2N5550		
R7	150K	D1	1N914		
R8	240K	Z1	10K920		
R9	3.3K				
R12	10K				

FIGURE 5 – MK5375 CIRCUIT SHEMATIC



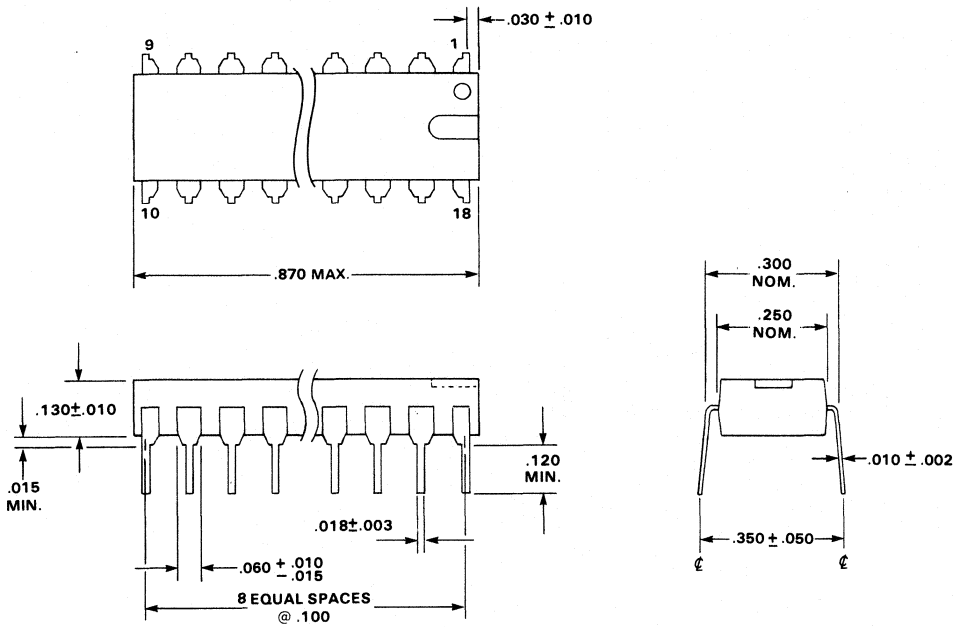
Parts List

R1	220k	C1	390pf
R2	1.5k	C2	100uF
R3	220k	C4	1uF
R4	220k	C6	1uF
R5	100		
R6	150k	D1	1N4001
R7	150k	D2-5	1N4001
R8	3.3k	Q1	2N5550
R11	10k	Q2	2N5550
R12	240k	Q3	2N5550
		Q4	2N5401
Z1	1N4621	Q5	2N2222
		Q6	2N6666

FIGURE 6 – MK5375 APPLICATION CIRCUIT SCHEMATIC

PHYSICAL DIMENSIONS

MK5375



NOTE: Overall length includes .010 flash on either end of package

18-Pin DIP (N) (.300)
Plastic

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSMK5375

HOMSON
COMPONENTS
MICONDUCTEURS

MK5376

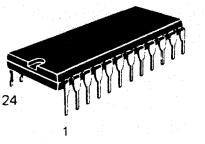
TEN-NUMBER REPERTORY TONE/PULSE DIALER

FEATURES

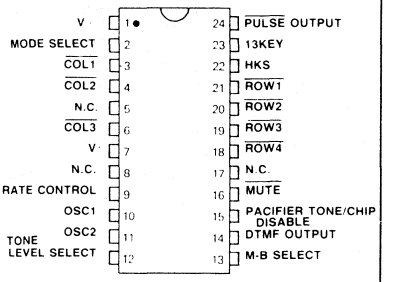
- Converts push-button inputs to both DTMF and pulse signals
- Stores ten 16-digit telephone numbers including last number dialed
- Pacifier tone and PBX pause
- Last number dialed (LND) privacy
- Manual and auto-dialed digits may be cascaded
- Ability to store and dial both * and # DTMF signals

CMOS

CASE



PIN ASSIGNMENT



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DESCRIPTION

The MK5376 is a monolithic, integrated circuit manufactured using Mostek's Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. Ten telephone numbers of up to 16 digits each may be stored in the on-chip RAM. Manual and auto-dialed numbers may be cascaded in any order.

Additional functions available are a Pacifier Tone output, PABX pause, external control of the signaling rate, and total functional control with either a standard 3x4 matrix keypad (FORM-A) or a 2-of-7 keyboard. A 13th key option allows control of the dialer's repertory features. The telephone keypad then functions for signaling purposes only, independent of the repertory functions. The 13th key mode and the M-B (Make/Break) Ratio is user selectable.

The dialer's flexibility provides for many applications, for example, off-hook programming, the use of additional chips in parallel for 10, 20, and 30 number repertory phones, permanent memory protection and the option of a supply-independent or supply-dependent tone level.

FUNCTIONAL DESCRIPTION

V+
Pin 1. Pin 1 is the positive supply for the circuit and must meet the voltage requirements defined in the Electrical Specifications.

MODE SELECT
Input. Pin 2. In normal operation, Pin 2 determines the Signaling Mode; a logic level 1 (V+) selects Tone Mode, while a logic level 0 (V−) selects Pulse Mode operation. To guarantee proper dialing, this input must be tied to one of the supplies.

$\overline{COL1}$, $\overline{COL2}$, $\overline{COL3}$, $\overline{ROW4}$, $\overline{ROW3}$, $\overline{ROW2}$, $\overline{ROW1}$
Keyboard Input. Pins 3, 4, 6, 18, 19, 20, 21. The MK5376 keypad interface allows users to add either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form-A) keyboard (see Figure 1). A valid key entry is either a single Row connected to a single Column or V− presented to both a single Row and Column. In Standby Mode, either all the Rows pull to a logic 1 (V+) and all the Columns are a logic 0 or vice versa.

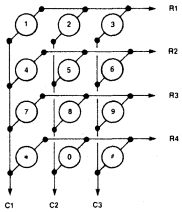


FIGURE 1A – KEYBOARD SCHEMATICS-CALCULATOR-TYPE KEYPAD

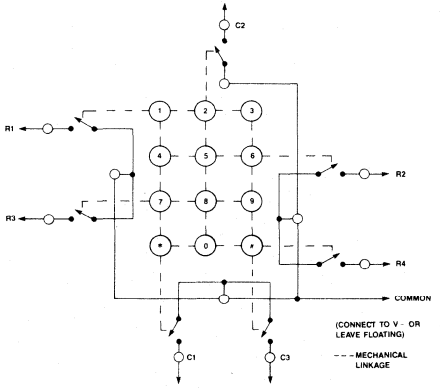


FIGURE 1B – KEYBOARD SCHEMATICS STANDARD TELEPHONE-TYPE KEYPAD

The keyboard interface logic detects an input being pulled low and enables the RC (RATE CONTROL) oscillator and keypad scan. Scanning consists of Rows and Columns alternately strobing high through on-chip pullups. After both a valid Row and Column key closure have been detected, the debounce counter is enabled. Breaks in contact continuity (bouncing contacts, etc.) are ignored for a debounce period (Tdb) of 32 ms. At this time, the keypad is sampled. If both Row and Column information is valid, this information is buffered into the LND.

V –

Input. Pin 7. This pin is the negative supply input to the device. This is the voltage reference for all specifications.

RATE CONTROL

Input. Pin 9. RATE CONTROL is a single-pin RC oscillator. An external resistor and capacitor determine signaling rates in both Tone and Pulse Modes. An 8 kHz oscillation provides nominal signaling rates of 10 PPS (pulses per second) in Pulse Mode and 5 TPS (tones per second) in Tone Mode; the tone duty cycle is 98 ms on, 102 ms off. RC values on this input can be adjusted to a maximum oscillation frequency of 16 kHz, resulting in an effective Pulse rate of 20 PPS and Tone rate of 10 TPS.

The following equation approximates the oscillation frequency:

$$Fosc = 1/(1.49RC)$$

The capacitor's (C) suggested value should be a maximum of 410 pF to guarantee accuracy of the oscillator. The resistor (R) is then selected for the desired signaling rate. The nominal frequency of 8 kHz is achieved with component values of 390 pF and 220K ohms.

OSC1, OSC2

Input/Output. Pins 10, 11. Pins 10 and 11 are the input and output, respectively, of an on-chip inverter. They have sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation is directly reflected in the Tone Output frequencies.

The repertory dialer directly controls the oscillator and is only enabled for tone signal transmission. It remains off at all other times and the input is high impedance. An external source may also drive the input.

TONE LEVEL SELECT

Input. Pin 12. The MK5376 has selectable tone levels with supply-independent or supply-dependent specifications. The tone levels available are similar to those provided on Mostek's industry standard MK5380 and MK5089 DTMF generators (see Table 1). The optimum tone scheme is application-dependent.

Tone Level Select Input	Tone Reference	Compatible With
V – (Method 1)	Supply	MK5089
V + (Method 2)	On-Chip Reference	MK5380

TABLE 1 – TONE LEVEL SELECT

Method 1 operates from a regulated supply. The tone level is related to this supply by either of the following equations:

$$T_O = 20 \text{ LOG } [0.0776 (V+)/0.775] \text{ dBm}$$
$$T_O = 0.0776 (V+) \text{ Vrms}$$

Method 2 provides a constant tone output and modulates its own supply in a minimum parts count configuration. The tone level, when used in a subscriber set, is a function of the output resistor R_E and the telephone AC resistance R_L. The low-group single tone output amplitude is a function of R_E and R_L described by the equation:

$$V_O = \{1/[0.2+R_E)/R_L]\}T_O$$

where V_O is the tone amplitude at the phone line and T_O is the tone level at the DTMF OUTPUT pin. This version may also be operated on a regulated supply, but users must observe additional caution to prevent signal distortion (clipping) on longer loops.

M/B SELECT
Input. Pin 13. In Pulse Mode, this pin selects the Make/Break ratio, or the percentage Break time per Pulse period (see Table 2).

M-B SELECT INPUT	BREAK TIME	MAKE TIME
V+	68	32
V−	60	40

TABLE 2 – MAKE/BREAK RATIO

DTMF OUTPUT
Output. Pin 14. The DTMF OUTPUT pin is connected internally to an NPN transistor's emitter with a collector tied to V+. The transistor base is the output of an on-chip operational amplifier that mixes the Row and Column Tones together.

The DTMF OUTPUT level is the sum of a single Row single tone sine wave is shown in Figure 2. This waveform is synthesized using a resistor tree with sinusoidally weighted taps. DTMF output frequencies are defined by Table 3.

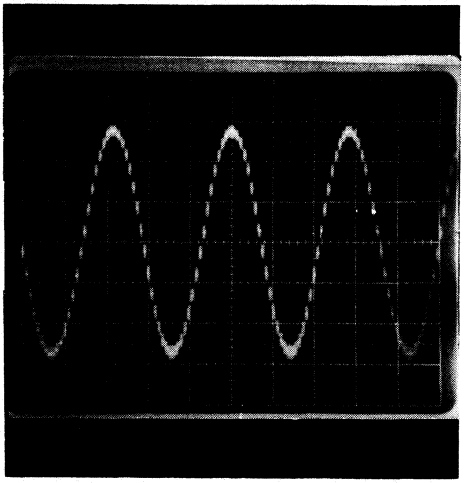


FIGURE 2 – TYPICAL SINE WAVE OUTPUT - SINGLE TONE

KEY INPUT	STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW 1	697	699.1	+0.31
2	770	766.2	−0.49
3	852	847.4	−0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	−0.32
3	1477	1471.9	−0.35

TABLE 3 – OUTPUT FREQUENCY

PACIFIER TONE OUTPUT/CHIP DISABLE
Input/Output. Pin 15. A 500 Hz square wave is output on this pin after acceptance of a valid key input and after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. The PACIFIER TONE audibly signals a valid key entry. This feature is particularly useful for on-hook storage and Pulse Mode signaling. The PACIFIER TONE is not enabled when users manually dial in Tone Mode. This eliminates any confusion between the audible DTMF feedback and the PACIFIER TONE. In both cases, the tone confirms that the key has been properly entered and accepted. Without the tone, users do not know if the keys have been properly entered.

This pin is normally high impedance until a key is entered. It also serves as a CHIP DISABLE pin. Pulling this input high through a resistor disables the keypad (high impedance) and initializes all counters and flip flops (memory remains undisturbed). Pulling the input low through the same resistor enables the circuit.

This feature is useful in several applications. It provides a convenient way to lock memory by connecting this input through a resistor to HKS. When it is on-hook, the device is then disabled and key inputs are not recogniz-

ed. The circuit will function normally off-hook. Information can only be entered into the permanent memory locations by switching to Program Mode. This requires that a switch and resistor be added to connect to V –.

$\overline{\text{MUTE}}$

Output. Pin 16. This pin is the mute output for both Tone and Pulse Modes. Timing depends on which mode is used.

The output consists of an open drain N-channel device and zener input protection. During standby, the output is high impedance and generally requires an external pullup resistor to the positive supply.

In Tone Mode, $\overline{\text{MUTE}}$ removes the transmitter and receiver from the network during DTMF signaling. The output then mutes continuously while auto-dialing and during manual DTMF signaling.

In Pulse Mode, the $\overline{\text{MUTE}}$ removes the receiver or even the entire network from the line. Timing is available both as a continuous mute (provided by the MK5376) or a mute that is active only when actually pulsing the line. Figure 3 depicts these timing relationships.

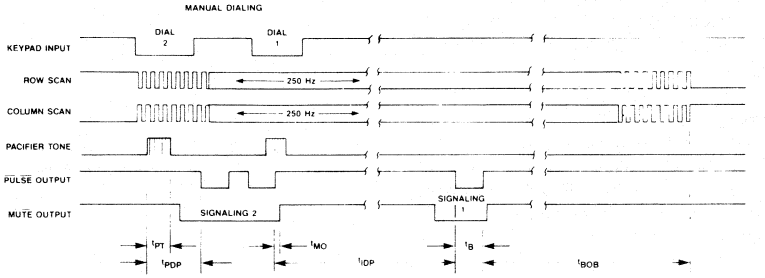


FIGURE 3A – MK5376 TIMING DIAGRAM – PULSE MODE OFF-HOOK OPERATION

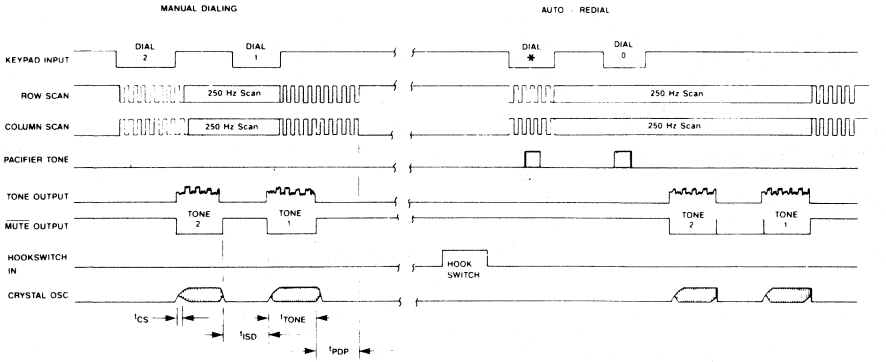


FIGURE 3B – MK5376 TIMING DIAGRAM – TONE MODE

HKS
Input. Pin 22. This pin is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input initializes the on-chip logic. This stops the current operation. A logic level independent of the hookswitch position may be presented to this input, which allows on-hook operations, such as storage, to be performed off-hook.

13KEY
Input. Pin 23. This pin is a high impedance input. When it is tied permanently low, it indicates 12KEY Mode. If users desire 13KEY operation, a switch to the negative supply is attached to this pin, along with an external pullup. This forces the repertory dialer into 13KEY Mode. The dialer switches to 12KEY mode if users depress the 13th key switch while simultaneously entering information through the keypad. The differences between these modes are presented in the Device Operation section.

$\overline{\text{PULSE}}$ OUTPUT
Output. Pin 24. An open drain N-channel device drives this pin. In Pulse Mode, the timing meets Bell Telephone and EIA specifications for loop disconnect signaling. The Make/Break ratio is user-selectable. RATE CONTROL regulates the dialing rate.

DEVICE OPERATION

The MK5376 interfaces to two keypad configurations - the 12KEY and 13KEY Modes (see Figures 4 and 5). This flexibility simplifies interfacing to existing keypads and products. The MK5376 can be used in inexpensive telephones with basic 3x4 matrix keypads to give them repertory dialer features. In 13KEY Mode, the MK5376 allows the keypad to be used for standard signaling and the special repertory functions are only activated by using the "control" (13th) key.

In both modes, keypad entries are decoded, debounced, and (if valid) stored in the LND (Last Number Dialed) buffer that acts much like a FIFO (First-In-First-Out) register. Each subsequent entry is stacked in the buffer. The dialing sequence begins 100 ms after the first digit is accepted. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and a 102 ms intersignal time.

Buffering data into the RAM before signaling is an important feature. This allows less expensive keypads to be used since users cannot enter digits too quickly for the system and the PACIFIER TONE can provide audible feedback after each non-toned key entry. It also guarantees that data stored in the RAM exactly matches the digits actually dialed.

Users can perform consecutive manual and auto-dialing, if auto-dialing is used to accomplish only a part of the desired number sequence. However, manual and auto-dialing cannot be performed simultaneously.

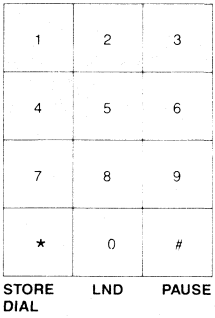


FIGURE 4 – KEYPAD CONFIGURATION 12KEY MODE (Tone Mode)

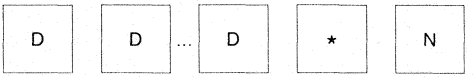
NORMAL DIALING

In 12KEY Mode, the "*" (Star) key is the modifier used to control repertory functions. All numeric keys signal normally unless a modifier precedes them. To signal either a "*" or "#," users must enter these keys twice in succession. The first entry is not signaled or stored.

LND PRIVACY

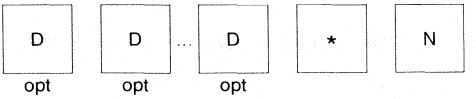
A "*" input prior to going on-hook erases information in the LND buffer.

AUTO-DIALING (Off-Hook)



The key sequence " * " followed by any digit auto-dials the number sequence stored in the designated address location. Note auto-dial can take place following manual key inputs.

STORAGE (On-Hook)



The number sequence stored in the LND buffer can be transferred to one of the nine other "permanent" locations with the simple sequence " * " followed by the address. New digits may be written into the LND buffer while on-hook. To enter a " * " signal, users enter the " * " key twice in succession as when dialed off-hook.

PABX PAUSE (Off-Hook and On-Hook)

When users input " * " key followed by a "#", an indefinite pause is stored in a number sequence. Upon redialing the number sequence, the dialer will pause when it encounters "#." A key input makes it continue.

KEYPAD CONFIGURATION 12KEY MODE (PULSE MODE)

Most of the Pulse key operations are identical to those in the 12KEY Tone Mode; PABX Pause is the only exception. In Pulse Mode, the pause is stored with a single "#" input. Two "#" inputs store two pauses.

The " * " key exercises the control function; two " * " inputs are the same as a single input (multiple inputs are not accepted).

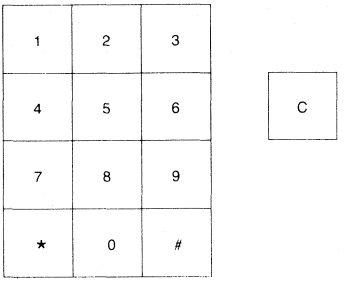
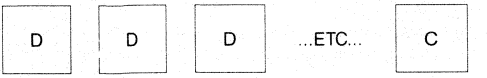


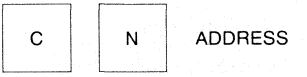
FIGURE 5 – KEYPAD SEQUENCE 13KEY CONFIGURATION

NORMAL DIALING AND LND PRIVACY OPTION (Off-Hook)



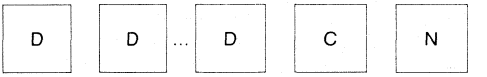
Normal dialing is straightforward; all keypad entries are stored in the LND (Last Number Dialed) buffer and signaled as each is entered. All digits in the LND register are maintained unless the final key prior to going on-hook is "C." In the metal mask version, the LND buffer is cleared unless users make a Control entry before going on-hook.

AUTO-DIALING (Off-Hook)



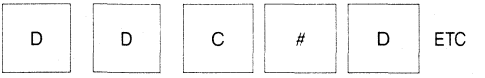
To auto-dial, users enter the control key "C," followed by the address key, (shown here as "N," representing memory location N). As soon as the address key is decoded and debounced, auto-dialing begins. Address zero is used to auto-dial LND.

STORAGE (On-Hook)



To store data in a given location (LOC N) users simply enter digits into the LND buffer and copy them to "N" by entering a control key "C" followed by the desired address. Users can copy the last number dialed before going on-hook to another location if they make no entries before the copy operation.

PABX PAUSE



Users may inject a pause at any point in the dialed sequences by keying in "C" followed by "#." When this number sequence is redialed, the dialer pauses indefinitely and continues to dial when another key input is received.

MAXIMUM RATINGS*

DC Supply Voltage ..... 6.5 Volts
Operating Temperature ..... −30 °C to +60 °C
Storage Temperature ..... −55 °C to +85 °C
Maximum Power Dissipation (25 °C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+) +0.3 Volts; (V−) −0.3 Volts

*All specifications are for 2.5 volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL OPERATING CHARACTERISTICS

DC CHARACTERISTICS

$-30\,°C \leq TA \leq 60\,°C$

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage	2.5		6.0	V	
I_{SB}	Standby Current		0.3	1.0	μA	1
V_{MR}	Memory Retention Voltage	1.5			V	5
I_{MR}	Memory Retention Current	750	200		nA	5
I_T	Operating Current (Tone)		0.5	1.0	mA	2
I_P	Operating Current (Pulse)		50	150	μA	2
I_{ML}	Mute Output Sink Current	1.0	3.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	3.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	Keypad Pulldown Resistance		500		kΩ	

NOTES:
1. All inputs unloaded. Quiescent Mode (oscillator off)
2. All inputs unloaded, single key input
3. V_{OUT} = 0.5 Volts
4. Sink Current for V_{OUT} = 0.5. Source Current for V_{OUT} = 2.0 Volts
5. Meeting these minimum supply requirements guarantees the retention of data stored in memory.

CHARACTERISTICS — KEYPAD INPUTS, PACIFIER TONE

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
T_{KD}	Keypad Debounce Time		32		ms	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		ms	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone		30		ms	1
F_{RC}	Frequency RC Oscillator	−7.0	+2.5	+7.0	%	2

NOTES:
1. Times based upon 8 kHz RC input for RATE CONTROL.
2. Deviation of oscillator frequency takes into account all voltage, temperature and unit-to-unit variations, but does not include the tolerance of external components.

CHARACTERISTICS — TONE MODE

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
T_{NK}	Tone Output No Key Down			−80	dBm	1
T_{Od}	Tone Output (dependent)	−13 173	−12 194	−11 218	dBm mV(rms)	1, 2
P_{Ed}	Pre-Emphasis, High Band		2.7		dB	
V_{DCd}	Average DC Bias Tone Out (V+ = 2.5 V)		1.2		Volts	
T_{Oi}	Tone Output (independent)		−12 194		dBm mV(rms)	2, 3
PE_i	Pre-Emphasis, High Band		2.0		dB	3
V_{DCi}	Average DC Bias Tone Out		1.5		Volts	
DIS	Output Distortion		5.0	8.0	%	3
R_E	Tone Output Load			10	kΩ	4
TR	Tone Signaling Rate		5	10	1/sec	5
PSD	Pre-Signal Delay		132		ms	5
ISD	Inter-Signal Delay		100		ms	5

NOTES:
1. ODBm equals 1 mWatt signal power into a 600 Ohm load or 775 mVolts
2. Single tone (low group) V· 2.5 V.
3. Supply voltage 2.5 to 6 volts. R_E 10K Ohms.
4. Maximum load which can be connected externally to pin 10 and maintain proper tone levels.
5. These values are directly related to the RC component values connected to Pin 7, the rate control frequency is nominally 8 kHz.

AC CHARACTERISTICS — PULSE MODE OPERATION

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
P_R	Pulse Rate		10		PPS	1
PDP	Predigital Pause		172		ms	1
IDP	Interdigital Pause		940		ms	1
T_{MO}	Mute Overlap Time		2		ms	1

NOTE:
1. Typical times assume nominal RC input frequency of 8 kHz. An increase in frequency results in an equal decrease in time values and increase in rate values.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

HOMSON
COMPONENTS
EMICONDUCTEURS

MK53761
REPERTORY DIALER

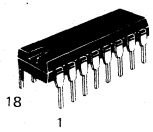
PRODUCT PREVIEW

CMOS

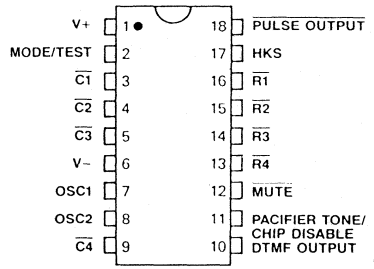
FEATURES

- Single chip DTMF and pulse dialer.
- Softswitch changes signaling mode from pulse to tone.
- Nine number repertory plus recall of last number dialed (18 digits each).
- Flash key input initiates timed hook flash.
- 8 Tone Per Second dialing in tone mode and 10 PPS in pulse mode.
- Continuous Tone.
- Pacifier tone.
- Powered from telephone line, low operating voltage for long loop applications.

CASE



PIN ASSIGNMENT



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DESCRIPTION

The MK53761 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53761 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, and Flash.

A LND key input automatically redials the last number dialed. Keys entered during auto-dialing sequence will be ignored. However, auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed.

The FLASH key simulates a 600 msec hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

1	2	3	FLASH
4	5	6	PROG
7	8	9	MEM
* SOFTSWITCH	0	#	LND

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HOMSON
COMPONENTS
EMICONDUCTEURS

MK53762
REPERTORY DIALER

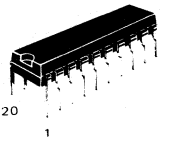
PRODUCT PREVIEW

CMOS

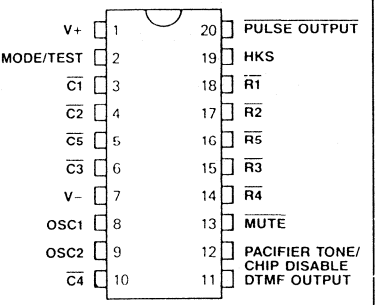
FEATURES

- Single chip DTMF and pulse dialer.
- Stores 10 18-digit telephone numbers, including last number dialed.
- Softswitch changes signaling mode from pulse to tone.
- Single button redial of all ten memories.
- Flash key input initiates timed hook flash.
- 8 Tones Per Second dialing in Tone Mode and 10 PPS in Pulse Mode.
- Continuous Tone.
- Pacifier tone for non-DTMF key entries.
- Powered from telephone line, low operating voltage for long loop applications.

CASE



PIN ASSIGNMENT



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DESCRIPTION

The MK53762 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53762 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, Flash, and 9 memories.

A LND key input automatically redials the last number dialed. Keys entered during auto-dialing sequence will be ignored. However, auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed.

The FLASH key simulates a 600 msec hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

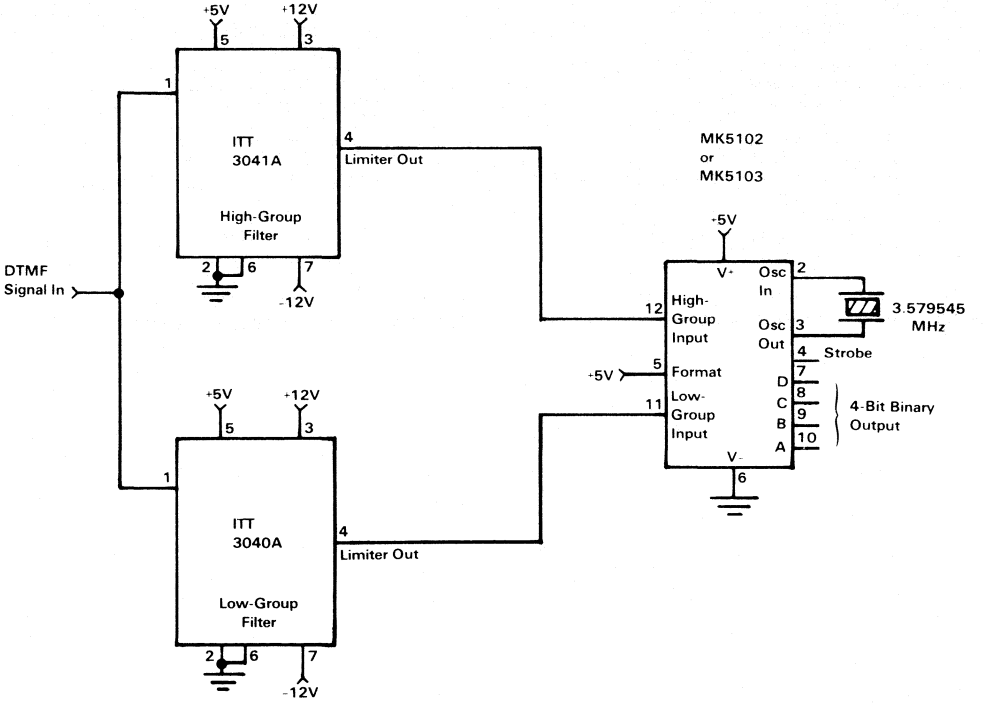
1	2	3	FLASH	MEM 9
4	5	6	PROG	MEM 8
7	8	9	PAUSE	MEM 7
* SOFTSWITCH	0	#	LND	MEM 6
MEM 1	MEM 2	MEM 3	MEM 4	MEM 5

Printed in France

Ref.DSMK53762

DTMF RECEIVER SYSTEM

A DTMF receiver system with a low parts count may be constructed using the MK5102 or MK5103 tone decoder and the ITT 3040A and ITT 3041A hybrid filter[1]. The ITT 3040A and ITT 3041A filters have on-chip limiters so that external squaring circuits are not needed. An alternate design allowing precise adjustment of external squaring circuits is described in another Mostek Application Note[2]. Tables 1 and 2 show the MITEL (CM7290) tape results using the ITT 3040A / 41A with the MK5102 and MK5103, respectively.



NOTES:

(1) ITT 3040A and ITT 3041A filters with limiters may be obtained from:
ITT North Microsystems Division
700 Hillsboro Plaza
Deerfield Beach, Florida 33441
Telephone: 305-421-8450
TWX: 510-953-7523

(2) MK5102N-5 DTMF Decoder Application Note, "Design Considerations for a DTMF Receiver System" is available from:
Mostek • Telecom Dept
1215 W. Crosby Rd.
Carrollton, Texas 75006
Telephone: 214-323-6000

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TEST #	RESULTS
2a, b	BW = 4.7 % of fo
2c, d	BW = 4.8 % of fo
2e, f	BW = 5.4 % of fo
2g, h	BW = 4.9 % of fo
2i, j	BW = 5.3 % of fo
2k, l	BW = 5.4 % of fo
2m, n	BW = 5.6 % of fo
2o, p	BW = 4.9 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio 19.7 dB
5	Dynamic Range 25 dB
6	Guard Time 32.9 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	3 Hits on Talk-Off Test

MK5102 with ITT 3040A and ITT 3041A
MITEL TAPE (CM7290) TEST RESULTS
Table 1

TEST #	RESULTS
2a, b	BW = 5.3 % of fo
2c, d	BW = 5.2 % of fo
2e, f	BW = 5.0 % of fo
2g, h	BW = 5.4 % of fo
2i, j	BW = 5.6 % of fo
2k, l	BW = 5.3 % of fo
2m, n	BW = 5.4 % of fo
2o, p	BW = 5.6 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 19.9 dB
5	Dynamic Range = 30 dB
6	Guard Time = 23.3 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	9 Hits on Talk-Off Test

MK5103 with ITT 3040A and ITT 3041A
MITEL TAPE (CM7290) TEST RESULTS
Table 2

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THOMSON COMPONENTS SEMICONDUCTEURS

MK5102

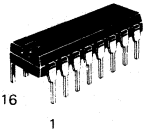
INTEGRATED TONE DECODER

FEATURES

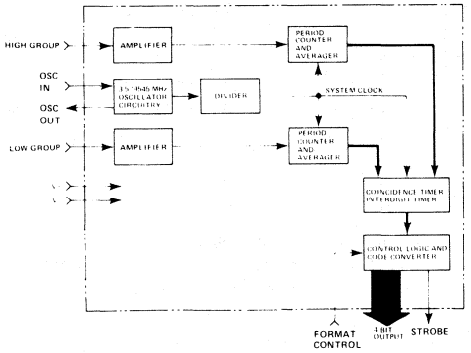
- Detects all 16 standard DTMF digits
- Requires minimum external parts count for minimum system cost
- Uses inexpensive 3.579545 MHz crystal for reference
- Digital counter detection with period averaging insures minimum false response
- 16-pin package for high system density
- Single supply 5 Volts ± 10%
- Output in either 4-bit binary code or dual 2-bit row/column code
- Latched outputs

CMOS

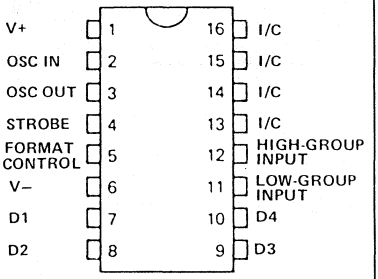
CASE



BLOC DIAGRAM



PIN ASSIGNMENT



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DESCRIPTION

The MK5102 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television colorburst crystal for reference, the MK5102 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5102 ideal for applications requiring minimum size and external parts count.

The MK5102 detects the high and low group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 33 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

The MK5102 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP Package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The MK5102 contains an on-board inverter with sufficient gain to provide oscillation when working with a low cost television "color burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins D1 through D4. This three-state input selects a 4-Bit Binary Code, a Dual 2-Bit Row/Column code, or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V–	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

	Col 1	Col 2	Col 3	Col 4
Row 1	1	2	3	A
Row 2	4	5	6	B
Row 3	7	8	9	C
Row 4	*	0	#	D

Note: Column 4 is for special applications and is not normally used in telephone dialing.

FIGURE 1 – DTMF DIALING MATRIX

The following table describes the two output codes.

	4-Bit Binary				Dual 2-Bit Row/Column			
					Row		Column	
Digit	D1	D2	D3	D4	D1	D2	D3	D4
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

Figure 1 shows the relationship between the data output code shown in Table 1 and the standard DTMF keyboard.

TABLE 1 – FORMAT CONTROL

Low Group f_o	High Group f_o
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

TABLE 2 – DETECTION FREQUENCY

OUTPUTS D1 THRU D4 (PINS 7 THRU 10)

Outputs D1 thru D4 are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

D1 thru D4 are the data out lines. The output data can be in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with D1 and D2 indicating the row selected, and D3 and D4 indicating the column selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

I/C (PINS 13 THRU 16)

Pins 13 thru 16 are internally connected and are intended to be left floating.

STROBE (Pin 4)

The STROBE output goes to a "1" when 33 milliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at D1-D4 are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

LOW-GROUP INPUT (Pin 11) and HIGH-GROUP INPUT (Pin 12)

The low- and high-group inputs are comparators that can detect capacitively-coupled square-wave signals as small as 0.9 volts peak-to-peak. The circuitry driving these inputs would typically use back-to-back silicon diodes as symmetrical limiters to regulate this level.

These inputs are biased to the midpoint of the supply with a resistive divider. Nominal input impedance is 100K Ω.

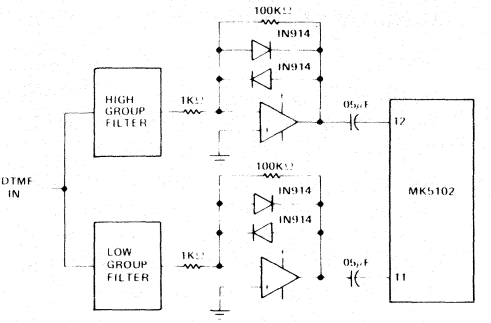
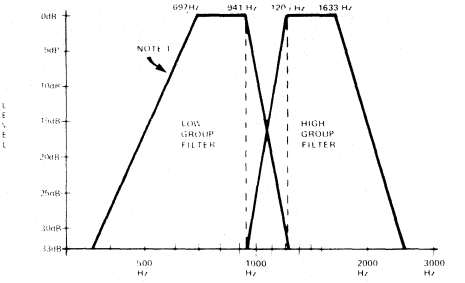


FIGURE 2 – SUGGESTED INPUT LIMITER CIRCUIT

INPUT BAND SPLIT REQUIREMENTS



RELATIVE INPUT LEVEL VS FREQUENCY

NOTES:

1. Dial tone notch filter adequate to maintain S/N ratio of ≥ 18dB in above pass bands.

2. Filter response described above will normally result in operation to 6dB of twist with 18dB S/N.

MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V–) ..... +6.0 Volts
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... –55°C to 100°C
Maximum Circuit Power Dissipation ..... 300 mW
Voltage on any pin, with respect to V– ..... –0.3 Volt
Voltage on any pin, with respect to V+ ..... +0.3 Volt

*Operation Above Absolute Maximum Ratings May Damage The Device

ELECTRICAL OPERATING CHARACTERISTICS

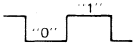
$0° C \leq T_A \leq 70° C$ V– = 0 Volts

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V+)	(V– = 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	50% Duty Cycle Square Wave	0.9		V+	Volts Peak-to-Peak	1,2
STROBE D1, D2, D3, D4 OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V+)–1		V+	Volts @ 0.1 mA	
FORMAT CONTROL Input	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V+) -0.5		V+	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		33			ms	4
Interdigit Interval		35			ms	4
Signal to Noise Ratio		18			dB	3
Supply Current @ 5.5V	Inputs and Outputs Unloaded		5	10	mA	

NOTES:

1. Due to internal biasing, this input must be capacitively coupled with a low leakage .05 μF capacitor.

2. No coupling capacitor is needed if the DTMF square wave meets the following criteria:



a. Logic "0" level = 1 Volt (max)
b. Logic "1" level = 4 Volts (min)

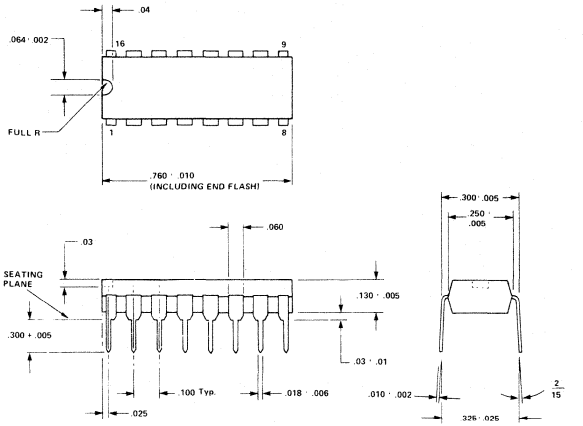
3. Signal-To-Noise Ratio is defined as:

$$SN = 20 \log \frac{SA}{NA}$$

where SA = RMS Amplitude of single tone being detected.
NA = RMS white noise in the band from 300Hz to 3.4KHz.

4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.

PHYSICAL DIMENSIONS



PLASTIC DIP
16-Pin

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THOMSON COMPONENTS MICONDUCTEURS

MK5103

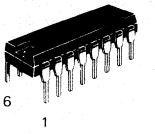
INTEGRATED TONE DECODER

FEATURES

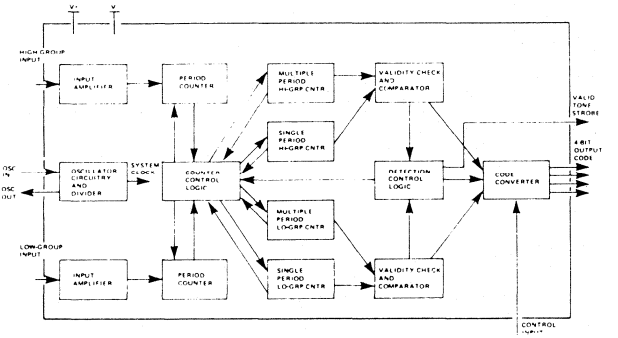
- Detects all 16 standard DTMF digits
- Requires minimum external parts count for minimum system cost
- Uses inexpensive 3.579545 MHz crystal for reference
- Digital counter detection with period averaging insures minimum false response
- 16-pin package for high system density
- Single supply: 5 volts ±10%
- Output in either 4-bit binary code or dual 2-bit row/column code
- Will operate at 14dB S/N ratio under worst-case signal conditions
- Latched outputs

CMOS

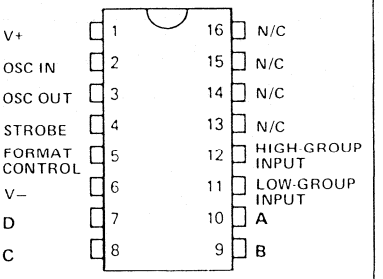
CASE



BLOCK DIAGRAM



PIN ASSIGNMENT



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DESCRIPTION

The MK5103 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television color-burst crystal for reference, the MK5103 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5103 ideal for applications requiring minimum size and external parts count.

The MK5103 detects the high- and low-group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 30 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

The MK5103 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The MK5103 contains an on-board inverter with sufficient gain to provide oscillation when working with a low-cost television "color-burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins 7 through 10. This three-state input selects a 4-bit Binary Code, a Dual 2-Bit Row/Column code, or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V-	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

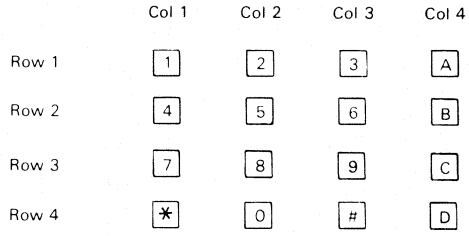
TABLE 1 – FORMAT CONTROL FUNCTIONS

The following table describes the two output codes.

Digit	4-Bit Binary D	C	B	A	Dual 2-Bit Row D	C	Column B	A
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

TABLE 2

Figure 1 shows the relationship between the data output code shown in Table 2 and the standard DTMF keyboard.



Note: Column 4 is for special applications and is not normally used in telephone dialing.

FIGURE 1 – DTMF DIALING MATRIX

Table 3 shows the detection frequency associated with each row or column:

Low Group fo	High Group fo
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

TABLE 3 – DETECTION FREQUENCY

OUTPUTS A THRU D (PINS 7 THRU 10)

Outputs A thru D are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

A thru D are the data out lines. The output data can be in in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with A and B indicating the column selected, and C and D indicating the row selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

N/C (PINS 13 THRU 16)

Pins 13 thru 16 are not internally connected and may be used as tie points.

STROBE (PIN 4)

The STROBE output goes to a "1" when 30 milliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at A-D are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

LOW-GROUP INPUT (PIN 11) AND HIGH-GROUP INPUT (PIN 12)

The circuitry driving these inputs, as shown in Figure 4, should be squaring circuits which use resistive dividers to set the output duty cycle to 50%. The squaring circuit shown was designed to provide hysteresis and allow the circuit to respond to signal levels of -28dBm or greater, where -28dBm corresponds to a peak-to-peak voltage of 87.1 mV. Any squaring circuit providing a 47% - 53% duty cycle over the receiver and dynamic range is sufficient.

The high-group and low-group signals are provided by the high-group filter and the low-group filter, as shown in Figure 2. These filters have the response characteristics shown in Figure 3 and are used to separate the DTMF signal into its high-group and low-group components.

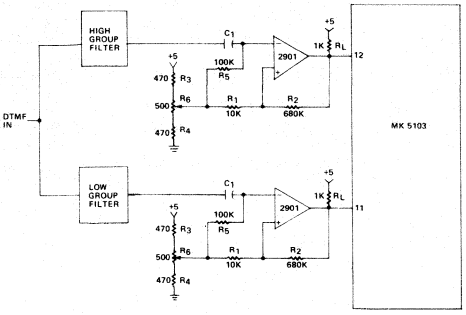
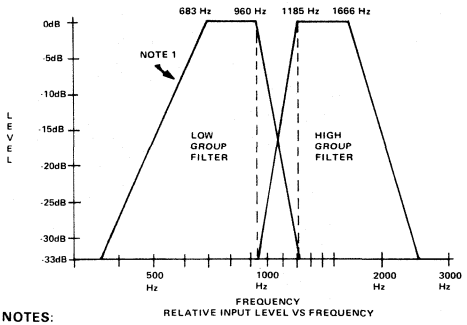


FIGURE 2 – SUGGESTED INPUT LIMITER CIRCUIT

APPLICATIONS

Two possible applications of the MK5103 are shown in Figure 4 and Figure 5. The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 6. On this circuit, the MK5103N-5, CD4556 and MK5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK5103N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.



NOTES:
RELATIVE INPUT LEVEL VS FREQUENCY

FIGURE 3 – INPUT BAND SEPARATION FILTER

For simple remote-control applications, the circuit of Figure 5 is useful. After a valid tone is detected, strobe will go high and one of the 16 outputs on the binary-to-1-of-16 encoder will go true. Thus, a DTMF transmitter and 16-key keyboard can be used to control 1 of 16 functions in a DTMF receiver.

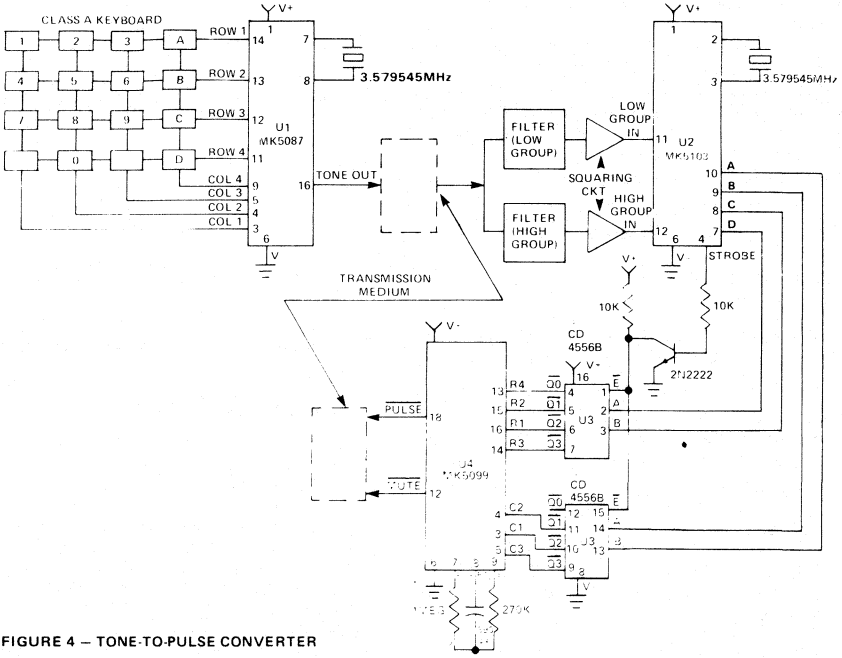


FIGURE 4 – TONE-TO-PULSE CONVERTER

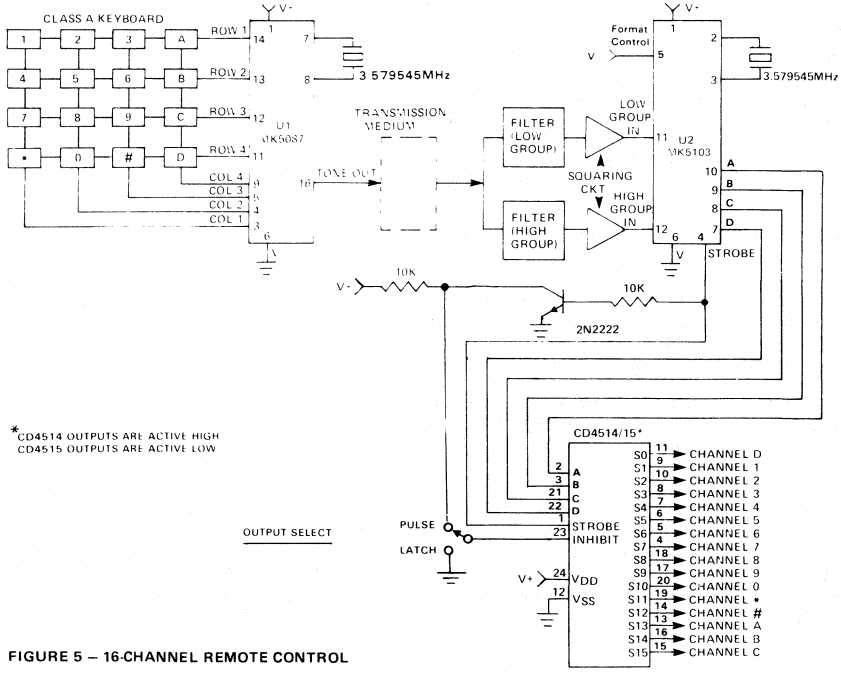


FIGURE 5 – 16-CHANNEL REMOTE CONTROL

MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V-) ..... 6.0 Volts
Operating Temperature ..... 0 C to 70 C
Storage Temperature ..... -55 C to 100 C
Maximum Circuit Power Dissipation 300mW
Voltage on any pin, with respect to V- ..... -0.3 Volt
Voltage on any pin, with respect to V+ ..... -0.3 Volt

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

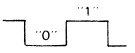
ELECTRICAL OPERATING CHARACTERISTICS

$0°C \leq T_A \leq 70°C$ V- **0 Volts**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V-)	(V- 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	47% - 53% Duty Cycle Rectangular Wave	0.9		V-	Volts Peak-to-Peak	1,2
STROBE, A, B, C, D OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V-)-1		V-	Volts @ 0.1 mA	
FORMAT CONTROL INPUT	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V-)-0.5		V-	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		30			ms	4
Interdigit Interval		35			ms	4
Signal-to-Noise Ratio		14			dB	3,5
Supply Current @ 5.5V	Inputs and Outputs Unloaded		2	5	mA	

NOTES:

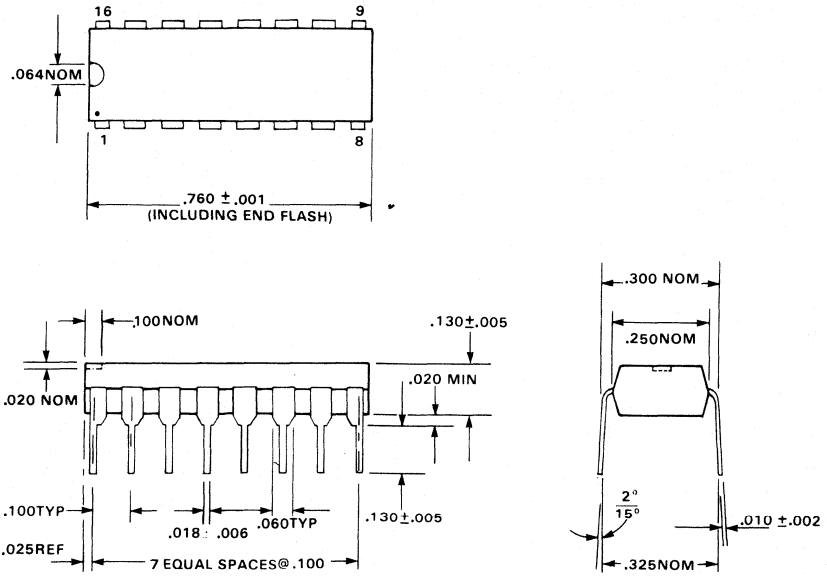
1. Due to internal biasing, this input must be capacitively coupled with a low-leakage 0.05 μF capacitor.
2. No coupling capacitor is needed if the DTMF rectangular wave meets the following criteria.



A. Logic "0" level 1 Volt (max)
B. Logic "1" level 4 Volts (min)

3. Signal-To-Noise Ratio is defined as:
   $SN \quad 20 \log \frac{SA}{NA}$
   where SA RMS Amplitude of single tone being detected.
   NA RMS white noise in the band from 300Hz to 3.4KHz.
4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.
5. Signal-To-Noise Ratio with 33db Filter Separation.

PHYSICAL DIMENSIONS



PLASTIC DIP
16-PIN

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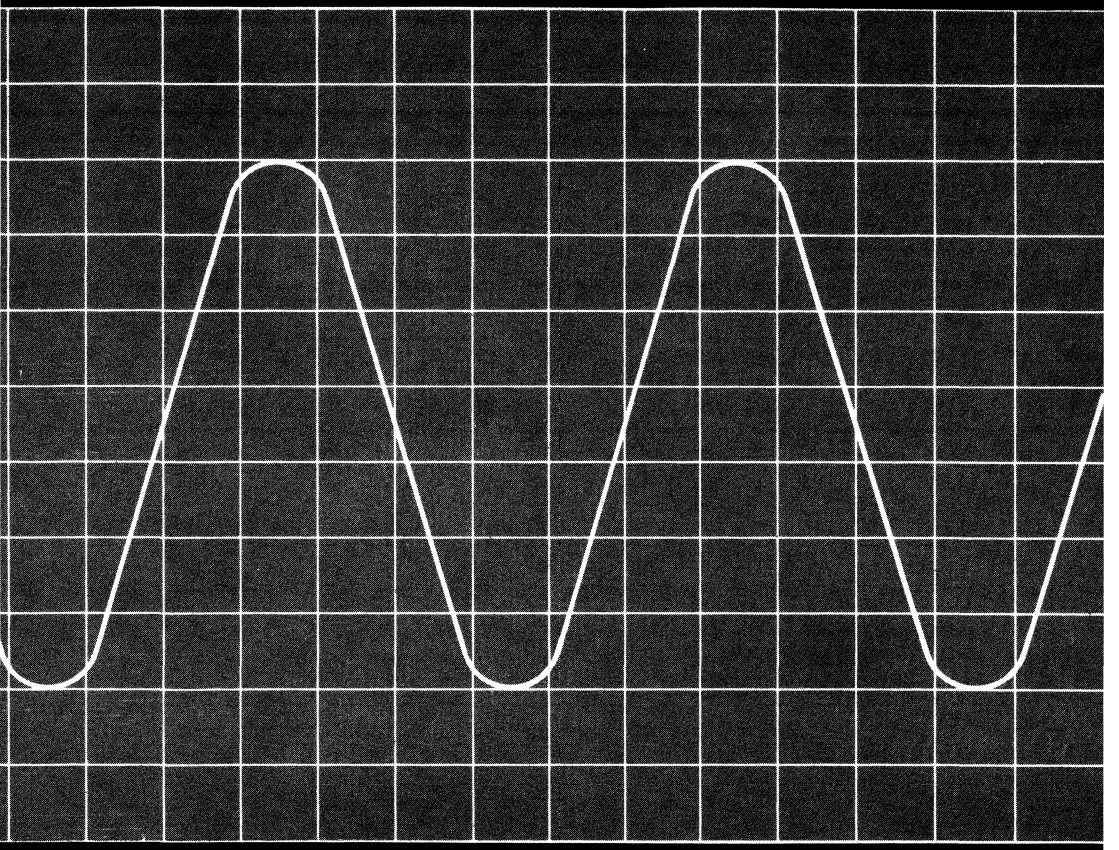
MK5102N-5
DTMF DECODER

APPLICATION NOTE AN-071



THOMSON
COMPONENTS
SEMICONDUCTEURS

SUMMARY

The MK5102N-5 provides a high-performance solution for DTMF detection at a lower cost than competing approaches. Band separation requirements for the MK5102N-5 are not as stringent as for competing designs, and, as was seen in the test results of Table 4 and Table 5, the MK5102N-5 provides excellent talk-off rejection. When used in conjunction with either the Cermetek or the North Electric filters, the MK5102N-5 will give the user a high-quality DTMF receiver which may be used in myriad applications.

APPLICATION

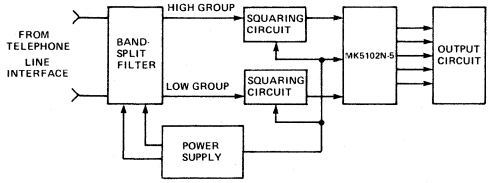
This application note will describe all of the requirements for building a high-quality DTMF receiver using the MK5102N-5 and hybrid filters. The following topics will be discussed:

1. Power supply requirements
2. Band separation filter requirements
3. Squaring circuit requirements
4. Squaring circuit-to-decoder coupling requirements
5. Receiver testing
6. Output formatting
7. Other system considerations

Since the MK5102N-5 is intended to be a portion of a tone receiver SYSTEM, SYSTEM requirements must be met before a satisfactory decoder can be constructed. A block diagram of a typical system is shown in Figure 1. Each portion of the block diagram is discussed in succeeding paragraphs.

TYPICAL DTMF RECEIVER

Figure 1



POWER SUPPLY REQUIREMENTS

For proper operation of the MK5102N-5, the V+ power supply must be between 4.5 VDC and 5.5 VDC, with V- grounded. A power supply decoupling capacitor (typically .1uF) should be connected between V+ and V- to insure that no high-frequency noise is present on the V+ supply. Typically, a 1-volt peak-to-peak signal may be applied to V+ and the MK5102N-5 will function properly.

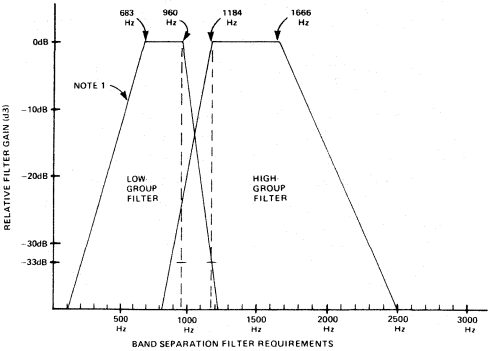
FILTER REQUIREMENTS

For proper operation of the MK5102N-5, an external band separation filter must be provided to split the DTMF signal into its high-group and low-group components. However, the band separation requirements are not as stringent for the MK5102N-5 as they are for competing designs. As shown in figure 2, the MK5102N-5 requires a band separation of only 33dB in an average application. The 33dB requirement allows for a S/N ratio of 18dB, 6dB of twist, and a detection bandwidth of at least ± 2%. A reduction of twist margin or S/N requirements will result in a corresponding lower requirement for band separation. For example, if there is not a requirement for twist margin, the band separation can be reduced to 27dB. In a system with no noise and no twist, the band separation can be 22dB.

The plot shown in Figure 2 depicts corner frequencies of 683Hz, 960Hz, 1184Hz and 1666Hz. These represent a 2% deviation from the DTMF frequencies of 697Hz, 941Hz, 1209Hz and 1633Hz, respectively. This deviation is necessary because of the requirement that a DTMF receiver must detect frequencies which are 2% higher or lower than the nominal DTMF frequency. Table 1 lists the 8 DTMF frequencies and the corresponding frequencies which a DTMF decoder is required to detect.

BAND SEPARATION FILTER REQUIREMENTS

Figure 2



NOTES:

1. Dial tone notch filter must maintain S/N ratio ⩾ 18dB
2. Filter response shown will allow operation to 6dB of twist with 18dB S/N.

TABLE I

8 STANDARD DTMF FREQUENCIES AND CORRESPONDING UPPER AND LOWER REQUIRED DETECTION FREQUENCIES

DTMF FREQUENCY (HZ)	LOWER DETECTION FREQUENCY LIMIT (HZ)	UPPER DETECTION FREQUENCY LIMIT (HZ)
697	683	711
770	755	786
852	834	869
941	922	960
1209	1184	1233
1336	1309	1363
1477	1447	1507
1633	1600	1666

DETECTION ALGORITHM

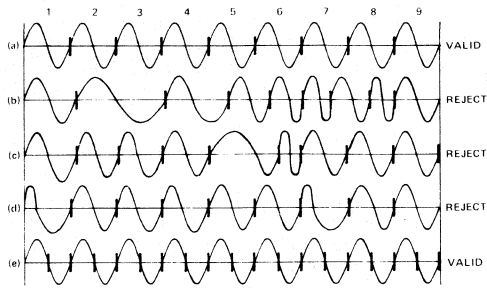
The detection approach used in the MK5102N-5 utilizes zero-crossing detection and digital period-counting. To increase the rejection of random noise and the residue from out-of-band components, an averaging scheme is used. Figure 3(a) shows nine cycles of a symmetrical sine wave. If zero-crossings were the only detection criteria, and if the average period-count obtained over nine periods were acceptable, then the signal in Figure 3(a) represents a valid tone. The jitter of the zero-crossings is integrated out by the nine-period average. However, based on the simple nine-period average, the signal shown in Figure 3(b) would be accepted as a valid tone. To improve rejection of this speech-type waveform, the nine-period detection time can be broken into three period-averaged sub-groups as indicated by the dashed lines in Figure 3(b). By combining the nine-period average and the sub-group average criteria, 200 false hits are obtained on 30 minutes of a standard speech tape. Figure 3(c) represents a type of waveform that would produce a hit based on the nine-period and sub-group average algorithm. To improve rejection of this waveform, requirements must be placed on every single period in addition to the nine-period average and the sub-group average. However, the waveform of Figure 3(d) will be detected using only these three criteria. Therefore an additional requirement must be placed on each half-period of the waveform. Figure 3(e) shows the only type of signal which will be accepted by a detection algorithm which requires the following:

1. Valid nine-period average
2. Three valid sub-group averages
3. Valid single-period
4. Valid half-period

Using these four criteria, the number of hits on a standard speech tape can be reduced to less than six.

POSSIBLE INPUT WAVEFORMS

Figure 3

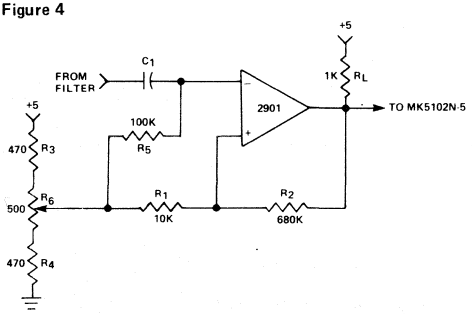


INPUT SQUARING CIRCUITS

As described above, to minimize the number of false hits, a detection algorithm must place stringent requirements on each half-period of the input waveform (high group or low group). To successfully meet these requirements, the duty cycle of the input waveform must be between 49% and 51%. The input squaring circuit must therefore provide an output which accurately tracks the input without adversely affecting the duty cycle. Such a circuit, an inverting comparator with hysteresis, is illustrated in Figure 4.

INPUT SQUARING CIRCUIT

Figure 4



C_1 is used to ac couple the filter output to the squaring circuit so that DC bias present at the filter output will not affect the performance of the squaring circuit. R_3, R_4, and R_6 establish a bias level at about 2.5 Volts, and R_5 is used to provide the same bias level at the inverting input of the comparator used in the squaring circuit. The maximum input bias current for the LM2901 is 500nA, so the DC bias level at the inverting input is effectively the same as the voltage at the wiper of R_6. R_6 must be adjusted so that, for an input signal level of -28dBm, the output duty cycle will be 50%. This adjustment compensates for

the input offset voltage of the LM2901. R_L is the pullup resistor for the open-collector output of the comparator. R_1 and R_2 set the hysteresis level. Their values are determined by the following approximate relationships:

$$V_{UT} = 2.5 + \frac{(2.5)(R_1)}{(R_1 + R_2 + R_L)}$$

where V_{UT} is the upper threshold

$$V_{LT} = \frac{(2.5 - V_{OL})(R_2)}{(R_1 + R_2)}$$

where V_{LT} is the lower threshold and V_{OL} is the output saturation voltage

In both cases, any variation due to the current in R_5 is ignored.

For central office applications, the tone receiver system must operate over an input signal level range of -26dBm to +6dBm. The squaring circuit, therefore, must respond to signal levels of -26dBm or greater but is not required to respond to lower signal levels.

To allow for signal attenuation through the band separation filter, the squaring circuit should be set to respond to signal levels of -28dBm or greater. The -28dBm cutoff point corresponds to a peak-to-peak voltage of 87.1mV. For a 50% duty cycle output waveform, V_{UT} should be set 43.5mV above and V_{LT} should be set 43.5mV below the DC bias point. The passive components for the squaring circuit are then selected as follows:

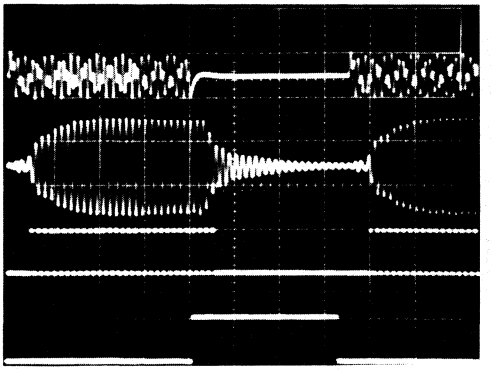
$R_L = 1k\Omega$	Chosen value.
$R_2 = 680k\Omega$	Chosen value.
$R_1 = 12k\Omega$	Calculated value.
$R_3 = R_4 = 470\Omega$	Chosen value for DC bias.
$R_5 = 100k\Omega$	Chosen value. Tradeoff effect on DC bias vs. drop across R_5 due to 2901 input bias current.
$C_1 = 1\mu F$	Chosen value. Must be low impedance over frequency range of 683Hz to 1666Hz.

To achieve proper operation at low signal levels, R_1 must be 10kΩ. The discrepancy between the calculated value and the actual required value results from component tolerances.

Since many commercially-available filters exhibit a ringing characteristic at their output, as shown in Figure 5 and Figure 6, additional circuitry is required to detect the beginning of ringing and squelch the output of the squaring circuit. The required circuitry, an envelope detector, is shown in Figure 7. The detector consists of two precision rectifiers, two sample-and-hold circuits, and a comparator. C_3 is used to couple the low-group filter output to the envelope detector. Z1a, D_1, C_1, R_2, and R_3 then rectify the incoming signal and store a peak value. The $R_2/R_3/C_1$ time constant is set for 20ms so that the voltage at the inverting input of Z_2 will represent ½ the peak value of the incoming signal. Z1b, D_2, R_1 and C_2 also rectify the incoming signal and store a peak value, but the time constant is set for 1.4ms so that the voltage at the non-inverting input of Z_2 will represent the instantaneous peak value of the incoming waveform. As long as the instantaneous value is greater than ½ of the peak value, the comparator output will be high. However, as soon as the instantaneous value decreases to less than ½ the peak value (this will occur as ringing begins), the comparator output will go low and inhibit the output of the squaring circuit. It is necessary to provide only one envelope detector since the MK5102N-5 will treat the absence of a valid low-group/high-group tone combination as interdigit time.

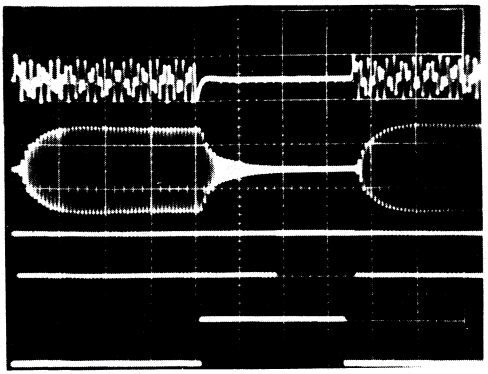
LOW-GROUP FILTER RESPONSE (3044)

Figure 5



EACH TIME DIVISION = 10 MS

HIGH–GROUP FILTER RESPONSE (3045)
Figure 6



EACH TIME DIVISION = 10 ms

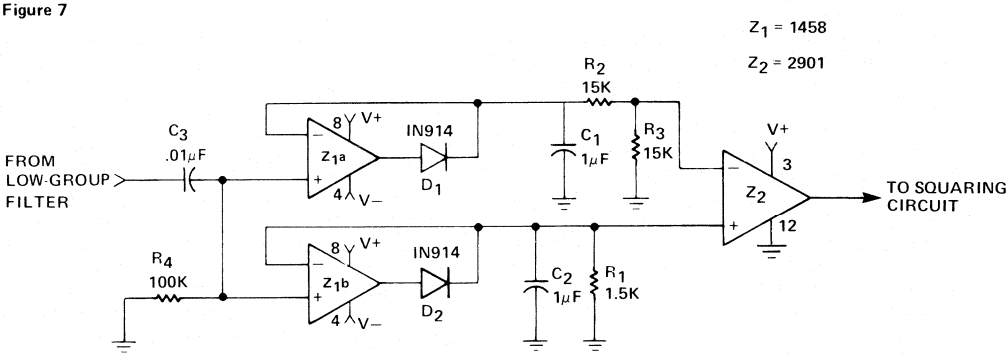
DTMF INPUT TO FILTER (5V/DIV.)

LOW-GROUP
FILTER OUTPUT (IV/DIV.)

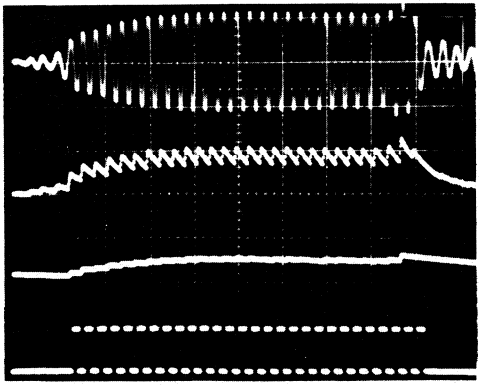
SQUARING CIRCUIT
OUTPUT (5V/DIV.)

STROBE FROM MK5102N-5
(5V/DIV.)

ENVELOPE DECAY DETECTOR
Figure 7



ENVELOPE DETECTOR OPERATION
Figure 8



LOW-GROUP
FILTER OUTPUT (IV/DIV.)

INSTANTANEOUS PEAK
DETECTOR (IV/DIV.)

AVERAGE PEAK
DETECTOR (IV/DIV.)

LOW-GROUP INPUT
TO 5102N-5 (5V/DIV.)

SQUARING CIRCUIT-TO-DECODER COUPLING

The output of the squaring circuit may be tied directly to the MK5102N-5 if it meets the following requirements:

Logic 1 ≥ 4 volts
Logic 0 ≤ 1 volt

A squaring circuit with an output that does not meet these requirements must be capacitively coupled to the MK5102N-5 with a 0.05μF capacitor. The value of the coupling capacitor is critical because of the impedance of the bias circuit at the high-group or low-group input. As shown in Figure 9, the sudden appearance of a tone burst causes the DC bias point to shift upward. Until the DC bias returns to its normal level, the input comparator will not switch and the input signal will be ignored, causing an increase in the dual-tone detection time. Using a 0.05μF capacitor will minimize the effect of this DC level shift.

SHIFT IN DC BIAS LEVEL CAUSED BY APPLICATION OF TONE BURST

Figure 9

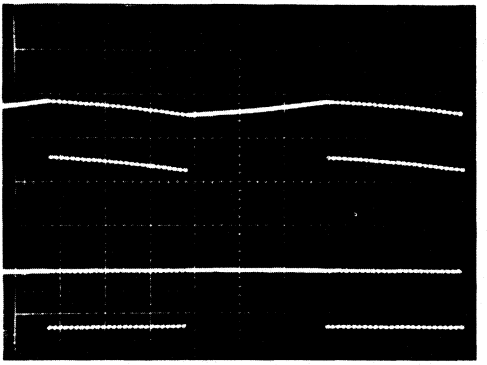


Table 3 describes the two output codes available.

TABLE 3

OUTPUT FORMAT

			4-Bit Binary				Dual 2-Bit Row/Column			
							Row		Column	
Key	Row	Col.	D1	D2	D3	D4	D1	D2	D3	D4
1	1	1	0	0	0	1	0	1	0	1
2	1	2	0	0	1	0	0	1	1	0
3	1	3	0	0	1	1	0	1	1	1
4	2	1	0	1	0	0	1	0	0	1
5	2	2	0	1	0	1	1	0	1	0
6	2	3	0	1	1	0	1	0	1	1
7	3	1	0	1	1	1	1	1	0	1
8	3	2	1	0	0	0	1	1	1	0
9	3	3	1	0	0	1	1	1	1	1
0	4	2	1	0	1	0	0	0	1	0
*	4	1	1	0	1	1	0	0	0	1
#	4	3	1	1	0	0	0	0	1	1
A	1	4	1	1	0	1	0	1	0	0
B	2	4	1	1	1	0	1	0	0	0
C	3	4	1	1	1	1	1	1	0	0
D	4	4	0	0	0	0	0	0	0	0

The peak-to-peak value of the coupled signal must be greater than .9 volts but less than V+ volts.

OUTPUT SIGNALS

D1, D2, D3, and D4 are the data output lines. The output format present on these pins is determined by the format control (pin 5) as shown in Table 2.

FORMAT CONTROL FUNCTIONS
TABLE 2

Format Control Input	Data Output Format
V−	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

When all detection criteria are present, the MK5102N-5 will latch the proper data into its outputs and strobe will go high. After an interdigit time has been detected, strobe will go low, but the data will remain on D1 through D4.

The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 10. On this circuit, the MK5102N-5, CD4556 and MK 5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK 5102N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.

TEST CIRCUIT FOR CERMETEK AND NORTH ELECTRIC FILTERS

Figure 13

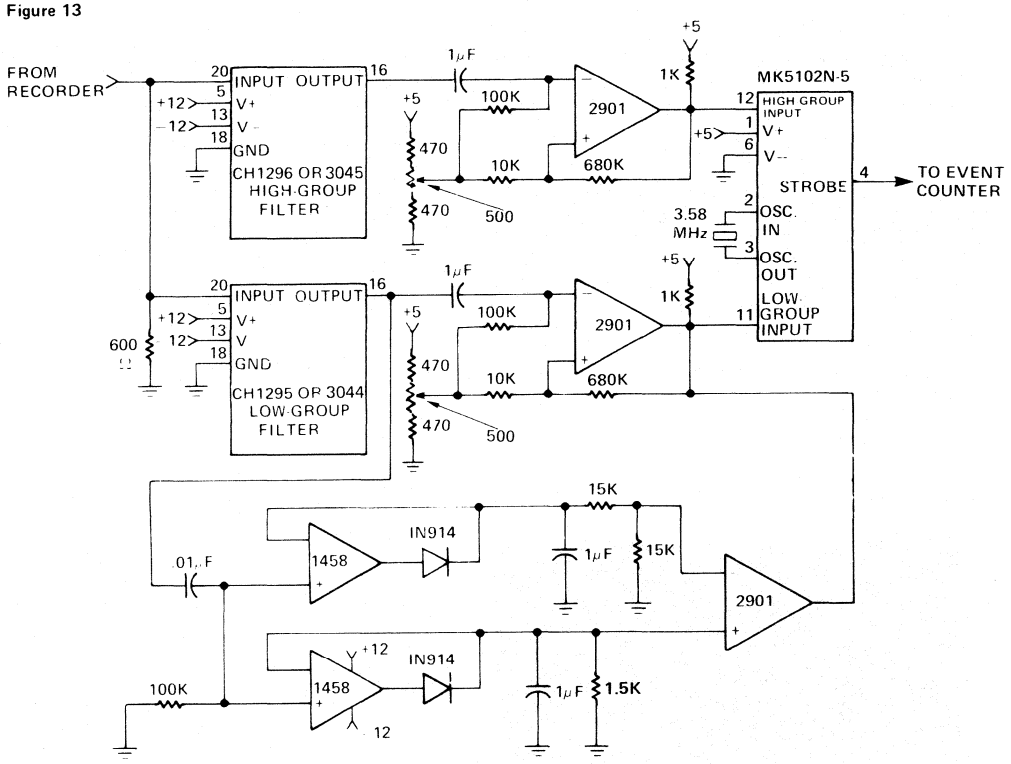


TABLE 4
MITEL TAPE TEST RESULTS FOR NORTH ELECTRIC FILTERS

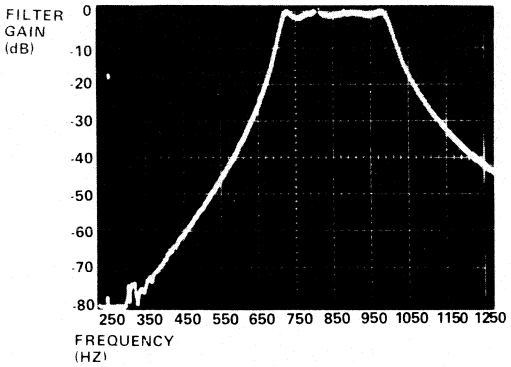
TEST #	RESULTS
2a, b	BW = 4.7 % of fo
2c, d	BW = 5.2 % of fo
2e, f	BW = 5.1 % of fo
2g, h	BW = 5.1 % of fo
2i, j	BW = 5.1 % of fo
2k, l	BW = 4.9 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 13.1dB
5	Dynamic Range = 31.33 dB
6	Guard Time = 34.23 ms
7	99.8 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

TABLE 5
MITEL TAPE TEST RESULTS FOR CERMETEK FILTERS

TEST #	RESULTS
2a, b	BW = 5.6 % of fo
2c, d	BW = 5.7 % of fo
2e, f	BW = 5.0 % of fo
2g, h	BW = 5.3 % of fo
2i, j	BW = 5.2 % of fo
2k, l	BW = 5.0 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	158 decodes
4	Acceptable Amplitude Ratio = 12.6dB
5	Dynamic Range = 31.67 dB
6	Guard Time = 33.4 ms
7	98.33 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

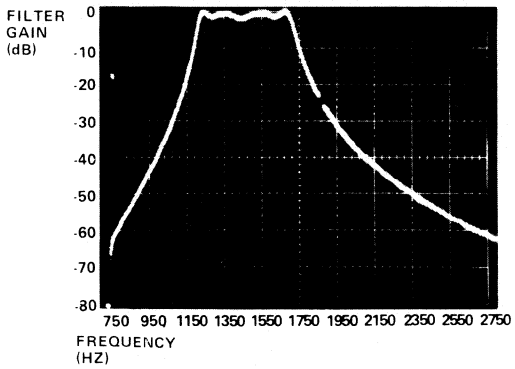
SPECTRAL RESPONSE OF CH1295 LOW-GROUP FILTER

Figure 14



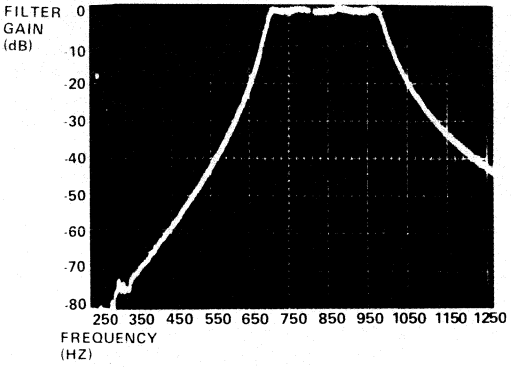
SPECTRAL RESPONSE OF CH1296 HIGH-GROUP FILTER

Figure 15



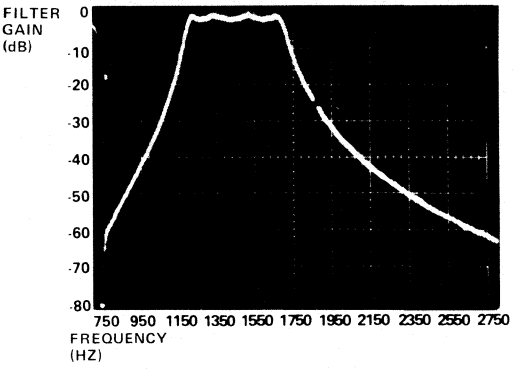
SPECTRAL RESPONSE OF 3044 LOW-GROUP FILTER

Figure 16



SPECTRAL RESPONSE OF 3045 HIGH-GROUP FILTER

Figure 17



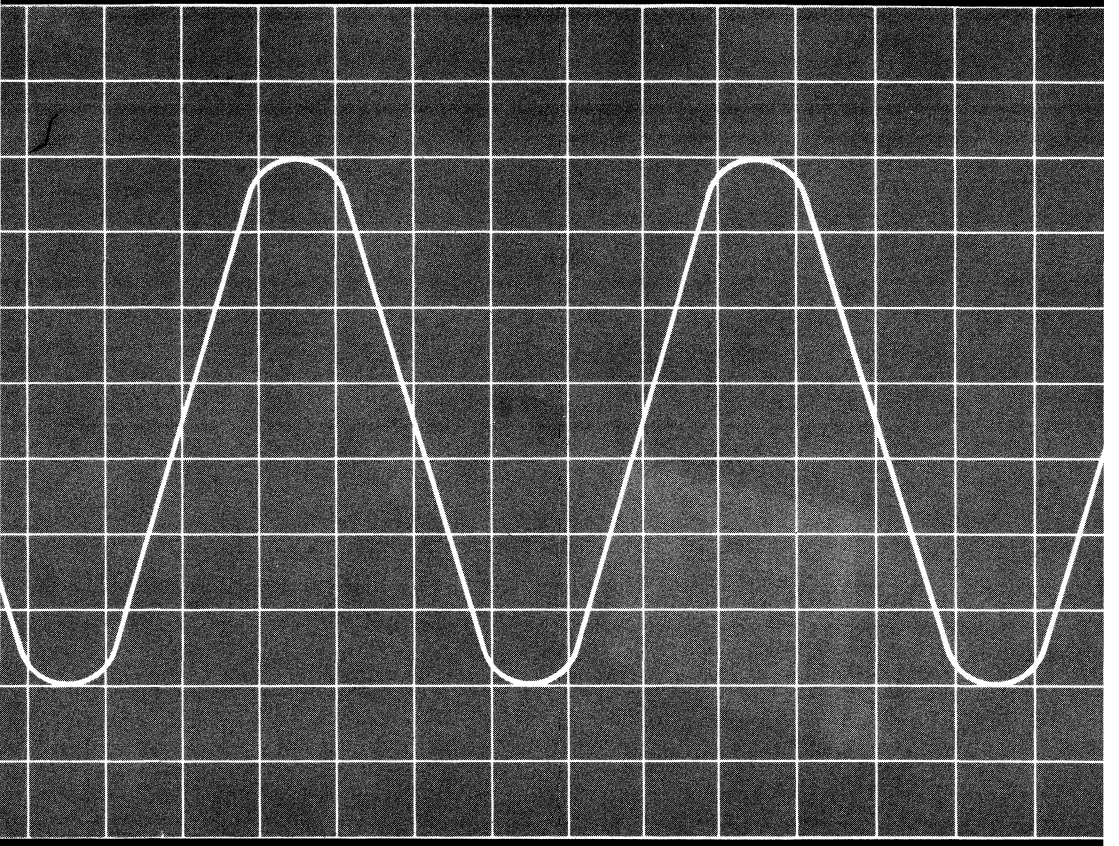
OTHER SYSTEM CONSIDERATIONS

System noise will affect the operation of the MK5102N-5 by causing the detection bandwidth to shrink. The instantaneous value of the low-group or high-group waveform is represented by the following approximate relationship, $a = a_T \sin w_T t + a_N \sin w_N t$, where a is the instantaneous amplitude of the overall waveform, a_T is the amplitude of the high-group or low-group component, and a_N is the amplitude of the noise. If the highly-simplified noise term ($a_N \sin w_N t$) were removed, then the remaining term would represent a pure sine wave and the zero crossings of the waveform would be repeatable from cycle to cycle. All detection criteria would be present and the DTMF tone would be detected within a ± 2.0% to ± 2.9% bandwidth. However, adding the noise term introduces instantaneous amplitude variations which will effectively alter the duty cycle of the sine wave by causing the zero crossing points to jitter. If 0.5% jitter is caused by system noise, detection bandwidth will be decreased by .5%. Therefore, as the system noise level increases, the detection bandwidth will decrease.

As noted in the Filter Requirements paragraph, the 33dB band separation requirement allows for a S/N ratio of 18dB, with 6dB of twist, which means that the algorithm in the MK5102N-5 has been set up to provide a ± 2% minimum detection bandwidth in the presence of noise which is 18dB below the signal level and in the presence of high-group and low-group signals with an amplitude difference of 6dB.

MK5371/72 and MK5375/76
TYPICAL APPLICATIONS FOR MULTIPHONE

APPLICATION NOTE AN-078



THOMSON
COMPONENTS
SEMICONDUCTEURS

The Mostek Pulse Tone dialer circuits (MK5371, MK5372, MK5375, MK5376) provide a cost effective method for accomplishing both DTMF (Tone) and Loop Disconnect (Pulse) dialing using the same keypad and telephone-line interface circuitry. The MK5371 and MK5372 feature 28-digit redial with Hookflash, Pause, and Mode Softswitch (switches between Pulse and Tone modes via the keyboard as well as the Mode switch). The MK5375 and MK5376 are 10 number (16-digits each) repertory Pulse Tone switchable dialers with variable tone and pulse dialing rates (RC determined). The 24-pin MK5372 and MK5376 also feature Make/Break ratio selection of 40/60 or 32/68, 10 20 PPS pulse dialing rate selection (MK5372), RC Hookflash timing (MK5372), and 12 13 key operation (MK5376). This application circuit is designed to accommodate any of the above mentioned parts, utilizing a configuration header and an overlapping 16/24 pin footprint (MK5371 & 5375-16 pins, MK5372 & 5376-24 pins).

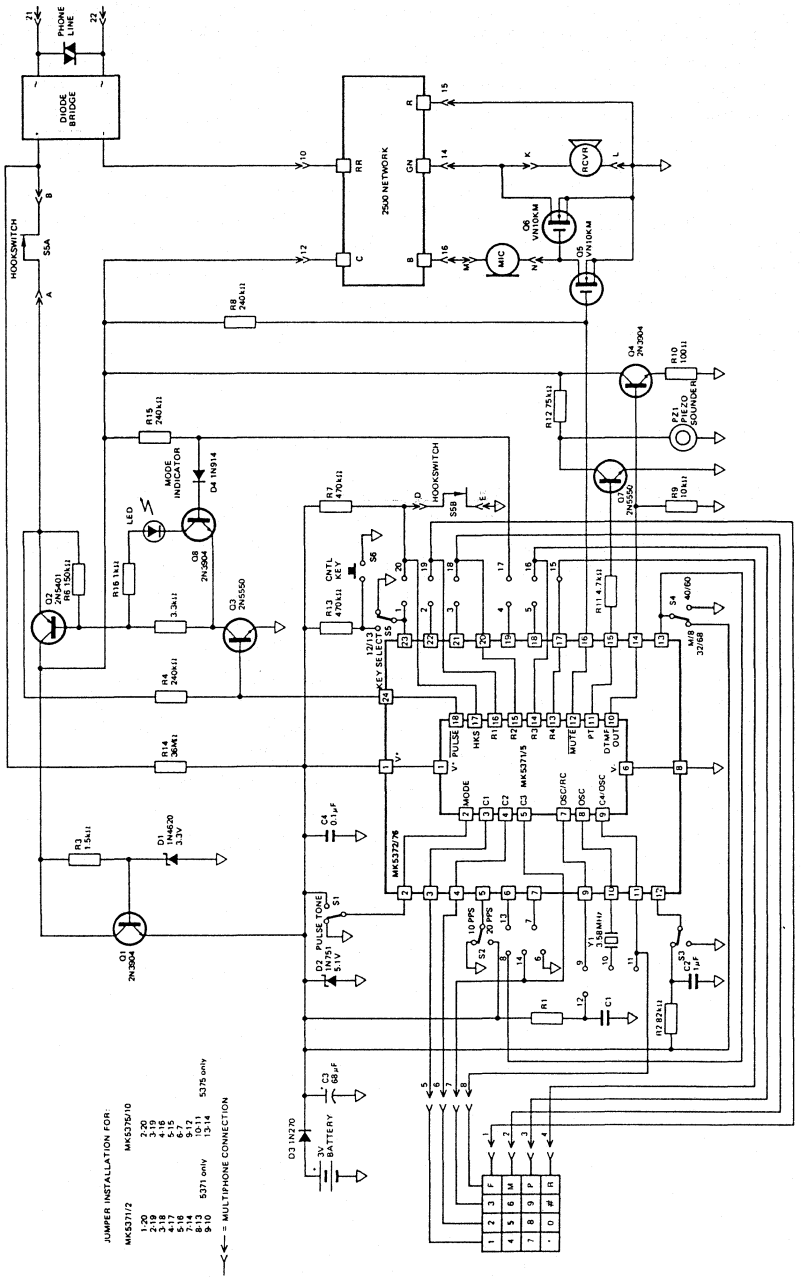
In loop-disconnect signalling, each digit dialed consists of a series of momentary interruptions or breaks of telephone loop current (i.e., a digit "1" consists of one break, a "2" of two breaks, and so on up to a digit "0" which consists of 10 breaks). The Pulse output of the dialer is dedicated to loop-disconnect signalling and controls the flow of loop current through the speech network using transistors Q2 and Q3. The Mute output drives transistors Q5 and Q6 to mute the receiver and transmitter to eliminate loud pops caused by the switching of current through the speech network.

DTMF signalling requires that the telephone loop current be modulated with the appropriate dual tone signal corresponding to the digit dialed. The DTMF Out pin drives the base of transistor Q4 to modulate the loop current through resistor R10. The Mute output removes the transmitter and shunts the receiver by switching transistors Q5 and Q6. This eliminates any interference with the DTMF signal from the transmitter and lowers the amplitude of the DTMF tone heard at the receiver.

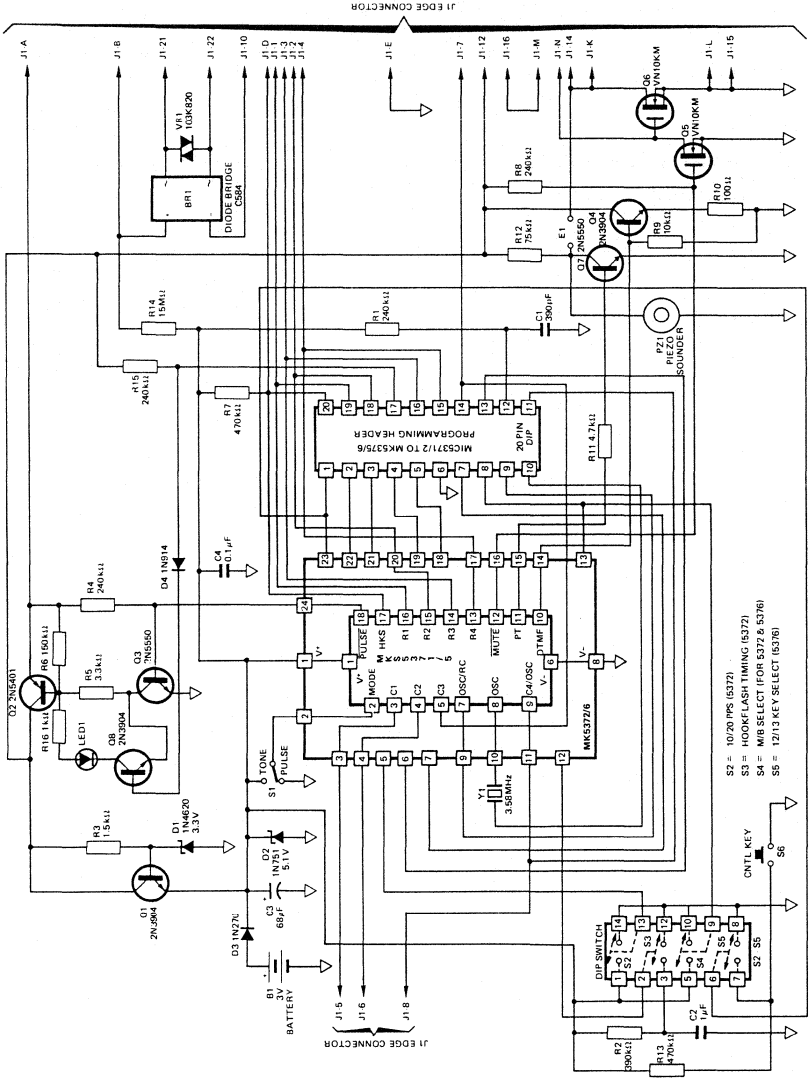
The voltage regulator circuit comprised of resistor R3, zener diode D1, and transistor Q6 provides a regulated supply to the dialer in both Tone and Pulse modes, and helps provide some isolation from the transients caused by pulsing when in the Pulse mode. During normal off-hook operation the dialer derives its power from the telephone line. When on-hook, the small amount of current required to retain memory (200 nA typical) is supplied through resistor R14. However, a 3 volt lithium battery is used for the MK5375/6 on-hook storage of numbers, and the assurance of long term retention of its 10 number memory (regardless of phone line disconnections). Under normal usage this battery should last from 7 to 10 years.

Please consult the device data sheets for further information.

MK5371/72 AND MK5375/76 APPLICATION FOR THE MULTIPHONE

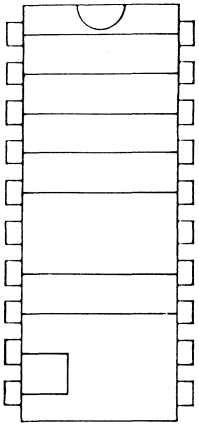


MK5371/72/75/76 MULTIPHONE CIRCUIT SHEMATIC

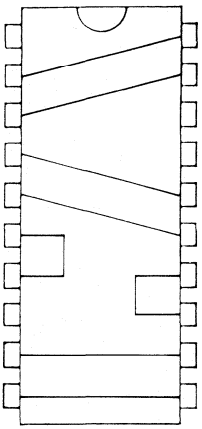


MK5371/75 MULTIPHONE BOARD
CONFIGURATION HEADERS

MK5370/71/72



MK5375/76

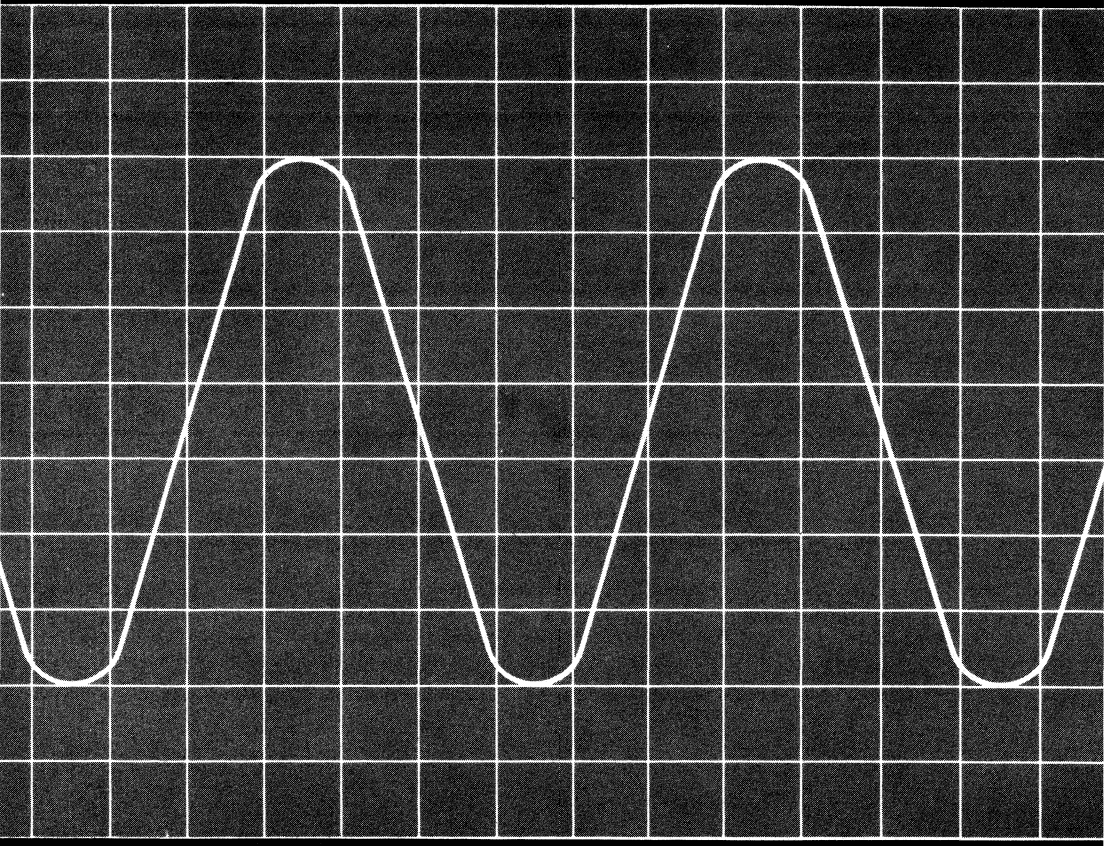


Note :
The MK5372 and MK5376 require the use of different 20-pin configuration headers. By inserting the propery labeled header in the 20-pin socket, the demo board can be configured for the MK5370/71/72 or for the MK5375. 76. The 20-pin headers are individually labeled for MK5371/72 (also 5370) or MK5375/76.

For MK5370/71/72 the S5 (12/13 Key select) DIP switch should be set to the 13 Key position for proper circuit operation.

MK5375 TYPICAL APPLICATIONS NO BATTERY BACK-UP & CONTINUOUS TONE

APPLICATION NOTE AN-079



THOMSON
COMPONENTS
SEMICONDUCTEURS

The MK5375 is a very versatile Tone/Pulse dialer product which can be used in a wide variety of applications. There are however two applications questions which arise very frequently.

1) Is a battery necessary for memory retention and on-hook storage operations ?
2) Is it possible to make the MK5375 generate a continuous tone for the length of a key depression ?

This application not will discuss how an MK5375 application circuit can be designed to operate without a battery for storage operations and memory retention, as well as generate a continuous tone for the length of the key closure.

The MK5375 was designed so that normal dialing and auto-dialing could take place while off hook, and programming operations would take place while on-hook. This, as well as long term memory retention, typically requires a battery, wich is objectionable to some telephone circuit manufacturers. There are however methods for accomplishing off-hook programming by placing the MK5375 in its on-hook mode (HKS, pin 17, to V−) while the telephone circuit is still off hook and drawing telephone line current. The minimal memory retention current required by the MK5375 (200 nA typ.) can also be supplied from the telephone line through a very large resistor, and with a large capacitor to maintain the memory for the time that the telephone may be disconnected.

In the application circuit shown in Figure 1, a Program/Normal switch (S4) is used to place the MK5375 in the "Program" mode by taking HKS (pin 17) to V − (pin 1), to allow for programming numbers into the 9 memory locations while off-hook. The Pacifier Tone/Chip Disable input/output (pin 11) is connected to hookswitch S2 (through load resistor R4) so that the MK5375 will be disabled (pin 11 to V −) when on hook. This is done so that the memory will not be lost due to the increased current consumption of trying to program with the limited on-hook current supply. In this application circuit, memory retention current is supplied from the telephone line through a diode bridge (to insure correct polarity) and a 15 M Ω resistor, with a 5.1 V zener diode (Z2) to limit the voltage across the MK5375. A 100 μF capacitor is used to maintain the MK5375 memory during any small amounts of time (30 minutes typ.) that the telephone may be disconnected. Therefore, by adding a switch and a resistor, and increasing the value of a capacitor, the need for a battery can be eliminated.

An importante feature of the MK5375 is that all of timing pulse dialing and tone output rate is controlled by an RC oscillator whose values may be varied to achieve a wide variety of signalling rates. It is this RC oscillator that determines the lengh and interdigit time for each output tone burst. Therefore to achieve a continuous tone, the RC oscillator must be stopped while that tone is being output. The tone will then remain until the RC oscillator is allowed to continue running and complete the burst time. The solution to getting a continuous tone for the lengh of a key closure requires some method of stopping the RC oscillator for the duration of the key closure, one the key entry has been debounced and decoded.

In the Figure 2 application circuit, a single transistor circuit (Q7, R14, R15, & C3) is used to stop the RC oscillator once a key entry has been debounced, decoded, and the output tone burst has begun. A keyboard with a common connection is used because whenever a row is connected to a column, that node is pulled low through the MK5375 keyboard input circuitry, so that the keyboard common will be normally open and go low when any key is pressed. Once a key entry has been debounced and decoded, the DTMF output will go high (to a DC level about which the output signal will be generated), thus turning on transistor Q7 and pulling the RC oscillator input (pin 7) low through the keyboard common. This will stop the RC oscillator,

which will cause the DTMF signal to remain until the key is released. When the key is released, the keyboard common will be open and the RC oscillator will resume running until the remainder of the tone burst time is completed. Since the RC determined tone burst time (100 ms using standard values) is added on to the time that the key is held low after debounce, the RC period must be decreased to allow for rapid key entry. To do this, an extra resistor (R13) is added in parallel to R1, and another pole of Mode Switch S1 is used to revert to the standard RC values for the nominal 10 PPS pulse dialing rate.

Aside from the minor circuit additions discussed, both application circuits, are standard MK5375 Tone/Pulse switchable, 10-number repertory dialer circuits. Both circuits are telephone line powered, using a diode bridge to insure proper line polarity, and a voltage regulator circuit comprised of transistor Q6, resistor R2, and zener diode Z1. The rate at which dialing occurs is determined by the values of resistor R1 and capacitor C1, which are the timing components for the RC oscillator. The 3.5795 MHz crystal is used as a reference for synthesizing the DTMF signals and is activated only for the short periods during which these tones are being generated.

Pulse dialing (which consists of a series of momentary interruptions of loop current) is achieved by the Pulse output controlling transistors Q4 and Q5 to break and make the loop current through the speech network. The Mute output, controlling transistors Q2 and Q3, mutes the transmitter and receiver to eliminate the loud pops which would otherwise be heard in the receiver due to the pulsing of the loop current through the speech network.

Tone signalling requires that the loop current be modulated with the appropriate DTMF signal. The DTMF output of the MK5375 drives transistor Q1 to modulate the telephone loop current through resistor R5. The signal level present at the telephone line can be varied by changing the value of R5. The Mute output controls transistors Q2 and Q3 to remove the transmitter and mute the receiver. This is done to eliminated any interference of the DTMF signal from the transmitter, and to reduce the level of tone heard at the receiver.

The two application circuits discussed in this application note are examples of just a few ways in which the MK5375 Tone/Pulse Repertory Dialer may be used to meet a wide variety of requirements. For additional applications information and further details on the operation of the MK5375 and its specifications, please consult the MK5375 data sheet.

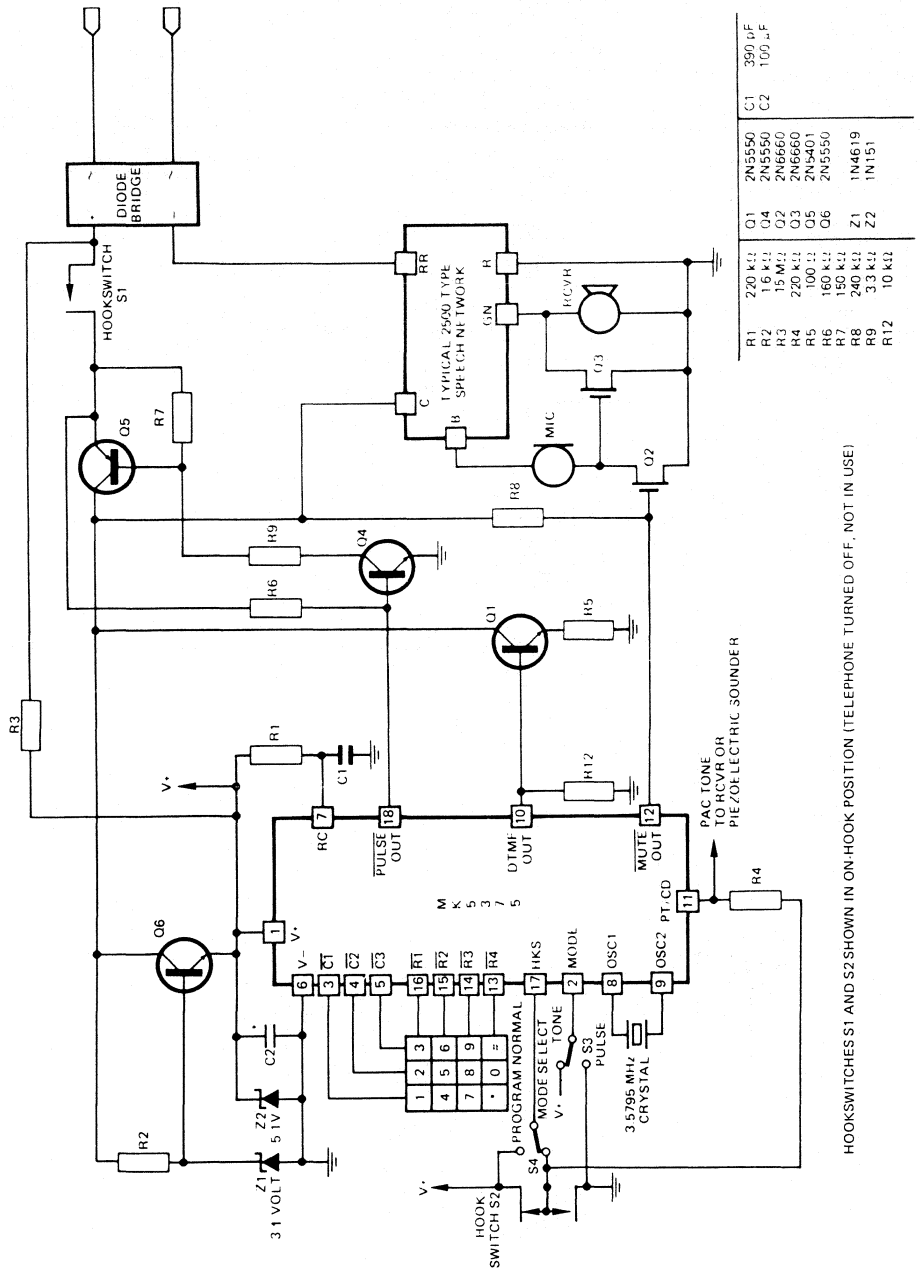
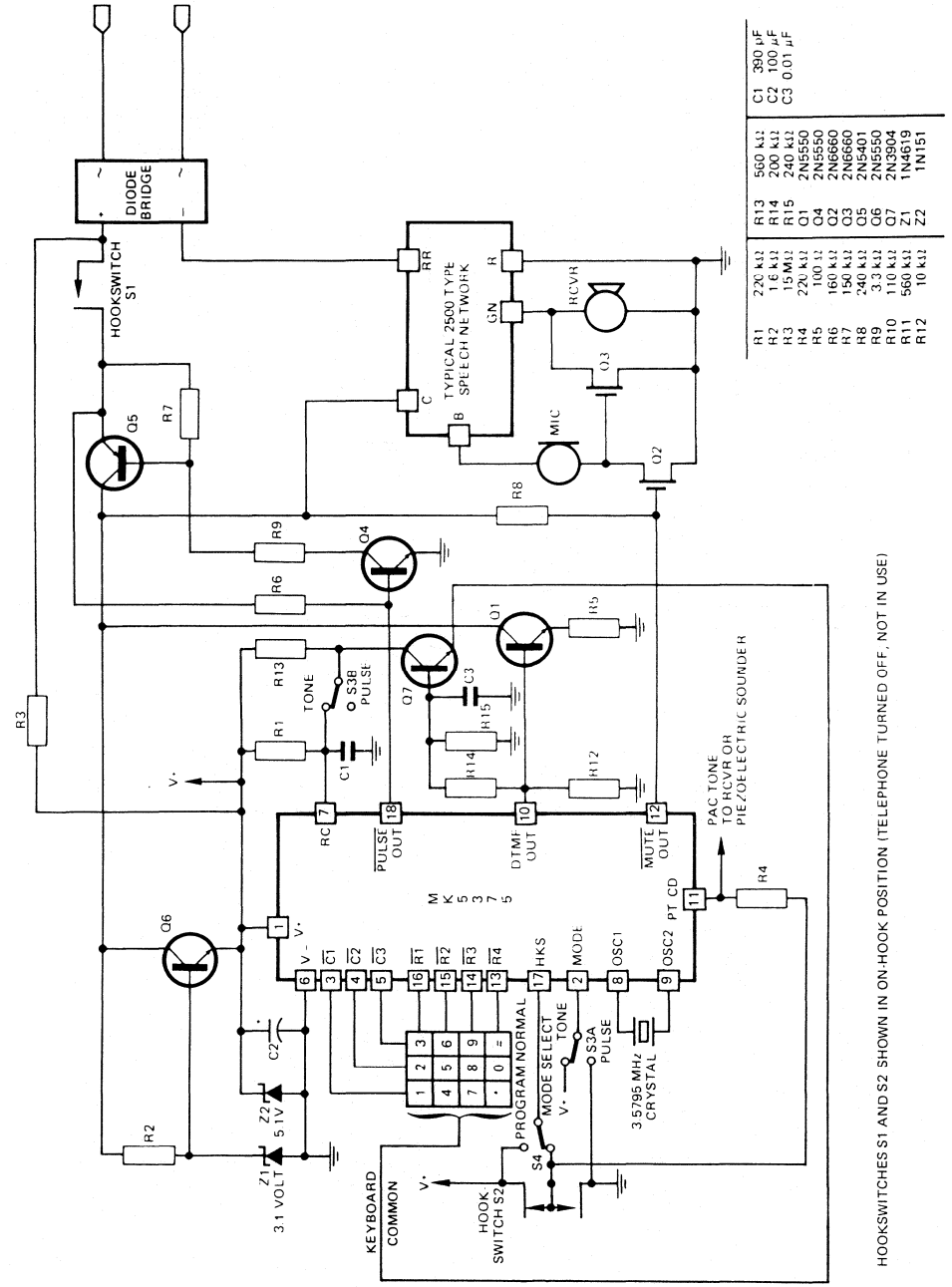


FIGURE 1 – MK5375 TYPICAL APPLICATION – WIHTOUT BATTERY BACK-UP

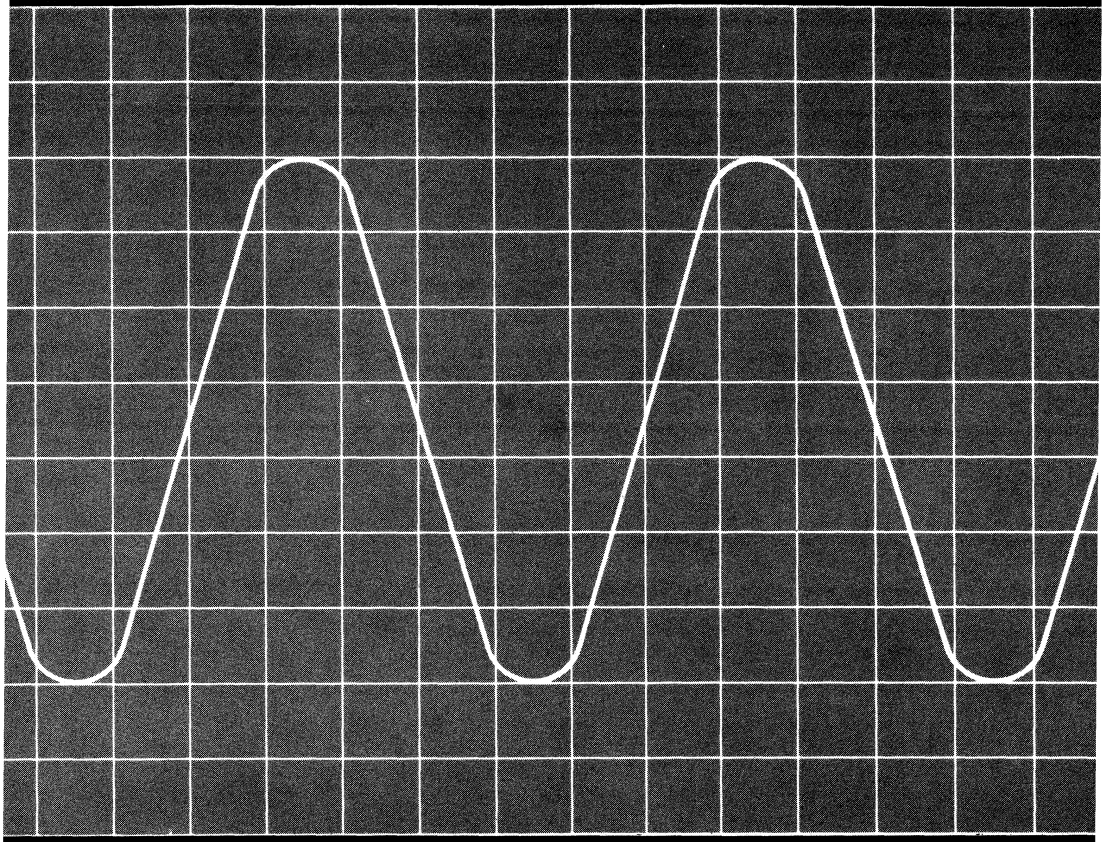


R1	220 kΩ	R13	560 kΩ	C1	390 µF
R2	1.6 kΩ	R14	200 kΩ	C2	100 µF
R3	15 MΩ	R15	240 kΩ	C3	0.01 µF
R4	220 kΩ	Q1	2N5550		
R5	100 Ω	Q2	2N5550		
R6	160 kΩ	Q3	2N6660		
R7	150 kΩ	Q4	2N6660		
R8	240 kΩ	Q5	2N5401		
R9	3.3 kΩ	Q6	2N5550		
R10	110 kΩ	Q7	2N3904		
R11	560 kΩ	Z1	1N4619		
R12	10 kΩ	Z2	1N151		

FIGURE 2 – MK5375 TYPICAL APPLICATION – CONTINUOUS TONE

MK5376
TYPICAL APPLICATIONS

APPLICATION NOTE AN-080



THOMSON
COMPONENTS
SEMICONDUCTEURS

The MK5376 is a very versatile Tone/Pulse dialer product which can be used in a wide variety of applications. A common application of the MK5376 is shown in Figure 1. In this application, the MK5376 uses a Control Key for autodialing and programming, so that the * and # keys operate as normal DTMF signalling digit. Also, a 3 volt battery is used for memory retention and on-hook programming operations. There are however two questions concerning the application of the MK5376 which arise frequently.

1) Is a battery necessary for memory retention and on-hook storage operations ?
2) Is it possible to make the MK5376 generate a continuous tone for the length of a key depression ?

This application not will discuss how an MK5376 application circuit can be designed to operate without a battery for storage operations and memory retention, as well as generate a continuous tone for the length of the key closure.

The MK5376 was designed so that normal dialing and auto-dialing could take place while off hook, and programming operations would take place while on-hook. This, as well as long term memory retention, typically requires a battery. wich is objectionable to some telephone circuit manufacturers. There are however methods for accomplishing off-hook programming by placing the MK5376 in its on-hook mode (HKS, pin 22, to V−) while the telephone circuit is still off hook and drawing telephone line current. The minimal memory retention current required by the MK5376 (200 nA typ.) can also be supplied from the telephone line through a very large resistor, and with a large capacitor to maintain the memory for the time that the telephone may be disconnected.

In the application circuit shown in Figure 2, a Program/Normal switch (S4) is used to place the MK5376 in the "Program" mode by taking HKS (pin 22) to V − (pin 1), to allow for programming numbers into the 9 memory locations while off-hook. The Pacifier Tone/Chip Disable input/output (pin 15) is connected to hookswitch S2 (through load resistor R4) so that the MK5376 will be disabled (pin 15 to V −) when on hook. This is done so that the memory will not be lost due to the increased current consumption of trying to program with the limited on-hook current supply. In this application circuit, memory retention current is supplied from the telephone line through a diode bridge (to insure correct polarity) and a 15 M Ω resistor, with a 5.1 V zener diode (Z2) to limit the voltage across the MK5376. A 220 μP capacitor is used to maintain the MK5376 memory during any small amounts of time (30 minutes typ.) that the telephone may be disconnected. Therefore, by adding a switch and a resistor, and increasing the value of a capacitor, the need for a battery can be eliminated.

An important feature of the MK5376 is that all of timing pulse dialing and tone output rate is controlled by an RC oscillator whose values may be varied to achieve a wide variety of signalling rates. It is this RC oscillator that determines the lengh and interdigit time for each output tone burst. Therefore to achieve a continuous tone, the RC oscillator must be stopped while that tone is being output. The tone will then remain until the RC oscillator is allowed to continue running and complete the burst time. The solution to getting a continuous tone for the lengh of a key closure requires some method of stopping the RC oscillator for the duration of the key closure, one the key entry has been debounced an decoded.

In the Figure 3 application circuit, a single transistor circuit (Q7, R14, R15, & C3) is used to stop the RC oscillator once a key entry has been debounced, decoded, and the output tone burst has begun. A keyboard with a common connection is used because whenever a row is connected to a column, that node is pulled low through the MK5376 keyboard input circuitry,

so that the keyboard common will be normally open and go low when any key is pressed. Once a key entry has been debounced and decoded, the DTMF output will go high (to a DC level about which the output signal will be generated), thus turning on transistor Q7 and pulling the RC oscillator input (pin 9) low through the keyboard common. This will stop the RC oscillator, which will cause the DTMF signal to remain until the key is released. When the key is released, the keyboard common will be open and the RC oscillator will resume running until the remainder of the tone burst time is completed. Since the RC determined tone burst time (100 ms using standard values) is added on to the time that the key is held low after debounce, the RC period must be decreased to allow for rapid key entry. To do this, an extra resistor (R13) is added in parallel to R1, and another pole of Mode Switch S1 is used to revert to the standard RC values for the nominal 10 PPS pulse dialing rate.

Aside from the minor circuit additions discussed, all application circuits are standard MK5376 Tone/Pulse switchable, 10-number repertory dialer circuits. These circuits are telephone line powered, using a diode bridge to insure proper line polarity, and a voltage regulator circuit comprised of transistor Q6, resistor R2, and zener diode Z1. The rate at which dialing occurs is determined by the values of resistor R1 and capacitor C1, which are the timing components for the RC oscillator. The 3.5795 MHz crystal is used as a reference for synthesizing the DTMF signals and is activated only for the short periods during which these tones are being generated.

Pulse dialing (which consists of a series of momentary interruptions of loop current) is achieved by the Pulse output controlling transistors Q4 and Q5 to break and make the loop current through the speech network. The Mute output, controlling transistors Q2 and Q3, mutes the transmitter and receiver to eliminate the loud pops which would otherwise be heard in the receiver due to the pulsing of the loop current through the speech network.

Tone signalling requires that the loop current modulated with the appropriate DTMF signal. The DTMF output of the MK5376 drives transistor Q1 to modulate the telephone loop current be through resistor R5. The signal level present at the telephone line can be varied by changing the value of R5. The Mute output controls transistors Q2 and Q3 to remove the transmitter and mute the receiver. This is done to eliminated any interference of the DTMF signal from the transmitter, and to reduce the level of tone heard at the receiver.

The application circuits discussed in this application note are examples of just a few ways in which the MK5376 Tone/Pulse Repertory Dialer may be used to meet a wide variety of requirements. For additional applications information and further details on the operation of the MK5376 and its specifications, please consult the MK5376 data sheet.

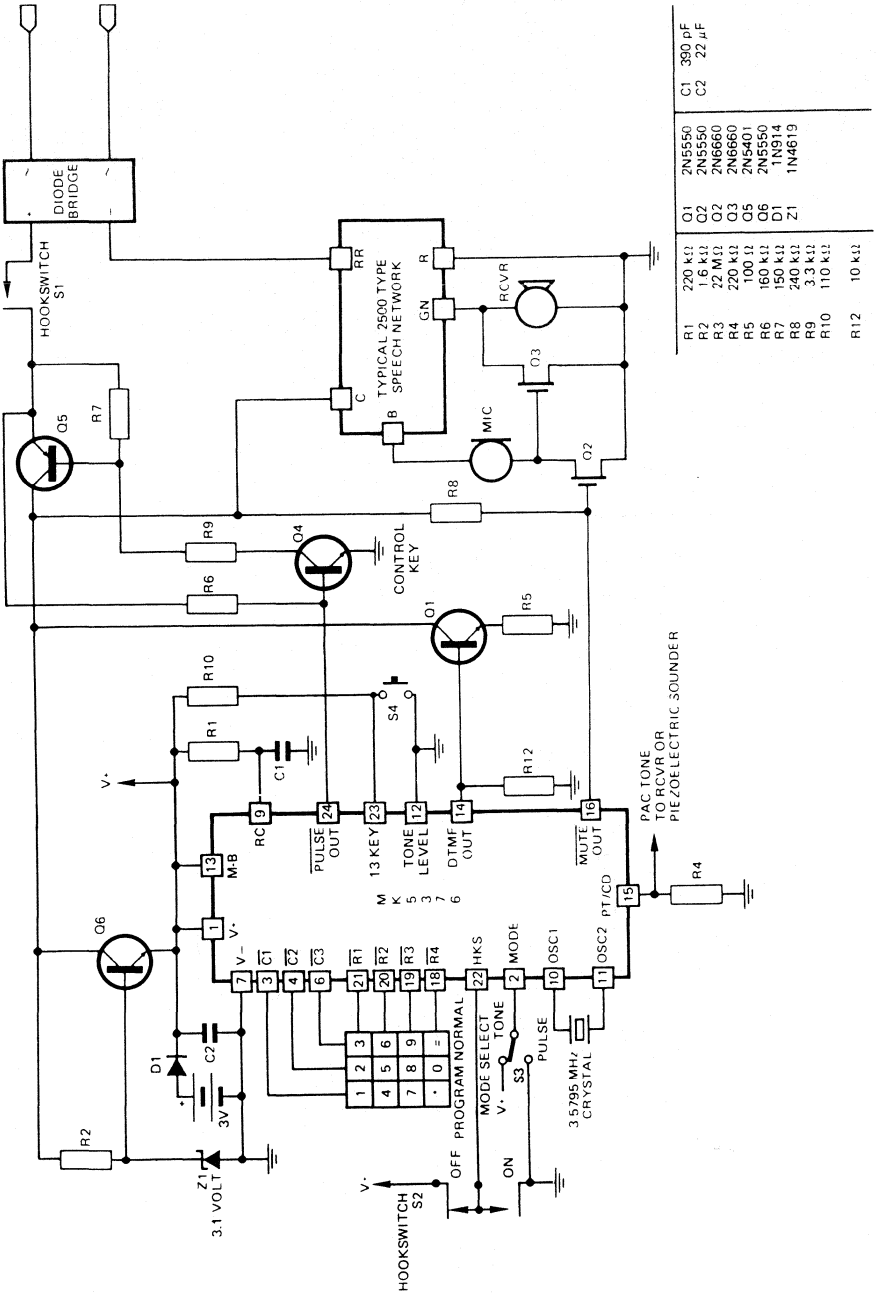


FIGURE 1 – MK5376 TYPICAL APPLICATION

USING CONTROL KEY FOR AUTODIALING AND PROGRAMING FUNCTIONS

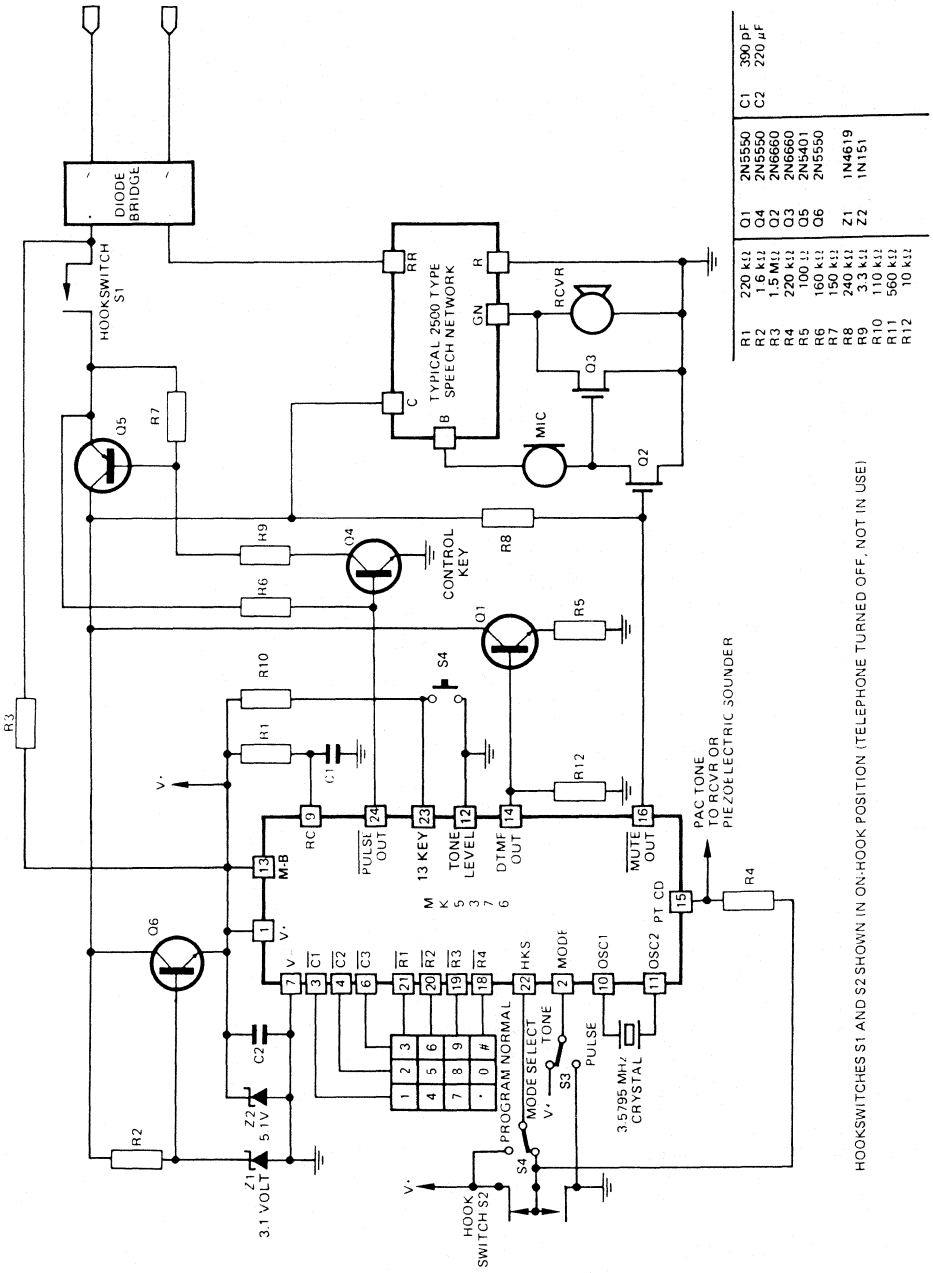
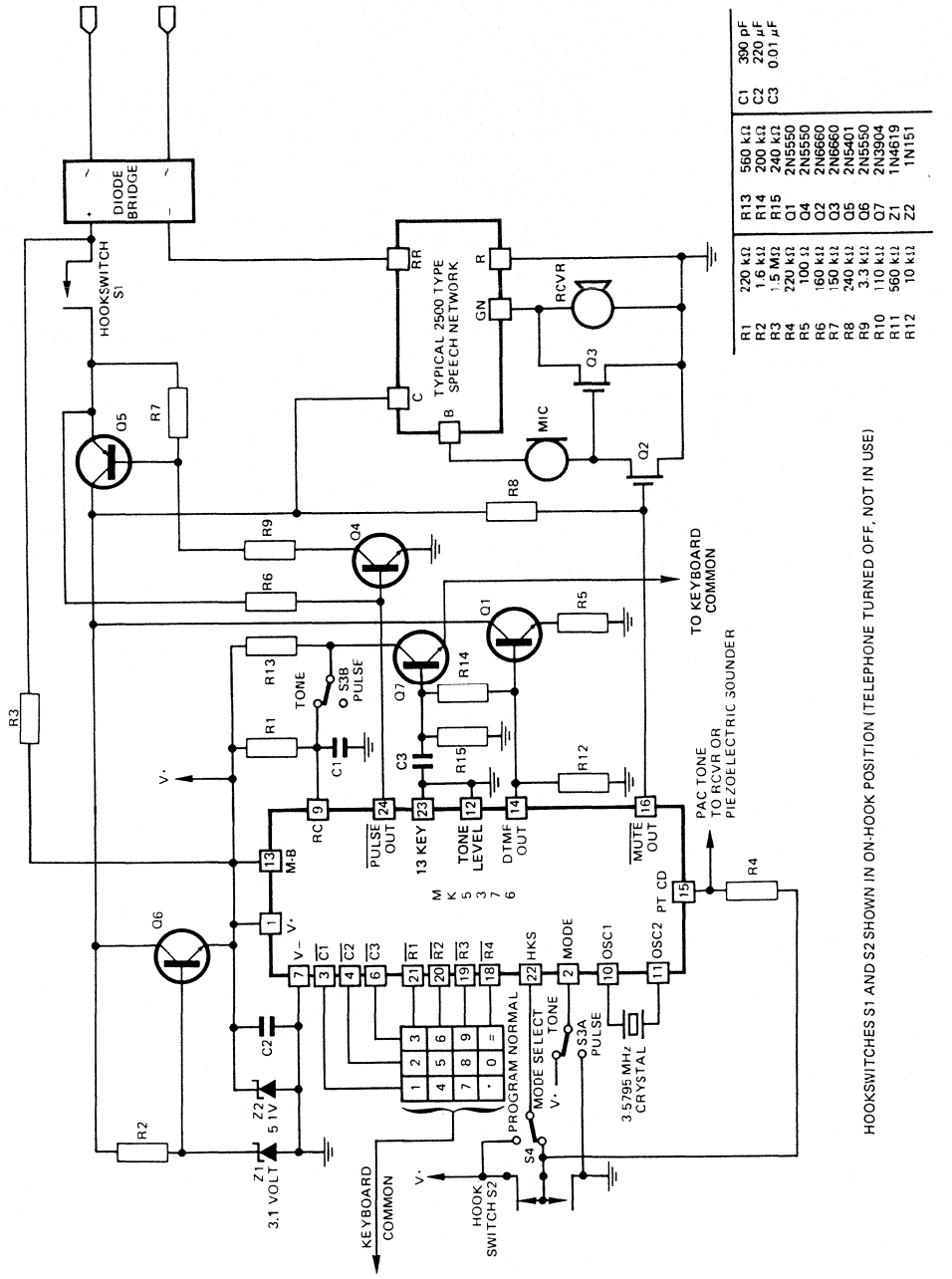


FIGURE 2 – MK5376 TYPICAL APPLICATION – WIHTOUT BATTERY BACK-UP



R1	220 kΩ	R13	560 kΩ	C1	390 pF
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R3	1.5 MΩ	R15	240 kΩ	C3	0.01 µF
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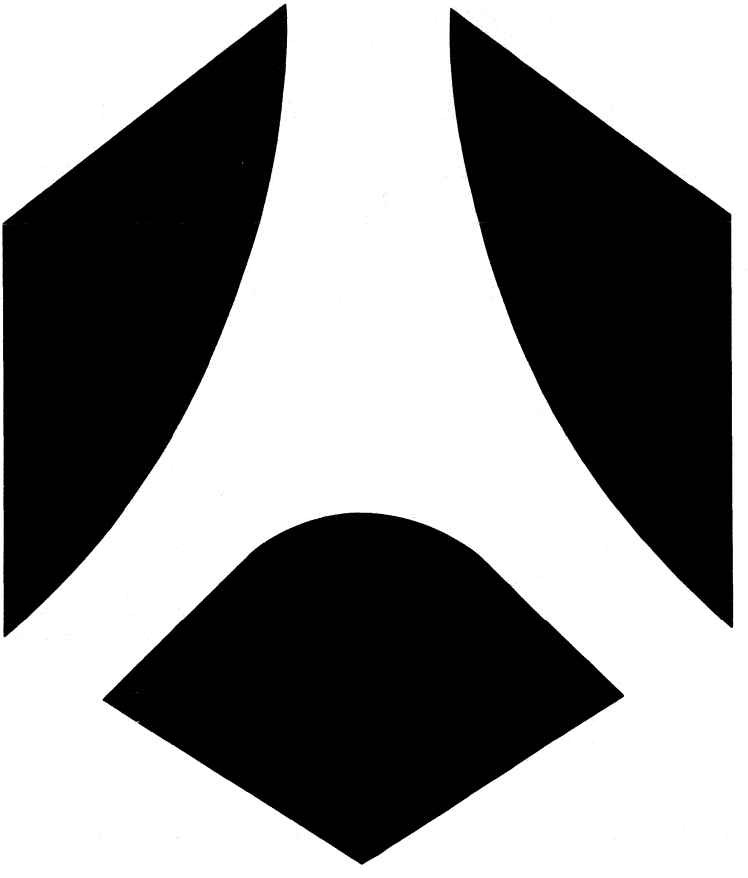
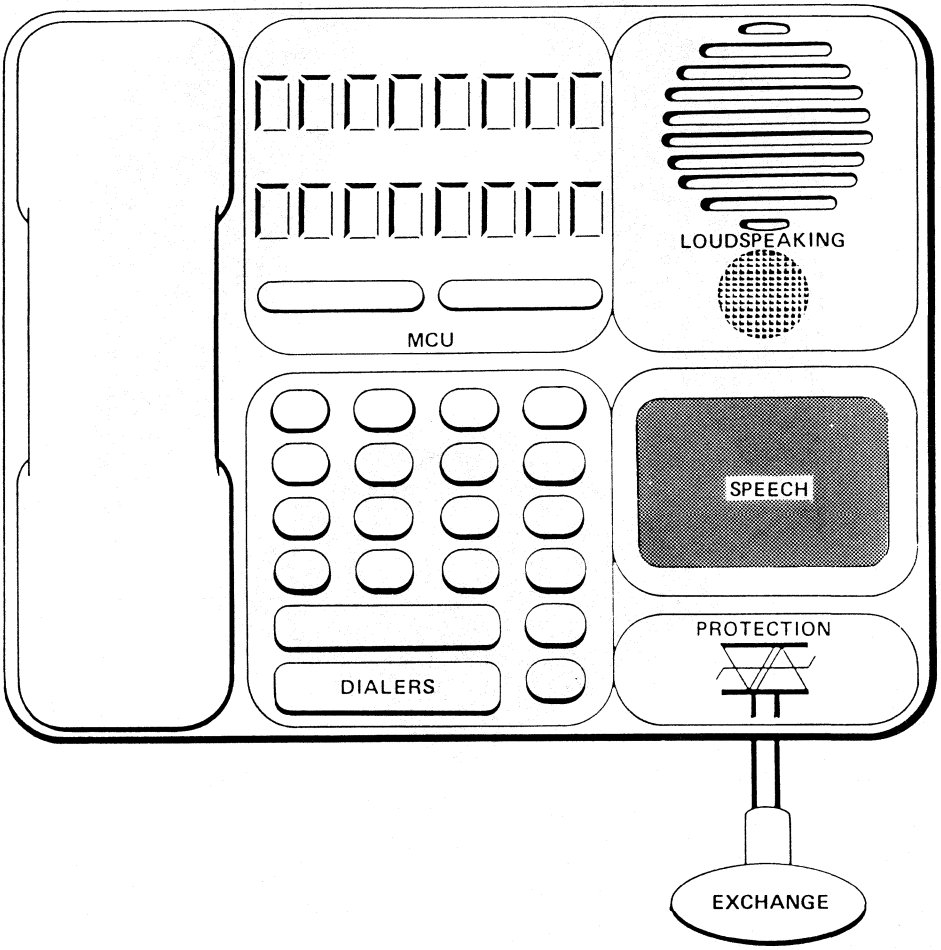
R11	560 kΩ	Z1	1N4619		
R12	10 kΩ	Z2	1N151		

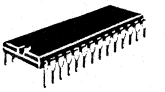
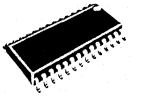
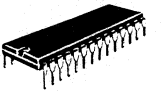
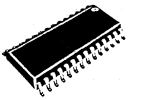
FIGURE 3 – MK5376 TYPICAL APPLICATION
WITH CONTINUOUS TONE AND NO BATTERY BACK-UP



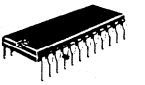
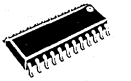
Speech ICs


LOUDSPEAKING
MCU
SPEECH
PROTECTION
DIALERS
EXCHANGE

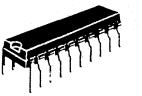
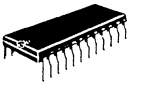
SPEECH AND TONE

Function	Part number	Characteristic		Package	Page
Telephone monochip	TEA3046	Transmission, line adaptation, DTMF generation and power supply for peripheral circuits. Interface is also possible with a microcomputer.	DIL 28		2-5
	TEA7047		SO 28		2-19
Telephone set transmission and DTMF generation circuit	TEA7037	Transmission, voice frequency power stabilization and microprocessor reset functions.	DIL 28		2-39
			SO 28		

SPEECH

Function	Part number	Characteristic		Package	Page
Speech for high range telephone sets	TEA7050	Transmission, line adaptation, power supply for peripherals and loudspeaker. Interface with a microcomputer.	DIL 24		2-63
			SO 24		

ISDN COMBO

Function	Part number	Characteristic		Package	Page
Digital telephone CODEC/filter	TS7650	A-law and μ-law (software selectable) serial interface CODEC/filter, interface for handset and handfree, ring and tone generation. Serial MCU interface.	DIL 20		2-69
			DIL 24		

TEA3046

SPEECH AND TONE

Specially designed for a basic telephone set application this 28 pin IC provides:

- Transmission and line adaptation,
- DTMF generation,
- Power supply for peripherals,
- Interface with MCU.

Major advantages

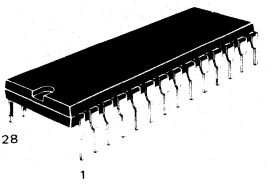
- Adjustable automatic line length receiving and sending gain control.
- Adjustable automatic line length tracking antisidetone system.
- Adjustable microphone and earphone amplifier gain.
- Adjustable dynamic impedance.

Other advantages

- Microphone amplifier compatible with symmetrical and asymmetrical inputs.
- Click-free switch over from speech to dialling mode & vice-versa.
- Silent position facility.
- Single tone facility.
- Two keys roll over provided.
- Switch bounce elimination.
- Adjustable output tone level.
- Temperature independent output level.
- Separated emission and reception mute.

BIPOLAR

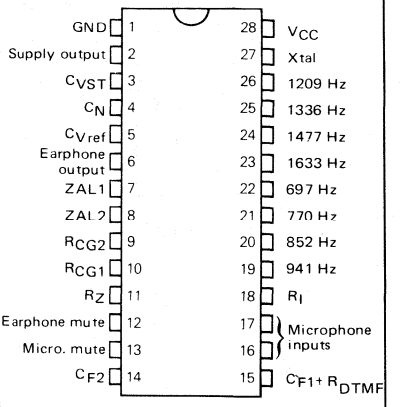
CASE
CB-132



DP SUFFIX
PLASTIC PACKAGE

Also available in SO package
(FP SUFFIX)

PIN ASSIGNMENT



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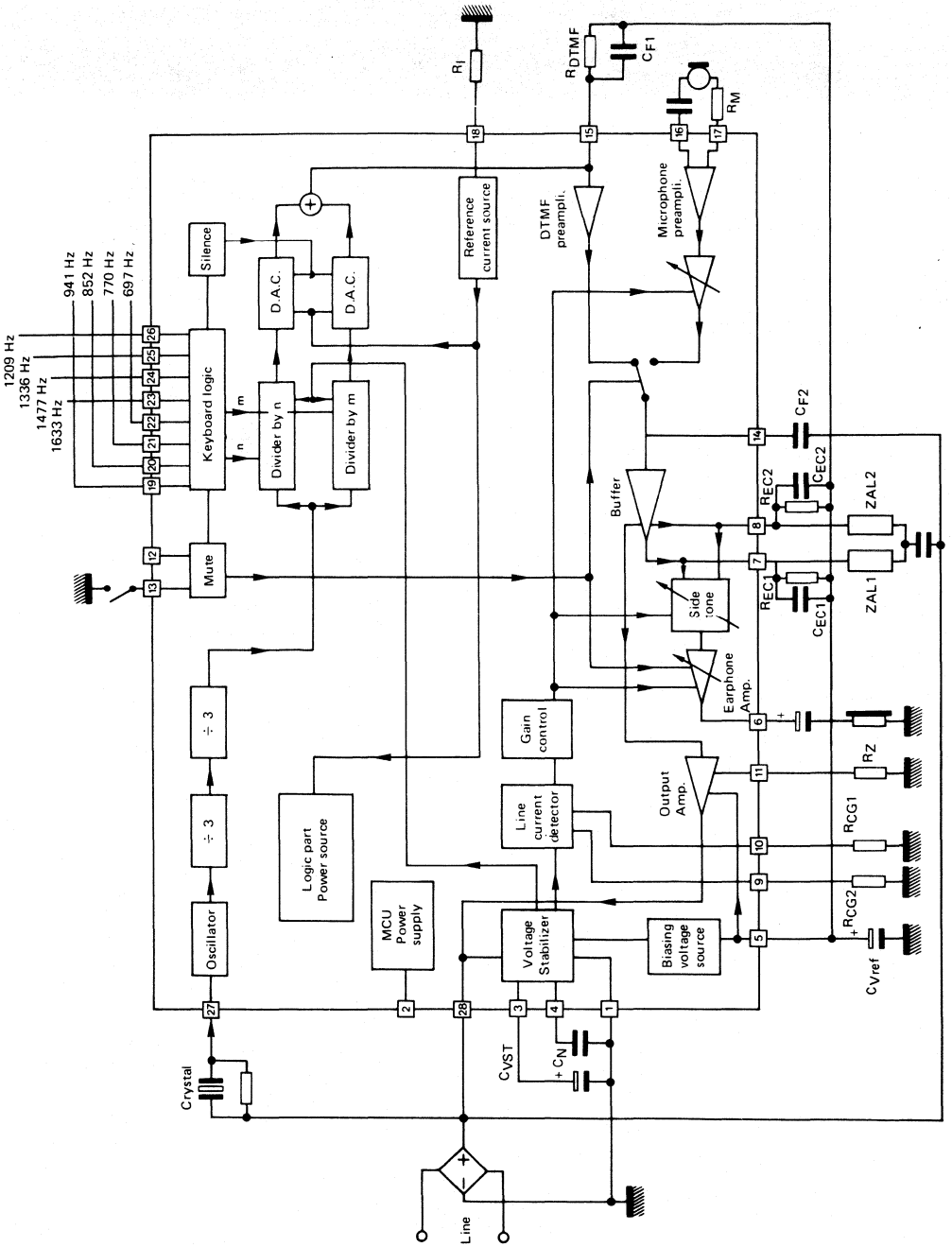
BLOCK DIAGRAM



PIN DESCRIPTION

Name	No	Description
G_{ND}	1	Ground
Supply output	2	Power supply output
C_{VST}	3	C_{VST} decouples the voltage stabilizer
C_N	4	Capacitor to reduce the noise
C_{Vref}	5	C_{Vref} decouples the biasing voltage. This reference biasing voltage is temperature independant.
Earphone output	6	Earphone amplifier output
Z_{AL1}	7	Short line antisidetone circuit Z_{AL1} and earphone amplifier input.
Z_{AL2}	8	Long line antisidetone circuit Z_{AL2} and earphone amplifier input.
R_{CG2}	9	R_{CG2} fixes gain control (see note 4).
R_{CG1}	10	R_{CG1} fixes gain control (see note 4).
R_Z	11	R_Z fixes the impedance value of the circuit.
Earphone mute	12	A short circuit to the ground on this pin mutes the earphone signal.
Micro mute	13	A short circuit to the ground on this pin mutes the microphone signal.
C_{F2}	14	C_{F2} filters both microphone and DTMF signals.
$C_{F1} + R_{DTMF}$	15	C_{F1} and R_{DTMF} filter the DTMF signal & set DTMF signal level..
Microphone inputs	16-17	
R_I	18	$V_{ref.}$ voltage on this pin is temperature stable.
941 Hz	19	"D" logic input. 941 Hz keyboard row.
852 Hz	20	"C" logic input. 852 Hz keyboard row.
770 Hz	21	"B" logic input. 770 Hz keyboard row.
697 Hz	22	"A" logic input. 697 Hz keyboard row.
1633 Hz	23	"H" logic input. 1633 Hz keyboard column.
1477 Hz	24	"G" logic input. 1477 Hz keyboard column.
1336 Hz	25	"F" logic input. 1336 Hz keyboard column.
1209 Hz	26	"E" logic input, 1209 Hz keyboard column.
X_{tal}	27	Oscillator input
V_{CC}	28	Supply voltage

FUNCTIONAL DESCRIPTION

TRANSMISSION AND LINE ADAPTATION

Includes microphone and telephone amplification, both with line length depending gain control and a line impedance automatic matching 2-wire to 4-wire conversion.

The microphone preamplifier performs high CMRR, and low noise characteristic. Its architecture allows symmetrical and asymmetrical inputs and external adjustment of gain to fit difference microphone capsules. A single pole filter limits the amplifier bandwidth for a best high frequency figure.

The earphone amplifier is a low consumption type. It is click free when muted and its gain can be externally adjusted.

2-wire to 4-wire conversion is performed by subtracting microphone signal from line before applying it to earphone amplifier. An automatic line impedance tracking antisidetone circuit provides excellent sidetone efficiency for every line length.

The dynamic impedance of the circuit is set by an external resistor to match with different line impedances.

The line length is sensed through the line current. 2 external components allow the gain control to compensate any kind of line length and feeding bridge.

DTMF SIGNAL GENERATION

Tones are obtained from a crystal controlled oscillator followed by two independent programmable dividers and 2 sinewave synthetizers. The crystal is a low-cost TV model 3.58 MHz oscillator.

The amplitude of the multi-frequency signal is set by an external resistor.
The required tone frequencies are selected by either an inexpensive single contact 4 x 4 keypad or by a microcomputer. Single-tone operation for testing is also provided.

THE POWER SUPPLY

This is 0.6 mA current source with a typ max voltage compliance of a 3.2 V.
It can power either and electret microphone or a microprocessor.
If this source is not used, pin 2 is connected to ground to reduce the ICC (pin 28) current.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	— 0.7 to 9	V
Power dissipation	P_{tot}	1.2	W
Operating temperature range	T_{oper}	– 25 to 65	°C
Storage temperature range	T_{stg}	– 55 to 150	°C
Line current (pin 28)	I_L	180	mA
Surge line current (pin 28)	I_L surge	850	mA

STATIC ELECTRICAL CHARACTERISTICS

$-25°C \leq T_{amb} \leq +65°C$
Line impedance $Z_L = 600\ \Omega$

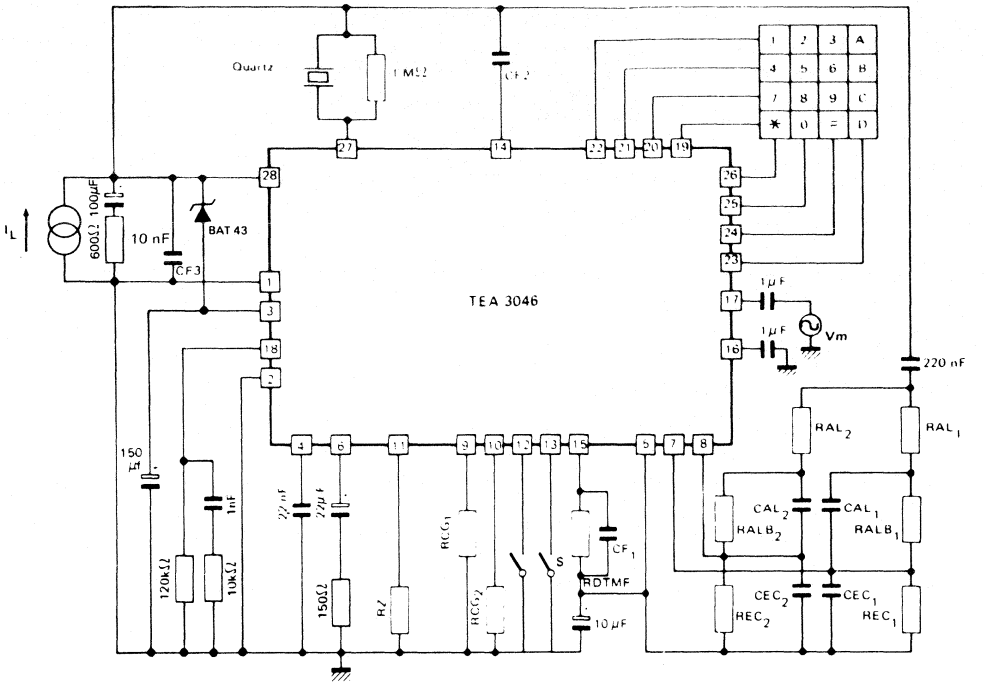
Characteristic	Symbol	Min	Typ	Max	Unit
Line current (pin 28)	–	–	–	–	mA
MPU supply OFF (pin 2 → GND)	I_L	15	–	150	–
MPU supply ON	I_L	17	–	150	–
Voltage over the I_C (pin 28)	–	–	–	–	V
I_L = 15 mA	V28	3.9	4.6	5.1	–
I_L = 100 mA	V28	–	–	7	–
Voltage stabilizer (pin 3)	–	–	–	–	V
I_L = 15 mA	V_C	–	2.7	–	–
I_L = 100 mA	V_C	–	3.7	–	–
Power supply (pin 2) max current (V2 = 3.2 V)	–	–	–	–	mA
Sending mode V28 = 5dBm	I2	0.6	–	–	–
Without A_C line signal	I2	1	1.2	–	–

DYNAMIC ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C
Line impedance Z_L = 600 Ω
F = 1 kHz

Characteristic	Symbol	Min	Typ	Max	Unit
Max sending gain R_M = 0 (No gain control action note 1)	– G_S max	– 49.5	– 50.5	– 51.5	 dB
Gain control Sending gain decrease (Note 1)	–	5	6	7	dB
Common mode rejection ratio (G_S max)	C_{MR}	50	60	–	dB
Line signal distortion MPU supply ON V28 ⩽ 3.5 dBm V28 ⩽ 5.5 dBm	 – –	 – –	 – –	 5 10	 % –
Line signal distortion MPU supply OFF V28 ⩽ 3.5 dBm V28 ⩽ 5.5 dBm	 – –	 – –	 – –	 2 10	 % –
Imput impedance Symetrical mode (pin 16.17) Asymetrical mode (pin 16) Asymetrical mode (pin 17)	 Zes Zea Zea	 1.5 0.7 5	 2 1 7	 2.5 1.3 9	kΩ – – –
Transmission noise level (pin 28) (Psophometric R_M = 200 Ω)	–	–	– 65	–	dBmp
Gain reduction during dialing (Note 1)	–	50	–	–	dB
2 wires to 4 wires conversion efficiency (Note 2 – Reception gain from line to earphone is 0 dB: V28/V6 = 1) I_L = 87 mA • Z_L = 600 Ω I_L = 30 mA • Z_L = Z_{LL}	 E E	 15 15	 – –	 – –	dB – –
Earphone amplifier (Note 3) Max gain (no gain control I_L = 30 mA • G_R = V6/ V8)	 G_R max	 19	 20	 21	dB –
Gain control (Reception gain decrease) (Note 3)	GR	5	6	7	–
Earphone signal distortion (R earphone > 150 Ω • V6 = – 10 dBV)	–	–	–	2	%
Output noise level	–	–	– 65	–	dBmp
Impedance: depends on external component, R_Z (Z = (V28/ I28) A_C and R_Z pin 11 = 75 Ω)	Z	500	600	700	Ω
DTMF Generator (note 4) Crystal oscillator frequency Tone frequency accuracy Low group tone level (depends on external components) High group tone level (depends on external components) Preemphasis (depends on external components) DTMF signal distortion (depends on external components) DTMF signal level spread (depends on external components)	 – – – – – – –	 – – 1.5 – 11 – 9 + 1 – – 2	 3.579545 – – – + 2 – –	 – + 1.5 – 6 – 4 + 3 – 26 + 2	 MHz % dBm dBm dB dB dB
Logic inputs (note 5) keyboard mode Switch bounce elimination Keyboard contact resistance "ON" Keyboard contact resistance "OFF"	 – – –	 0.5 – 500	 – – –	 – 10 –	 ms kΩ kΩ
Logic inputs (note 6) M_{PU} mode Current drawn by A.B.C. and D input to go low Current to force inputs E.F.G and H to go high Input impedance	 – – –	 – – –	 20 20 5	 50 50 –	 µA µA kΩ
Input max voltage on A.B.C.D. or E.F.G.H. inputs	–	0	–	V28	V

TESTS DIAGRAMS



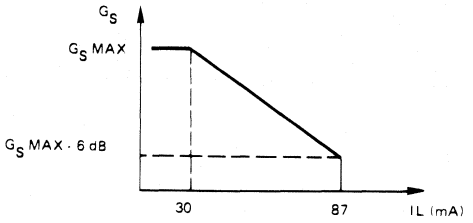
Note 1: Transmission mode - test diagram

External components:

RAL1 = RAL2 = 0
CAL1 = CAL2 = 47 pF
RALB1 = RALB2 = 56 kΩ
REC1 = REC2 = 6.2 kΩ
CEC1 = CEC2 = 2.2 nF
RDTMF = 511 Ω CF1 = 106 nF CF2 = 10 nF
RZ = 75 Ω
RCG1 = 60 kΩ RCG2 = 14 kΩ

Note 1: test conditions (continued)

Maximum transmission gain for IL 30 mA GS_{max} $\frac{V28}{Vm}$



Gain control:

- For IL = 30 mA: GS = GS_{max}.
- For IL = 87 mA: GS = GS_{max} — 6 dB.

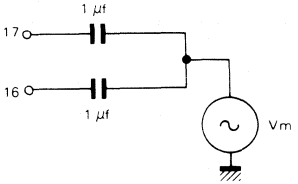
- For other values of line current and corresponding values of RCG1 and RCG2: see application note.

Gain reduction during dialing

- Close swith S (pin 13).

CMRR

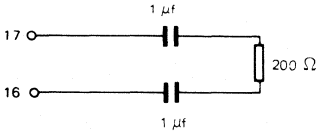
- For IL = 30 mA.



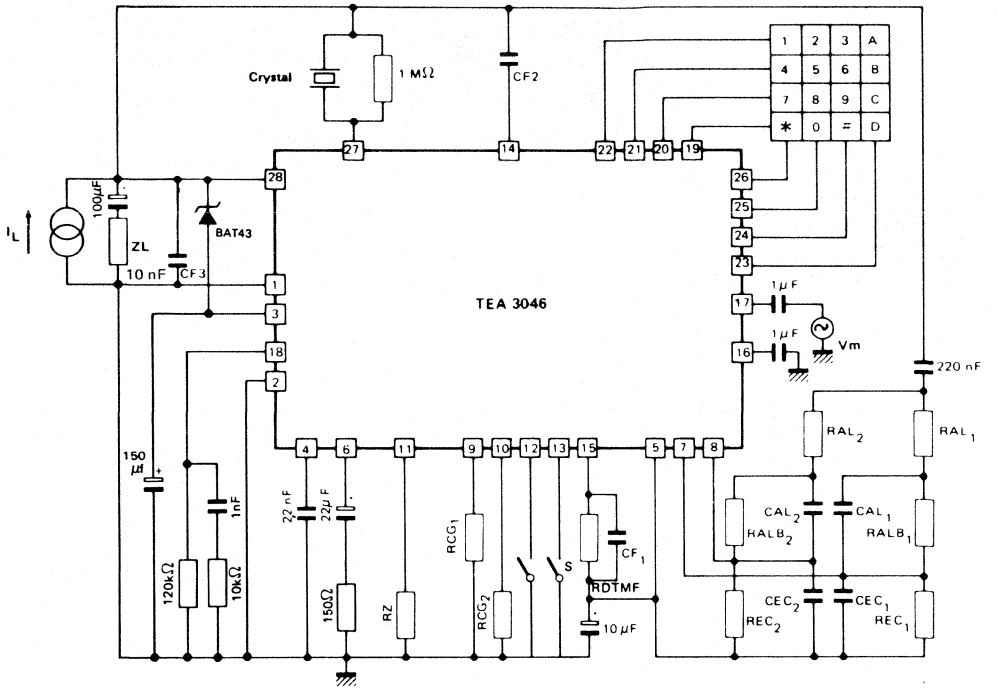
$$GSCM = \frac{V28}{Vm} \quad CMRR = \frac{GS_{max}}{GSCM}$$

Transmission noise level:

- Measured on pin 28 with IL = 30 mA and the corresponding diagram on the microphone inputs.



Note 2: Antisidetone - test diagram



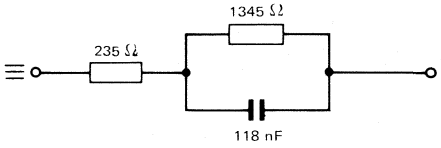
External components:

RZ = 75 Ω RDTMF = 511 Ω CF1 = 106 nF CF2 = 10 nF
RCG1 = 60 kΩ RCG2 = 14 kΩ
RAL1 = 0 RALB1 = 56 kΩ CAL1 = 47 pF REC1 = 6.2 kΩ CEC1 = 2.2 nF
RAL2 = 28 kΩ RALB2 = 51 kΩ CAL2 = 1.15 nF REC2 = 8.2 kΩ CEC2 = 2.2 nF

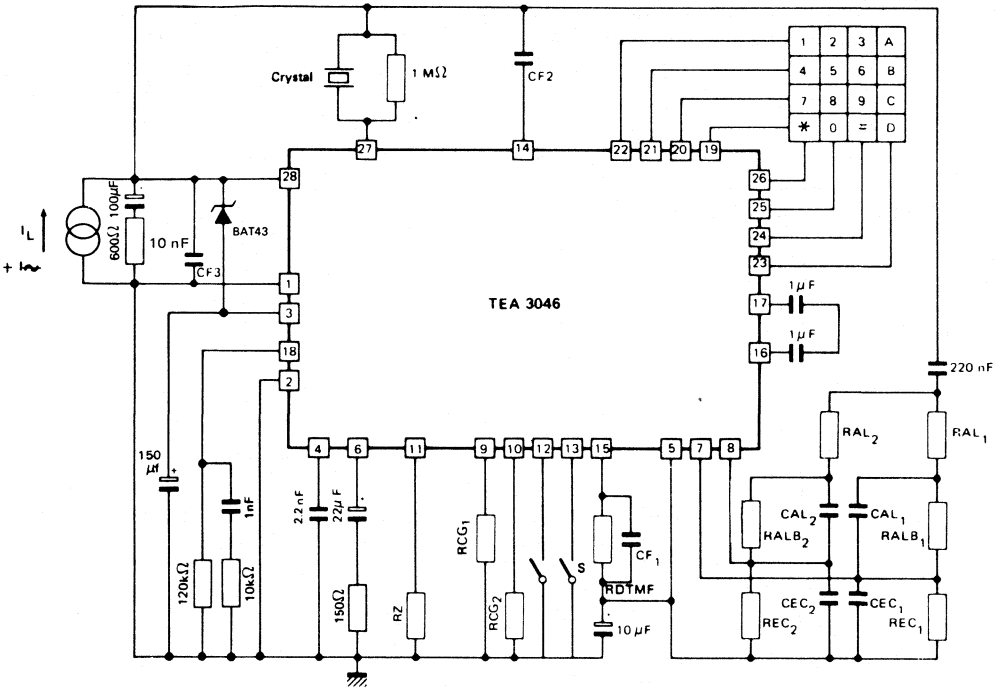
Test conditions:

- Short line: IL = 87 mA ZL = 600 Ω
- Long line: IL = 30 mA ZL = ZLL
  ZLL represents a 3.5 kilometers long line with a diameter = 0.4 mm.
  Antisidetone efficiency:

$$E = 20 \log_{10} \left(\frac{V28}{V6} \right)$$



Note 3: Receiving mode - Test diagram



External conponents:

RAL1 = RAL2 = 0 CAL1 = CAL2 = 47 pF RALB1 = RALB2 = 56 kΩ CEC1 = CEC2 = 62 kΩ
REC1 = REC2 = 2.2 nF RZ = 75 Ω RCG1 = 60 kΩ RCG2 = 14 kΩ RDTMF = 511 Ω
CF1 =106 nF CF2 = 10 nF

Test conditions:

Maximum receiving gain:

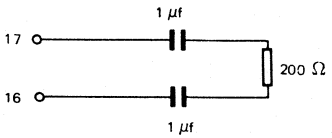
- For IL = 30 mA $GR_{max}=\frac{V6}{V8}$

Gain control:

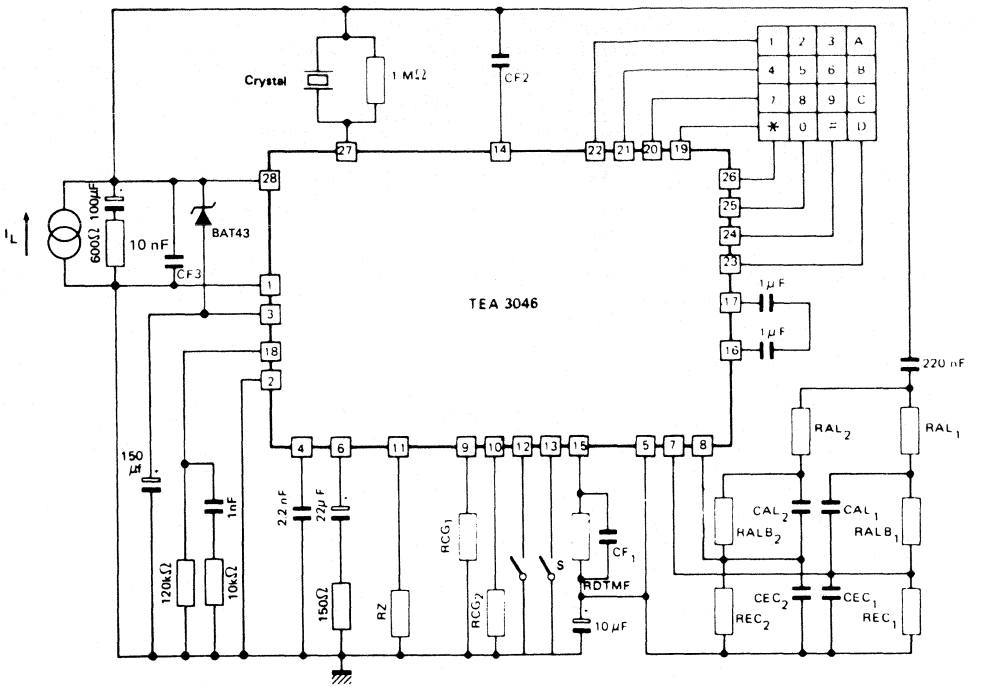
- For IL = 30 mA GR = GR_{max}
- For IL = 87 mA GR = GR_{max} — 6 dB

Output noise level:

- Measured on pin 6, with the corresponding diagram on microphone inputs.



Note 4: DTMF - Test diagram



External conponents:

RAL1 = RAL2 = 0 CAL1 = CAL2 = 47 pF RALB1 = RALB2 = 56 kΩ
CEC1 = CEC2 = 62 kΩ REC1 = REC2 = 2.2 nF
RZ = 75 Ω RCG1 = 60 kΩ RCG2 = 14 kΩ
RDTMF = 511 Ω CF1 =100 nF CF2 = 10 nF
IL = 30 mA

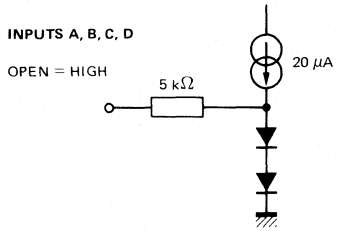
Frequency accuracy, tone levels, preemphasis, distortion can be measured by putting the right code on the logic inputs for every couple of frequencies. See note 5 and 6.

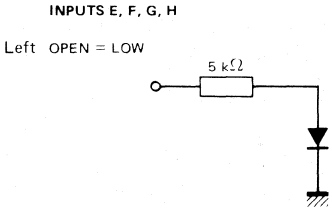
Remaining receiving gain during dialing: the circuit must be in test mode (single-tone).
Remaining gain = 20 $\log_{10}$ (V6/V28).

LOGIC INPUTS TABLE

Note 5: Keypad mode

EQUIVALENT DRAWING OF LOGIC INPUTS





Inputs								Generated tones (Hz)	Symbol	Mute	Notes
A	B	C	D	E	F	G	H				
H	H	H	H	L	L	L	L	–	–	off	5.1
L	H	H	H	L	L	L	L	697	–	on	5.2
H	L	H	H	L	L	L	L	770	–	on	
H	H	L	H	L	L	L	L	852	–	on	
H	H	H	L	L	L	L	L	941	–	on	
H	H	H	H	H	L	L	L	1 209	–	on	5.3
H	H	H	H	L	H	L	L	1 336	–	on	
H	H	H	H	L	L	H	L	1 447	–	on	
H	H	H	H	L	L	L	H	1 633	–	on	
L				H				697 + 1 209	"1"	on	5.4
L					H			697 + 1 336	"2"	on	
L						H		697 + 1 477	"3"	on	
L							H	697 + 1 633	"A"	on	
	L			H				770 + 1 209	"4"	on	
	L				H			770 + 1 336	"5"	on	
	L					H		770 + 1 477	"6"	on	
	L						H	770 + 1 633	"B"	on	
		L		H				852 + 1 209	"7"	on	
		L			H			852 + 1 336	"8"	on	
		L				H		852 + 1 477	"9"	on	
		L					H	852 + 1 633	"C"	on	
			L	H				941 + 1 209	"*"	on	
			L		H			941 + 1 336	"0"	on	
			L			H		941 + 1 477	"#"	on	
			L				H	941 + 1 633	"D"		

Note 5.1: Speech mode.

Note 5.2: Test mode.
Low group tones.

Note 5.3: Test mode.
High group tones.

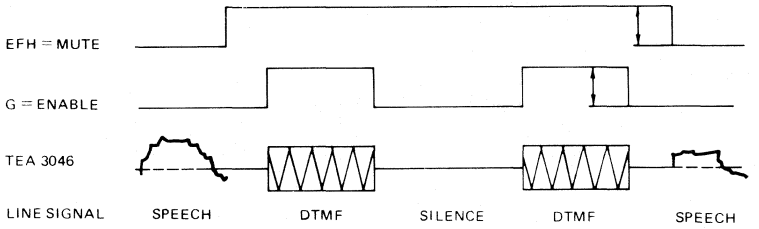
Note 5.4: This table is only valid if E,F,H, = low.
As soon as one of the inputs E,F,G,H, is high, the others are considered low.
As soon as one of the inputs A,B,C,D, is low, the others are considered high.

Note 6: Logic inputs table - Microprocessor mode

Inputs								Generated tones (Hz)	Symbol	Mute	Notes
A	B	C	D	E	F	H	G				
H	H	H	H		L		L	–	–	off	6.1
X	X	X	X		H		L	–	–	on	6.2
H	H	H	H		H		H	697 + 1 209	"1"	on	
H	H	H	L		H		H	697 + 1 336	"2"	on	
H	H	L	H		H		H	697 + 1 477	"3"	on	
H	H	L	L		H		H	697 + 1 633	"A"	on	
H	L	H	H		H		H	770 + 1 209	"4"	on	
H	L	H	L		H		H	770 + 1 336	"5"	on	
H	L	L	H		H		H	770 + 1 477	"6"	on	6.3
H	L	L	L		H		H	770 + 1 633	"B"	on	
L	H	H	H		H		H	852 + 1 209	"7"	on	
L	H	H	L		H		H	852 + 1 336	"8"	on	
L	H	L	H		H		H	852 + 1 477	"9"	on	
L	H	L	L		H		H	852 + 1 633	"C"	on	
L	L	H	H		H		H	941 + 1 209	"*"	on	
L	L	H	L		H		H	941 + 1 336	"0"	on	
L	L	L	H		H		H	941 + 1 477	"#"	On	
L	L	L	L		H		H	941 + 1 633	"D"	on	

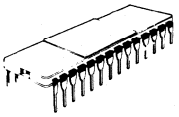
Note 6.1: Speech mode.
Note 6.2: Silence position.
Note 6.3: Mute coincides with tone bursts.

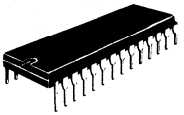
Impedance mute or silent setting



PHYSICAL DIMENSIONS

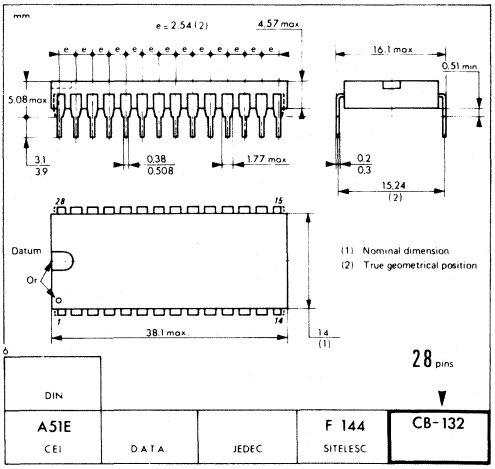
CB-132





C SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE



These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

HOMSON
COMPONENTS
MICONDUCTEURS

TEA7047

SPEECH AND TONE

Specially designed for telephone applications this 28 pins IC provides:

- Transmission and line adaptation.
- DTMF generation.
- Power supply for peripherals.
- Interface with MCU.

It meets completely the CEPT specifications.

Major advantages

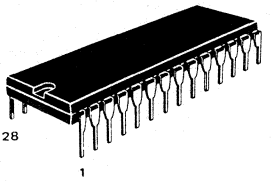
- Adjustable automatic line length receiving and sending gain control.
- Adjustable automatic line length tracking antisidetone system.
- Adjustable microphone and earphone amplifier gain.
- Adjustable complex or real dynamic impedance.

Other advantages

- Emission noise level typically — 75 dBmp.
- High input impedance.
- Inhibition of gain control possible.
- Mute in emission and reception.
- Two keys roll over provided.
- Adjustable output tone level.
- Click-free switch over from speech to dialing mode & vice-versa.

BIPOLAR

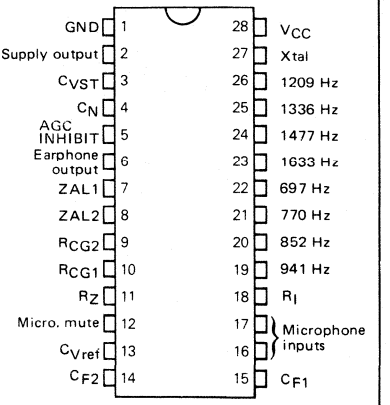
CASE
CB-132



DP SUFFIX
PLASTIC PACKAGE

Also available in SO package
(FP SUFFIX)

PIN ASSIGNMENT



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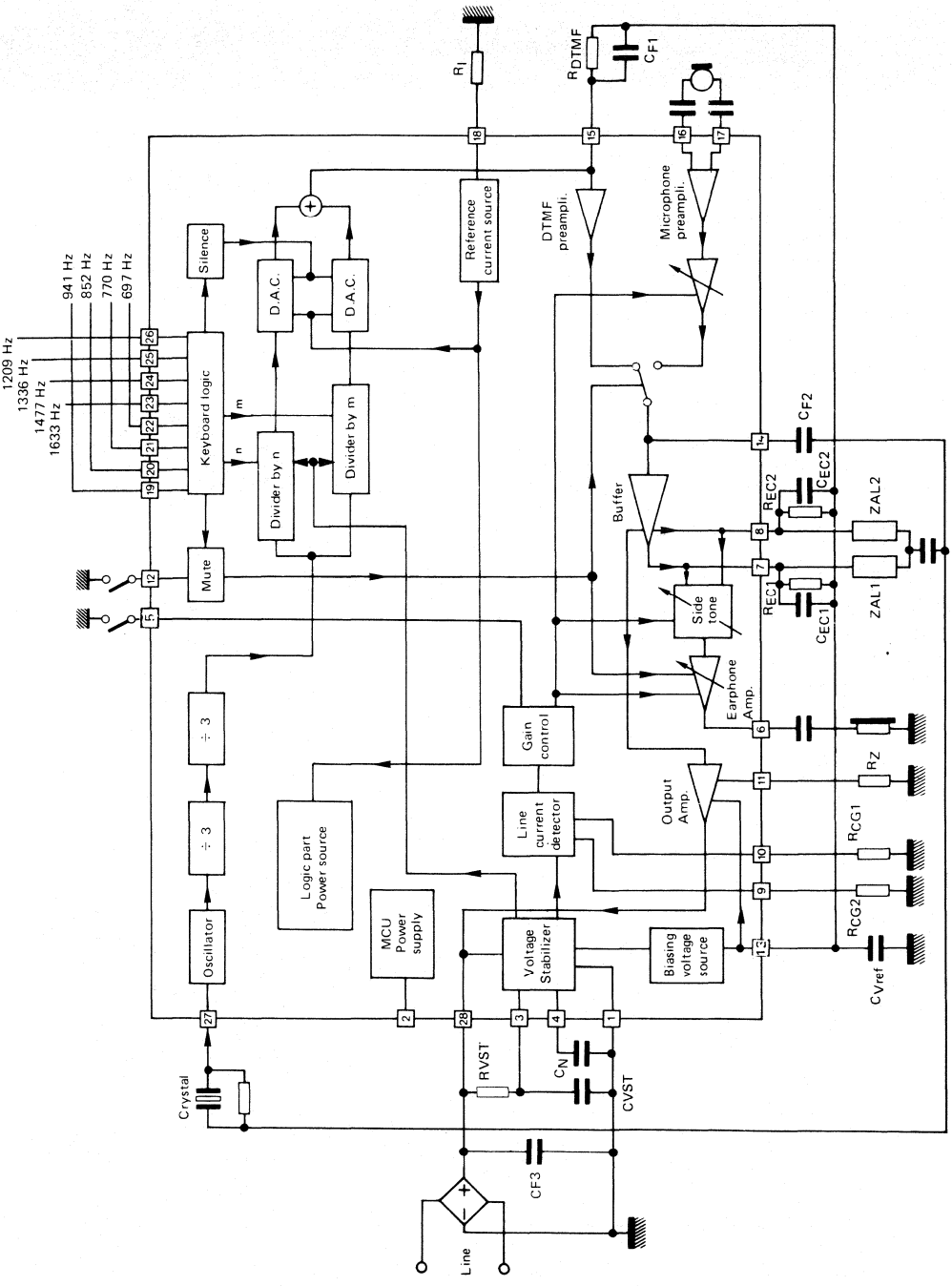
BLOCK DIAGRAM



PIN DESCRIPTION

POWER SUPPLY:

Name	No.	Description
GND	1	Ground
C_{VST}	3	C_{VST} decouples the voltage stabilizer
C_N	4	Capacitor to reduce noise
C_{VREF}	13	C_{VREF} decouples the biasing voltage. This reference biasing voltage is temperature stable
R_I	18	V_{REF} on this pin is temperature stable. R_I fixes internal current sources value
V_{CC}	28	

MICROPROCESSOR POWER SUPPLY:

Name	No.	Description
Supply output	2	Microprocessor power supply output

TRANSMIT SECTION:

Name	No.	Description
R_Z	11	R_Z fixes the impedance value of the circuit
Mute	12	A short circuit to the ground on this pin mutes the microphone and earphone signal.
C_{F2}	14	C_{F2} filters both microphone and DTMF signals
Microphone input	16	
Microphone input	17	

RECEIVE SECTION:

Name	No.	Description
Earphone output	6	Earphone amplifier output
Z_{AL1}	7	Short line antisidetone network Z_{AL1} and input of the earphone amplifier.
Z_{AL2}	8	Long line antisidetone network Z_{AL2} and input of the earphone amplifier.

GAIN CONTROL SYSTEM:

Name	No.	Description
G_{inh}	5	A short circuit to the ground on this pin inhibits the gain control system
R_{CG2}	9	R_{CG2} fixes the gain control (see note 4)
R_{CG1}	10	R_{CG1} fixes the gain control (see note 4)

PIN DESCRIPTION (continued)

DTMP SECTION:

Name	No.	Description
$C_{F1} + R_{DTMF}$	15	C_{F1} and R_{DTMF} filter the DTMF signal and set the DTMF signal level
941 Hz	19	"D" logic input. 941 Hz keyboard row
852 Hz	20	"C" logic input. 852 Hz keyboard row
770 Hz	21	"B" logic input. 770 Hz keyboard row
697 Hz	22	"A" logic input. 697 Hz keyboard row
1633 Hz	23	"H" logic input. 1633 Hz keyboard column
1477 Hz	24	"G" logic input. 1477 Hz keyboard column
1336 Hz	25	"F" logic input. 1336 Hz keyboard column
1209 Hz	26	"E" logic input. 1209 Hz keyboard column
X_{tal}	27	Oscillator input

FUNCTIONAL DESCRIPTION

OUTLINES

Specially designed for a basic low cost telephone set application, this 28 pins IC provides transmission and line adaptation, DTMF generation and power supply for peripheral circuits. Interface is also possible with a micro computer for a more sophisticated set.

Transmission and line adaptation

Includes Microphone and Telephone amplification, both with line length depending gain control and a line impedance automatic matching 2-wire to 4-wire conversion.

The microphone amplifier performs high CMRR, for crosstalk and low noise characteristic. Its architecture permits symmetrical inputs and external adjustment of gain to fit different microphone capsules. A single pole filter limits the amplifier banwidth for a best high frequency figure.

The earphone amplifier is a low consumption type. It is click free when muted and its gain can be externally adjusted.

2-wire to 4-wire conversion is performed by subtracting microphone signal from line before applying it to earphone amplifier. An automatic line impedance tracking antisidetone system performs an excellent sidetone efficiency for every line length.

The dynamic impedance of the circuit is fixed by an external resistor so as to match with different line impedance.

The line length is sensed through the line current. 2 external components allow the gain control to compensate any kind of line length and feeding bridge.

DTMF signal generation

Tones are obtained from a crystal controlled oscillator followed by two independent programmable dividers and 2 sinewave synthesizers. Crystal is an inexpensive TV model 3.58 MHz oscillator.

Amplitude of multi frequency signal is set by an external resistor.

The required tone frequencies are selected by either an inexpensive single contact 4 x 4 keypad or by a microcomputer. Single-tone operation for testing purposes is also possible.

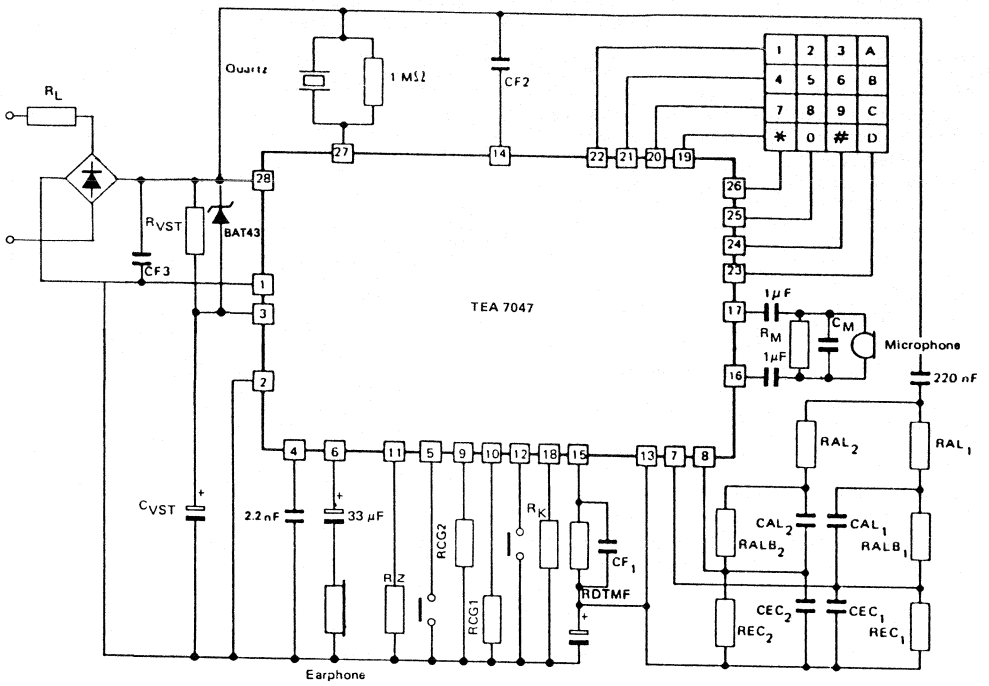
The power supply

This is 0.75 mA current source with a typical maximum voltage compliance of a 3.2 volts.

It can power either an electret microphone or a microcomputer.

If this source is not used it is possible to connect the pin 2 to ground to reduce the I_{CC} (pin 28) current.

APPLICATION DIAGRAM: PUBLIC LINE



R_L	= 100 Ω			R_{AL1}	= 30 kΩ	R_{ALB1}	= 73 kΩ
R_{DTMF}	= 560 Ω	C_{F1}	= 120 nF	R_{AL2}	= 43.2 kΩ	R_{ALB2}	= 80 kΩ
R_Z	= 100 Ω	R_K	= 3.75 kΩ (1 %)	R_{EC1}	= 6.8 kΩ	C_{EC1}	= 12 nF
R_{CG1}	= 120 kΩ			R_{EC2}	= 8.2 kΩ	C_{EC2}	= 12 nF
R_{CG2}	= 220 kΩ			R_{VST}	= 5.6 kΩ		
C_{VREF}	= 10 µF	C_{VST}	= 68 µF	C_{AL1}	= 1 nF	C_{AL2}	= 1.5 nF
C_{F3}	= 33 nF						
C_{F2}	= 2.2 nF						
R_M	= 10 kΩ	C_M	= 22 nF				

This application diagram is adapted to German specifications.

APPLICATIONS INFORMATION

SPEECH MODE

Microphone amplifier

The microphone amplifier inputs can only be driven in symmetrical mode. The input impedance of the microphone amplifier is fixed by an external resistor R_I connected between the microphone inputs (17), (16). The input impedance of the microphone amplifier is typically $Z_{IN0} = 58\ k\Omega$ so the value of R_I is given by:

$$R_I = \frac{Z_{IN} \times Z_{IN0}}{Z_{IN0} - Z_{IN}}$$

where Z_{IN} is the desired input impedance.

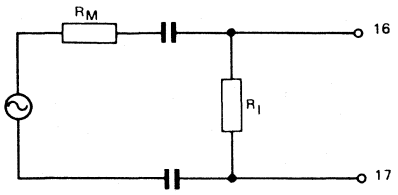
Numerical example:

For $Z_{IN} = 16\ k\Omega$ $R_I = 22\ k\Omega$

The maximum gain of the microphone amplifier is 9.5 dB and it can be decreased by an external resistor R_M connected between one of the inputs and the microphone. R_M is calculated as shown:

$$R_M = \frac{-(G_1 + 3) \times Z_{IN}}{G_1}$$

where G_1 is the desired gain (G_1 has a negative value).



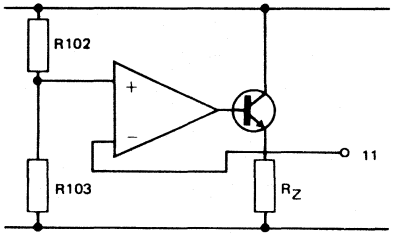
Output impedance: Z_{AC}

The main part of the circuit impedance is fixed by the output stage. You must also include the output impedance of the voltage stabilizer R_{100}, a parasitic impedance R_P corresponding to all the other stages of the circuit seen from the line, the protection resistor R_L and the different components C_{F3}, C_{F4}, R_{F4} used to set a complex output impedance.

Output stage impedance: Z_{out}

$$Z_{out} = R_z \frac{R_{102} + R_{103}}{R_{103}}$$

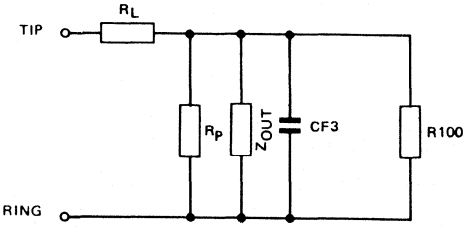
$$\frac{R_{102} + R_{103}}{R_{103}} = 10.75$$



R_{102} and R_{103} are internal resistors, so Z_{out} is fixed by R_z.

The application set impedance is given by:
$Z_{AC} = R_L + (Z_{CF3} // R_p // Z_{out} // R_{100})$

Equivalent circuit from the line:



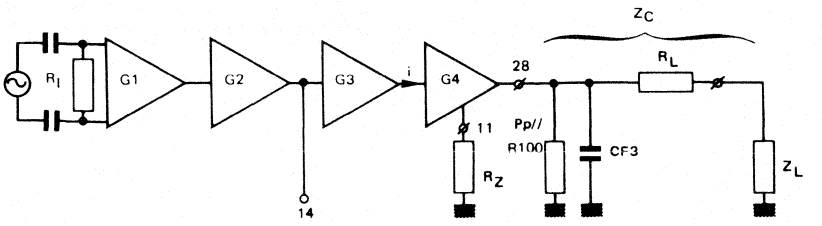
Numerical example:

$R_z = 110\ \Omega$ $R_L = 12\ \Omega$ $R_p = 20\ k\Omega$
$R_{100} = 5\ k\Omega$ $C_{F3} = 4{,}7\ nF$
$Z_{out} = 1180\ \Omega$ and $|Z_{AC}| = 879\ \Omega$ at F = 1 kHz

Overall maximum gain

This calculation is done with $R_M = 0$ and inhibited gain control.

We have a schematic representation of the transistor chain:



G_1 is the gain of the microphoneamplifier: $G_1 = -3$
G_2 is the gain of the customatic-gain-control stage: $G_2 = -4$
G_3 is a transconductance corresponding to the buffer stage : $G_3 = 1/4\ k\Omega$

$i = V_{14}\ 4\ k\Omega$

G_4 is the transresistance of the output stage; it is given by

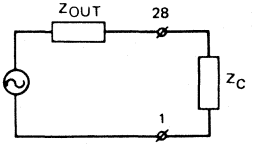
$$G_4 = -K\ \frac{Z_C}{Z_C - Z_{out}}$$

where Z_C represents the impedance seen by the output stage

$$Z_C = R_p \quad R_{100} // Z_{CF3} // (Z_L + R_L)$$

and K is a constant defined by internal components: $K = 175\ k\Omega$.

An equivalent circuit of the transmission chain can be defined:



$$G_{max} = -525\ \frac{Z_C}{Z_C + Z_{out}}$$

Numerical example:

With the components specified in the calculation of Z_{AC} and $Z_L = 600\ \Omega$ we obtain:

$G_{max} = 160$ or $G_{max} = 44.1$ dB at $f = 1$ kHz

Cut off frequency of the emission chain

Two external components affect the frequency response of the emission chain: C_{F2}, C_{F3}.

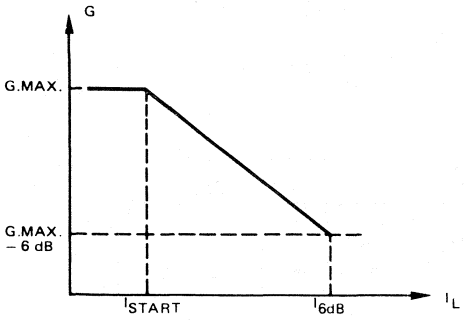
The values for those components specified on the application set permit to have less than 1 dB attenuation at 3400 Hz; and a cut off frequency of 7 kHz ($C_{F2} = 2.2$ nF; $C_{F3} = 4.7$ nF).

Remark that C_{F3}, C_{F4} and R_{F4} also affect the output impedance Z_{AC}. C_{F2} associated with a 4 kΩ internal resistor produces a first order filter which recommended cut off frequency is 18 kHz to have a good preemphasis in DTMF mode.

GAIN CONTROL SYSTEM (in both transmission and reception)

The gains of transmission and reception chains are depending on the linelength; so the gain control system is driven by the line current. A fixed amount 10 of the line current is drained for the proper operation of the circuit, the rest of the current ($I_L - I_0$) is measured and the result is used in the AGC. In the TEA7047 we have $I_0 = 13.7$ mA.

Two resistors are defining the currents where you have the maximum gain (G_{max} for I_{START}) and the lowest gain ($G_{max} - 6$ dB for I_6 dB).



Gain = G_{max} for $I_L < I_{start}$
Gain decreases for $I_{start} < I_L < I_6$ dB
Gain = G_{max} — 6 dB for $I_L = I_6$ dB

When I_{start} and I_6 dB are defined there are two relations for calculating the corresponding resistors R_{CG1} and R_{CG2}.

$$R_{CG1} = \frac{1600}{I_{START} - I_0}$$

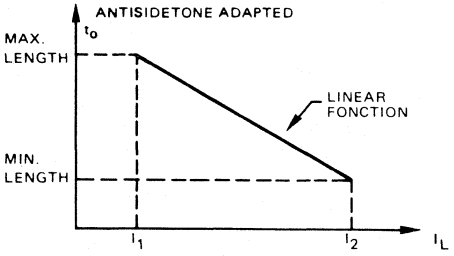
$$R_{CG2} = \frac{1600}{I_6\ dB - I_{START}}$$

where the currents are in mA and the resistors in kΩ.

The gain control system can be inhibited by putting pin 5 to the ground. In this case you always have the maximum gain in both emission and reception.

ANTISIDETONE SYSTEM

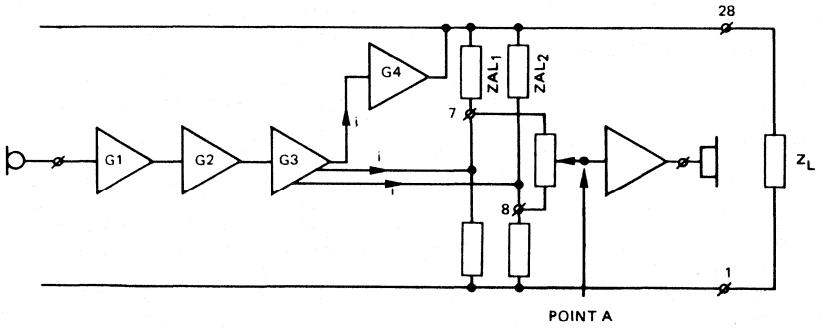
The TEA7047 has double antisidetone system. One is adapted to maximum line length and the other one is adapted to minimum line length. We have seen that the line length can be controlled by the measurement of the current line so the two antisidetone systems will be balanced according to the current line.



I_1 and I_2 are the currents defined as I_{START} and I_6 dB in the AGC chapter; they are fixed by R_{CG1} and R_{CG2} (pins (10) and (9)).

Basic principle of antisidetone system:

We can represent the transmission and reception chain as shown:



Z_{AL1} is the short line antisidetone network
Z_{AL2} is the long line antisidetone network

The impedance seen from the point A is a linear combination of the two antisidetone networks Z_{AL1} and Z_{AL2}. This combination depends on the line current and the values of R_{CG1} and R_{CG2}. In fact, there is only one antisidetone network seen from the point A: Z_{AL}.

with: $Z_{AL} = B Z_{AL1} + (1 - B) Z_{AL2}$ $\quad (0 < B < 1)$

Calculation of the antisidetone networks:

For a perfect antisidetone, the signal on point A must be null in transmission mode, so we must have:

$$i + \frac{V_L}{Z_{AL}} = 0 \qquad (1)$$

where V_L is the AC voltage on the line

In transmission mode, V_L is given by:

$$V_L = G_4\, i = -K\, i\, \frac{Z_C}{Z_C + Z_{out}} = \frac{-K}{Z_{out}}\; i\,(Z_C \,//\, Z_{out}) \qquad (2)$$

The combination of (1) et (2) gives:

$$Z_{AL} = \frac{K}{Z_{out}}\,(Z_C \quad Z_{out}) = \gamma\, Z_C \,//\, Z_{out} \text{ with } \gamma = \frac{K}{Z_{out}}$$

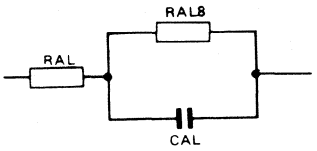
Z_{AL} must be proportional to $Z_C \,//\, Z_{out}$

We have the value of Z_{AL}:

$$Z_{AL} = \gamma\,[(Z_L - R_L) \quad Z_{CF3} \,//\, R_{100} \,//\, R_p \,//\, Z_{out}]$$

This calculation must be done twice to obtain the two antisidetone networks corresponding to maximum and minimum line length. You can remark that this calculation is not easily done. Consequently we have developed a program which calculates all the external components of the application set and especially the two antisidetone networks for every type of line. Please contact an application engineer for mor detailed information.

This programm calculates the antisidetone networks as shown:



GAIN IN RECEPTION MODE

The typical gain of the earphone amplifier is 26 dB.

You can adjust the reception gain in your application set with the two resistors R_{EC1} and R_{EC2} connected respectively between pin (7) and (8) and the ground. At your working frequency the gain of the reception chain between the line and the earphone is given by:

$$G_{max} = 26\text{ dB} - 20 \log \frac{R_{EC1}}{R_{EC1} + |Z_{AL}|}$$

This gain must be adjusted for maximum and minimum line length. The two capacitors C_{EC1} and C_{EC2} are calculated to have the same cut off frequency.

DTMF AMPLITUDE SIGNAL

The amplitude of the DTMF signal is set by an external resistor R_{DTMF} between pin 5 and pin 15.

The preamphasis for high group tones is typically 2 dB and the reference level is defined by the amplitude of low group tones.

If N dB is the level desired for low group tones, R_{DTMF} is given by:

$$R_{DTMF} = 1095 \,.\, 10^5 \,.\, 10^{(N\text{ dB} - 35.5)/20}$$

The right levels in DTMF mode are obtained if the cut off frequency of the two filters 1 and 2 have the right value:

filter 1 C_{F1}, R_{DTMF} $f_{C1} = 2200$ Hz

filter 2 C_{F2} and internal resistor 4 kΩ
$f_{C2} = 18$ kHz

A third filter is made by C_{F3}, C_{F4} and R_{L4}.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	8.5	V
Power dissipation	P_{tot}	1.1	W
Operating temperature range	T_{oper}	− 25 to + 65	°C
Storage temperature range	T_{stg}	− 55 to + 150	°C
Max. current before destruction of the circuit ($t < 250\ \mu s$)	T_{surge}	850	mA

STATIC ELECTRICAL CHARACTERISTICS:
$-25°C \leq T_{amb} \leq +65°C$, line impedance = $Z_L = 600\ \Omega$

Characteristic	Symbol	Min	Typ	Max	Unit
Line current (Pin 28)					mA
MPU supply OFF	I_L	15		120	
MPU supply ON	I_L	17		120	
Voltage over the IC (Pin 28)					V
I_L = 15 mA (R_{VST} = 5.6 kΩ)	V_{28}		5.4		
I_L = 120 mA (R_{VST} = 5.6 kΩ)	V_{28}		6.8		
Voltage stabilizer (Pin 3)					V
I_L = 15 mA	V_C		2.7		
I_L = 120 mA	V_C		4		
Power supply (Pin 2)					mA
Max current (V_2 = 3.2 V)					
Sending mode	I_2	0.75			
Without AC line signal	I_2	1			

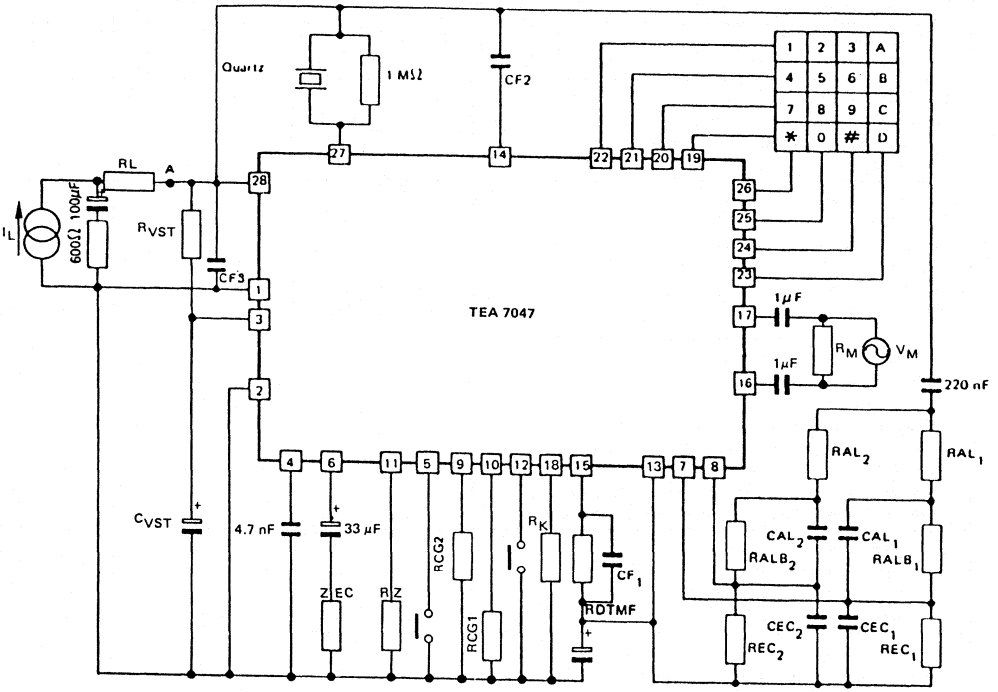
DYNAMIC ELECTRICAL CHARACTERISTICS:
T_{amb} = 25°C, line impedance = Z_L = 600 Ω, frequency = f = 1 kHz

Characteristic	Symbol	Min	Typ	Max	Unit
Max sending gain (No gain control action note 1)	G_{Smax}	43	44	45	dB
Gain control Sending gain decrease (note 1)		5	6	7	dB
Common mode rejection ratio (G_{Smax})	CMRR	50	60		dB
Line signal distortion MPU supply OFF					
$V_{28} < 3.5$ dBm				2	%
3.5 dBm $< V_{28} <$ 5.5 dBm				10	%
Line signal distortion MPU supply ON					
$V_{28} < 3.5$ dBm				5	%
3.5 dBm $< V_{28} <$ 5.5 dBm				10	%
Microphone input impedance Symetric mode	Z_{IN}	50	58		kΩ
Transmission noise level (note 1) psophometric		− 72	− 75		dBmp
Gain reduction during dialling		60			dB
Gain reduction in mute mode		60			dB
Earphone amplifier (note 2)					
Max gain (No gain control action)	G_{Rmax}	25	26	27	dB
Gain control (Reception gain decrease)		5	6	7	dB

DYNAMIC ELECTRICAL CHARACTERISTICS (continued):

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Earphone signal distortion (R earphone $< 150\ \Omega$. $V_6 = -10$ dBv)				2	%
Output impedance	Z_{ec}			3	Ω
Output noise level		− 72	− 75		dBmp
2 to 4 wires conversion (note 3) Efficiency					
$I_L = 80$ mA $Z_L = 600\ \Omega$	E	15			dB
$I_L = 30$ mA $Z_L = Z_{LL}$	E	15			dB
Impedance: depends on R_Z (note 2) $R_Z = 100\ \Omega$ Return loss compared to Z_0 (note 2)					
200 Hz $< f <$ 500 Hz	RL	12			dB
500 Hz $< f <$ 2500 Hz	RL	15			dB
2500 Hz $< f <$ 4000 Hz	RL	12			dB
DTMF generator (note 4)					
Crystal oscillator frequency			3.579545		MHz
Tone frequency accuracy		− 1.5		+ 1.5	%
Low group tone level (depends on external components)		− 11		− 6	dBm
High group tone level (depends on external components)		− 9		− 4	dBm
Preemphasis (depends on external components)		+ 1	+ 2	+ 3	dB
Distortion DTMF signal (depends on external components)				− 26	dB
DTMF signal level spread (depends on external components)		− 2		+ 2	dB
Logic inputs (note 5) keyboard mode					
Switch bounce elimination		0.5			ms
Keyboard contact resistance "ON"				10	kΩ
Keyboard contact resistance "OFF"		500			kΩ
Logic inputs (note 6) MPU mode					
Current drawn by A, B, C or D input to go low			20	50	μA
Current to force inputs E, F, G and H to go high			20	50	μA
Input impedance			5		kΩ
Input max voltage on A, B, C, D or E, F, G, H inputs		0		V_{28}	V

Note 1: Transmission mode — Test diagram



External components:

R_K	= 3.75 kΩ	R_Z	= 100 Ω	R_{VST}	= 5.6 kΩ	C_{VST}	= 68 μF
R_{CG1}	= 120 kΩ	R_{CG2}	= 47 kΩ	C_{VREF}	= 10 μF	R_L	= 100 Ω
R_{DTMF}	= 560 Ω	C_{F1}	= 120 nF	C_{F2}	= 2.2 nF	C_{F3}	= 33 nF
R_{AL1}	= 33 kΩ	R_{ALB1}	= 44.6 kΩ	C_{AL1}	= 560 pF	R_{EC1}	= 3.9 kΩ
R_{AL2}	= 47 kΩ	R_{ALB2}	= 67 kΩ	C_{AL2}	= 1.5 nF	R_{EC2}	= 6 kΩ
Z_{EC}	= 150 Ω	R_M	= 10 kΩ	C_{EC1}	= 15 nF	C_{EC2}	= 15 nF

Note 1 (continued):

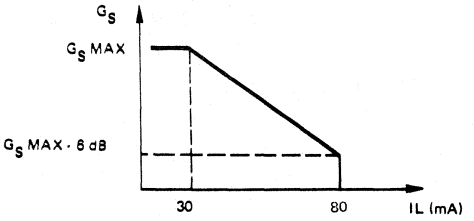
Test conditions:

- Maximum transmission gain:

for $I_L = 30$ mA $\quad G_{Smax} = \frac{V_A}{V_M}$

- Gain control:

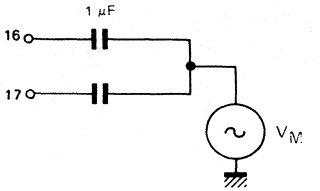
for $I_L = 30$ mA $\quad G_S = G_{Smax}$
for $I_L = 80$ mA $\quad G_S = G_{Smax} - 6$ dB



for other values of line current and corresponding values of R_{CG1} and R_{CG2}: see application note.

- C_{MRR}:

For I_L = 30 mA with the following diagram on microphone inputs.

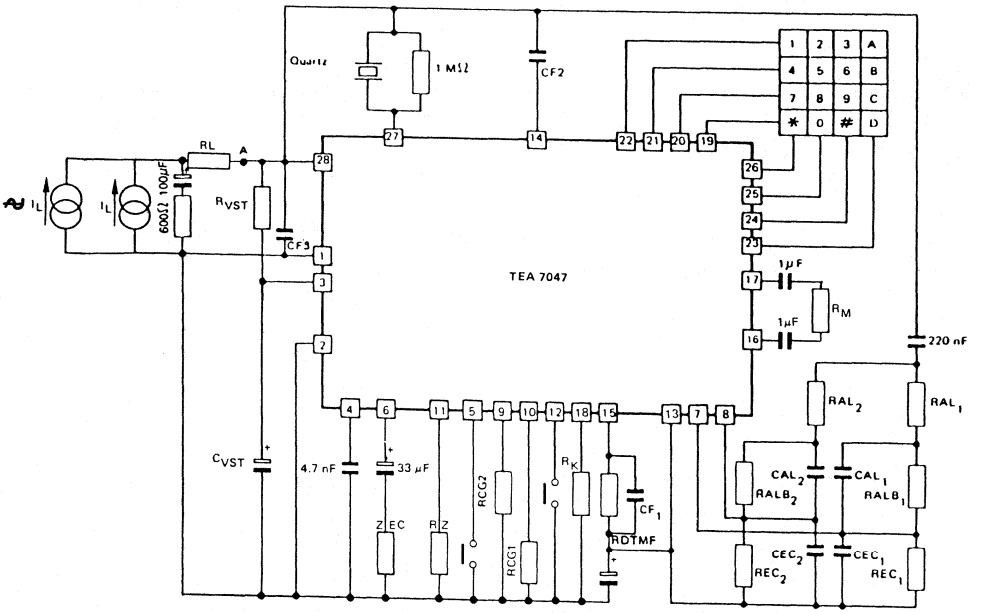


$$G_{SCM} = \frac{V_{28}}{V_M}$$

$$C_{MRR} = \frac{G_{Smax}}{G_{SCM}}$$

- Gain reduction in mute mode: close switch S
- Noise: measured on pin 28 with $R_M = 200\ \Omega$

Note 2: Reception mode — Test diagram



External components:

Idem note 1 + Z_{EC} = 150 Ω

Test conditions:

- Maximum receiving gain:

  for I_L = 30 mA $\quad G_{Rmax} = \dfrac{V_6}{V_8}$

- Gain control:

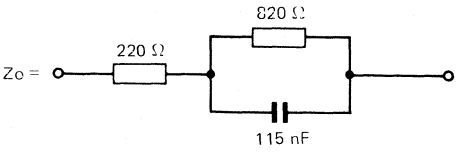
  for I_L = 30 mA $\quad G_R = G_{Rmax}$
  for I_L = 80 mA $\quad G_R = G_{Rmax} - 6$ dB

- Noise level: measured on pin 6 with R_M = 200 Ω

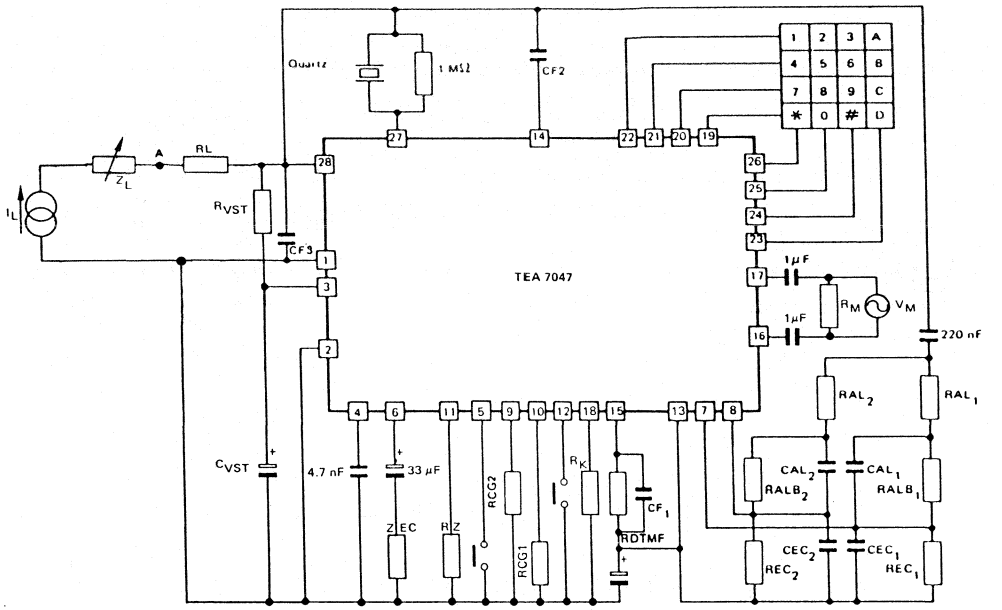
- Impedance: at I_L = 30 mA and the external 600 Ω resistor disconnected

  the AC impedance is defined by: $Z_{out} = \dfrac{V_A}{I_L}$

The return loss is defined by: $RL = 20 \log \dfrac{|Z + Z_0|}{|Z - Z_0|}$



Note 3: Antisidetone efficiency — Test diagram

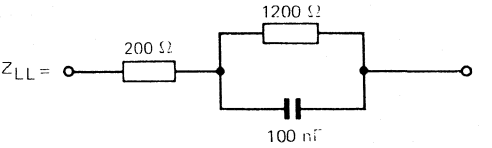


External components:

Idem note 1

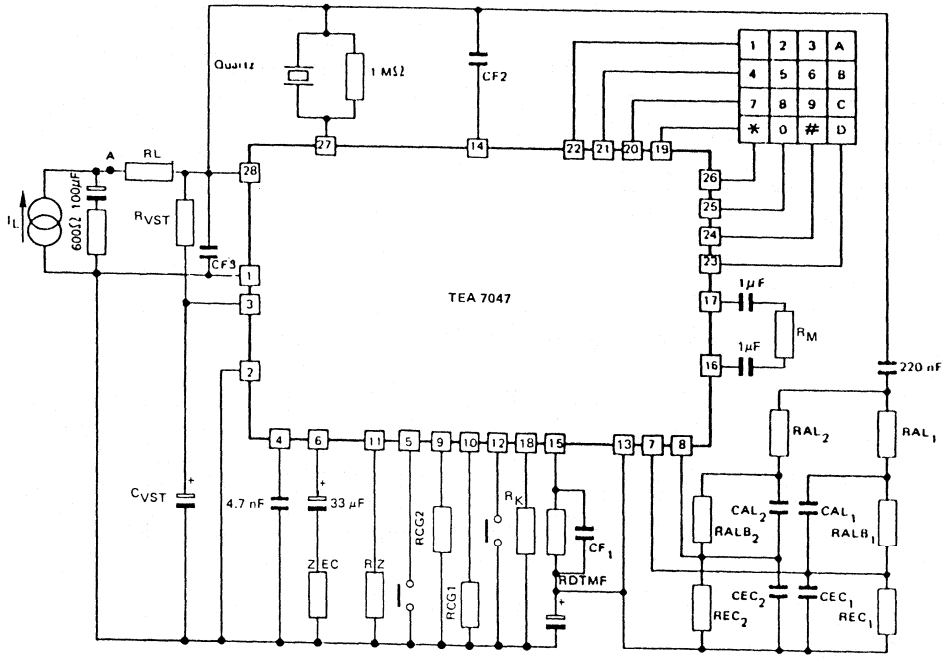
Test conditions:

- Short line: $I_L = 80$ mA $\quad Z_L = 600\ \Omega$
- Long line: $I_L = 30$ mA $\quad Z_L = Z_{LL}$



Antisidetone efficiency : $E = 20 \log_{10} \left(\frac{V_6}{V_A} \right)$

Note 4: Dual tone multifrequency — Test diagram



External components:

Idem note 1

Test conditions:

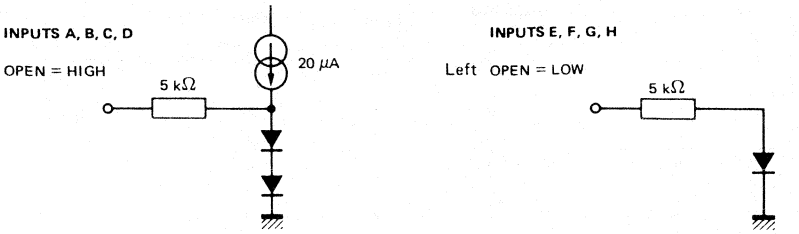
— Frequency accuracy
— Tone levels
— Pre-emphasis
— Distortion

} can be measured by putting the right code on the logic inputs, for every couple of frequencies (note 5 and 6)

— Remaining receiving gain during dialling = 20 log (V_6/V_A)

Note 5 : Logic inputs table - Keyboard mode

EQUIVALENT DRAWING OF LOGIC INPUTS

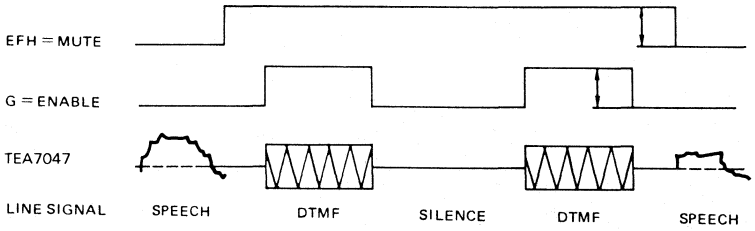


Inputs								Generated tones (Hz)	Symbol	Mute	Remarks
A	B	C	D	E	F	G	H				
H	H	H	H	L	L	L	L	–	–	off	Speech mode
L	H	H	H	L	L	L	L	697	–	on	Test mode
H	L	H	H	L	L	L	L	770	–	on	Low group tones
H	H	L	H	L	L	L	L	852	–	on	
H	H	H	L	L	L	L	L	941	–	on	
H	H	H	H	H	L	L	L	1 209	–	on	Test mode
H	H	H	H	L	H	L	L	1 336	–	on	High group tones
H	H	H	H	L	L	H	L	1 447	–	on	
H	H	H	H	L	L	L	H	1 633	–	on	
L				H				697 + 1 209	"1"	on	This table is only valid if E, F, H, = low As soon as one of the inputs E, F, G, H is high, others are considered low.
L					H			697 + 1 336	"2"	on	
L						H		697 + 1 477	"3"	on	
L							H	697 + 1 633	"A"	on	
	L			H				770 + 1 209	"4"	on	
	L				H			770 + 1 336	"5"	on	
	L					H		770 + 1 477	"6"	on	
	L						H	770 + 1 633	"B"	on	
		L		H				852 + 1 209	"7"	on	
		L			H			852 + 1 336	"8"	on	As soon as one of the inputs A, B, C, D is low, others are considered high.
		L				H		852 + 1 477	"9"	on	
		L					H	852 + 1 633	"C"	on	
			L	H				941 + 1 209	"*"	on	
			L		H			941 + 1 336	"0"	on	
			L			H		941 + 1 477	"#"	on	
			L				H	941 + 1 633	"D"		

Note 6 : Logic inputs table - Microcomputer mode

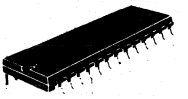
Inputs								Generated tones (Hz)	Symbol	Mute	Remarks
A	B	C	D	E	F	H	G				
H	H	H	H		L		L	-	-	off	Speech mode
X	X	X	X		H		L	-	-	on	Silent position
H	H	H	H		H		H	697 + 1 209	"1"	on	Mute coincides with tone bursts.
H	H	H	L		H		H	697 + 1 336	"2"	on	
H	H	L	H		H		H	697 + 1 477	"3"	on	
H	H	L	L		H		H	697 + 1 633	"A"	on	
H	L	H	H		H		H	770 + 1 209	"4"	on	
H	L	H	L		H		H	770 + 1 336	"5"	on	
H	L	L	H		H		H	770 + 1 477	"6"	on	
H	L	L	L		H		H	770 + 1 633	"B"	on	
L	H	H	H		H		H	852 + 1 209	"7"	on	
L	H	H	L		H		H	852 + 1 336	"8"	on	
L	H	L	H		H		H	852 + 1 477	"9"	on	
L	H	L	L		H		H	852 + 1 633	"C"	on	
L	L	H	H		H		H	941 + 1 209	"*"	on	
L	L	H	L		H		H	941 + 1 336	"0"	on	
L	L	L	H		H		H	941 + 1 477	"#"	On	
L	L	L	L		H		H	941 + 1 633	"D"	on	

Impedance mute or silent setting

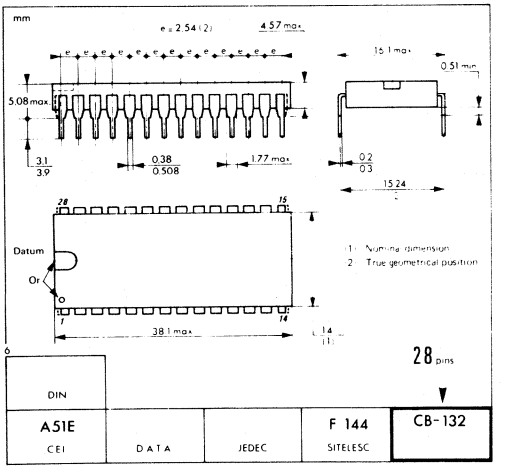


PHYSICAL DIMENSIONS

CB-132



PLASTIC PACKAGE



These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.:DSTEA7047

TEA7037

SPEECH AND TONE

Specially designed for telephone set applications this 28 pins IC provides:

- Transmission and line adaptation.
- F.V. generation.
- Power supply for peripherals.
- Interface with MCU.

It meets the French Specifications for handset homologation level 1.

Major advantages

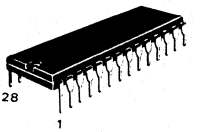
- Automatic line length receiving and sending gain control.
- Automatic line length tracking antisidetone system.
- Adjustable microphone and earphone amplifier gain.
- Meets French voltage/current limitations in speech and ring mode.

Other advantages

- Adapted to every kind of earphone transducer.
- Mute in emission and reception.
- PABX position.
- Two keys roll over provided.
- Adjustable output tone level.
- Click free switch over from speech to dialing mode & vice-versa.

BIPOLAR

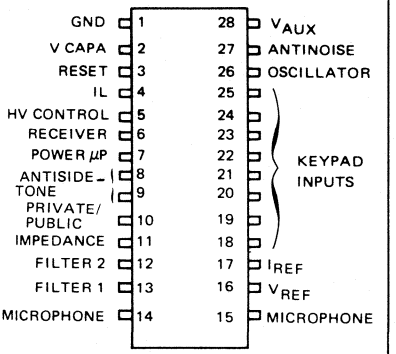
CASE
CB-132



DP SUFFIX
PLASTIC PACKAGE

Also available in SO package
(FP SUFFIX)

PIN ASSIGNMENT



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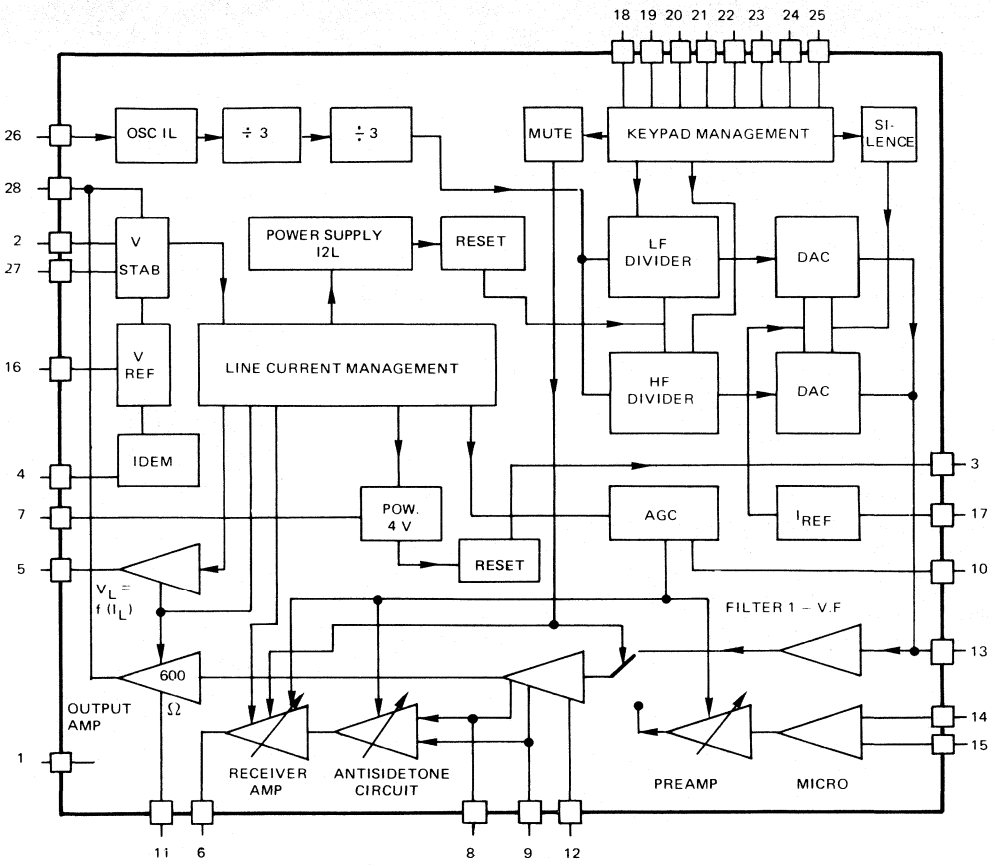
BLOCK DIAGRAM



PIN DESCRIPTION

Name	No.	Description
G_{ND}	1	Ground
V_{capa}	2	C7: voltage stabilizer filtering capacity
Reset	3	Microprocessor reset
I_L	4	R17/C6 sets call frame width
H_V control	5	Output controlling H_V stage
Receiver	6	Receiver output
Power µp	7	Stabilized power for peripheral circuits
Antisidetone	8	Antisedone network input for long lines (3.5 km)
	9	Antisedone network input for short lines (0.5 km)
Private/public	10	Gain control inhibition with respect to line length
Impedance	11	R7 sets dynamic impedance
Filter 2	12	Second filter input for voice frequencies
Filter 1	13	First filter input for voice frequencies
Microphone	14-15	Microphone
V_{ref}	16	Reference voltage
I_{ref}	17	R9 sets internal source reference current
Keypad inputs	18	"D" 941 Hz logic input
	19	"C" 852 Hz logic input
	20	"B" 770 Hz logic input
	21	"A" 697 Hz logic input
	22	"E" 1209 Hz logic input
	23	"F" 1336 Hz logic input
	24	"G" 1477 Hz logic input
	25	"H" 1633 Hz logic input
Oscillator	26	Oscillator input
Antinoise	27	C8 decreases line noise level
V_{aux}	28	V_{CC}: low voltage line

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{cse}	8.5	V
Power dissipation	P_{tot}	800	mW
Operating temperature range	T_{oper}	-25 to 65	°C
Storage temperature range	T_{stg}	-55 to 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$

Characteristic		Symbol	Min	Typ	Max	Unit
Stabilized voltage (note 1)	(pin 2)	V_C				
IL = 28 mA			2.6	2.8	2.95	V
Charging current		Idem	—	2.6	—	mA
Line current regulation for HV control	(pin 5)	Ir				
Pin 4 and pin 2 at 0 volt						
IL = 150 mA			150	—	—	μA
IL = 100 mA			—	—	5	μA
Pin 4 ON/pin 2 at 0 volt						
IL = 75 mA			150	—	—	μA
Pin 4 and pin 2 ON						
IL = 60 mA			150	—	—	μA
IL = 16 mA			—	—	100	nA
28 mA < IL < 50 mA			0.9	1	1.1	μA/mA
Internal bias current (note 1)	(pin 28)	I_{int}				
Vpin28 = R6 X I_{int} + V_C						
Width R9 = 16.2 K (1 %)						
IL = 28 mA			470	510	550	μA
Reference voltage	(pin 16)	Vref				
IL = 28 mA			1.35	1.42	1.49	V
Available current		Iref				
IL = 28 mA			-10	—	100	μA
Stabilized power supply (note 2)	(pin 7)					
Stabilized voltage		V_{mp}	3.8	4	4.2	V
Charging current		I_{cmp}				
Pin 4 and pin 2 at 0 volt						
IL1 = IL — Idem			0.7	—	—	IL1
Available current						
IL = 6 mA		I_{smp}	0.5	—	—	mA
IL > 25 mA			3.15	3.5	—	mA
IL > 25 mA + AC			1.6	1.75	—	mA
Internal consumption		I_{imp}	90	110	130	μA
Reset microprocessor (note 2)	(pin 3)					
High threshold		V_{rh}	0.82	0.85	0.88	Vpin7
Low threshold		V_{rb}	0.745	0.775	0.805	Vpin7
Output voltage	Reset = 1	V_{rsh}	0.9	—	—	Vpin7
	Reset = 0	V_{rsb}	—	—	0.1	Vpin7

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, F = 1 kHz, RL = 600 ohms

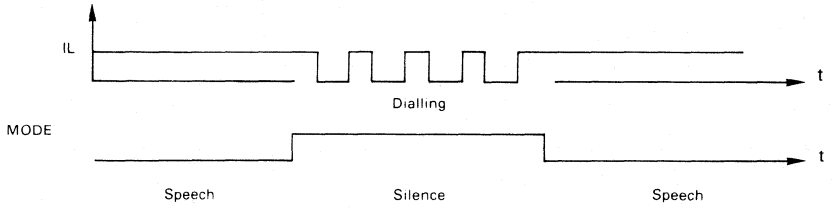
Characteristic	Symbol	Min	Typ	Max	Unit
Transmission (note 3)					
Gain IL = 28 mA	G_{el}	54	55	56	dB
IL = 44 mA	G_{ec}	47	49	51	dB
Distortion IL = 28/44 mA	De				
VL = 4.5 dBm		—	—	3	%
VL = 6 dBm		—	—	10	%
Microphone input impedance in symmetric mode	Ze	1.82	2.15	2.47	kohms
Psophometric noise 2 kohms across microphone inputs IL > 28 mA	B_{ep}	—	—69	—	dBmp
Signal attenuation in V.F. and silence mode IL > 28 mA	Re	60	—	—	dB
C.M.R.R.		—	60	—	dB
Reception (note 4)					
Gain IL = 28 mA	G_{rl}	28.5	29.5	30.5	dB
IL = 44 mA	G_{rc}	21.5	23.5	25.5	dB
Distortion IL = 28/44 mA	Dr	—	—	—	—
Vec = 500 mV		—	—	3	%
Vec = 700 mV		—	—	10	%
Noise IL = 28/44 mA Rec = 600 ohms	B_{rp}	—	—74	—	dBmp
Antisidetone (note 5)					
Efficiency IL = 28 mA	G_{al}	22	—	—	dB
IL = 44 mA	G_{ac}	26	—	—	dB
Impedance (note 6)					
IL > 28 mA	Z_{ac}	500	650	800	ohms

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, RL = 600 ohms

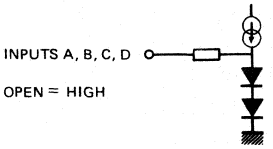
Characteristic	Symbol	Min	Typ	Max	Unit
Voice frequency generator (note 7)					
Quartz 3.579545 MHz		—	—	—	—
Frequency dispersion	D_{fv}	— 0.5	—	0.5	%
Low frequency level (set by external devices)	N_{fb}	— 11	—	— 6	dBm
High frequency level (set by external devices)	N_{fh}	— 9	—	— 4	dBm
Output level dispersion	D_{nfv}	— 2	—	+ 2	dB
Preemphasis FVH/FVB	P_{fv}	+ 1	+ 2	+ 3	dB
Distortion (harmonic level up to 1 MHz less than amplitude (Appendix 1))					
Voice frequency monitoring	C_{fv}	28	35	42	dB
Logic inputs					
A, B, C, D					
Open = high					
Current to be drawn to set one of these inputs to low level	I_{fb}	10	—	60	µA
E, F, G, H					
Open = low					
Current to be absorbed to set one of these inputs to high level	I_{fH}	10	—	—	µA
Input impedance					
A, B, C, D, E, F, G	Z_{fv}	—	5	—	kohms
H	Z_h	—	2.5	—	kohms

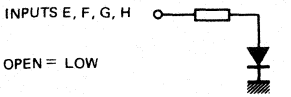
In pulse dialling the receiver mute is the silence mode.



FUNCTIONAL DESCRIPTION

- Logic inputs equivalent diagrams





Inputs								Voice Frequencies (Hz)	Symbol	Mute	Notes
A	B	C	D	E	F	G	H				
H	H	H	H	L	L	L	L	–	–	off	15
L	H	H	H	L	L	L	L	697	–	on	16
H	L	H	H	L	L	L	L	770	–	on	
H	H	L	H	L	L	L	L	852	–	on	
H	H	H	L	L	L	L	L	941	–	on	
H	H	H	H	H	L	L	L	1 209	–	on	17
H	H	H	H	L	H	L	L	1 336	–	on	
H	H	H	H	L	L	H	L	1 447	–	on	
H	H	H	H	L	L	L	H	1 633	–	on	
L				H				697 + 1 208	"1"	on	18
L					H			697 + 1 336	"2"	on	
L						H		697 + 1 477	"3"	on	
L							H	697 + 1 633	"A"	on	
	L			H				770 + 1 209	"4"	on	
	L				H			770 + 1 336	"5"	on	
	L					H		770 + 1 477	"6"	on	
	L						H	770 + 1 633	"B"	on	
		L		H				852 + 1 209	"7"	on	
		L			H			852 + 1 336	"8"	on	
		L				H		852 + 1 477	"9"	on	
		L					H	852 + 1 633	"C"	on	
			L	H				941 + 1 209	"*"	on	
			L		H			941 + 1 336	"0"	on	
			L			H		941 + 1 477	"#"	on	
			L				H	941 + 1 633	"D"		

Note 15: Conversation mode.

Note 16: Test mode.
Low frequencies.

Note 17: Test mode.
High frequencies.

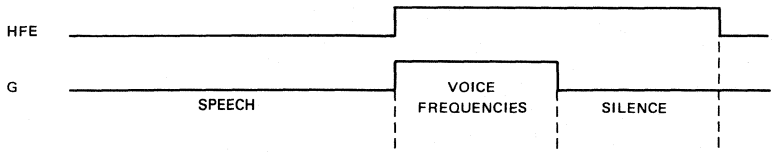
Note 18: If one of inputs E,F,G,H, is high, the others are low.
If one of inputs A,B,C,D, is low, the others are ligh.

LOGIC TABLE - MICROPROCESSOR MODE

Inputs								Voice Frequencies (Hz)	Symbol	Mute	Notes
A	B	C	D	E	F	H	G				
H	H	H	H		L		L	–	–	off	19
X	X	X	X		H		L	–	–	on	20
H	H	H	H		H		H	697 + 1 209	"1"	on	
H	H	H	L		H		H	697 + 1 336	"2"	on	
H	H	L	H		H		H	697 + 1 477	"3"	on	
H	H	L	L		H		H	697 + 1 633	"A"	on	
H	L	H	H		H		H	770 + 1 209	"4"	on	
H	L	H	L		H		H	770 + 1 336	"5"	on	
H	L	L	H		H		H	770 + 1 477	"6"	on	
H	L	L	L		H		H	770 + 1 633	"B"	on	
L	H	H	H		H		H	852 + 1 209	"7"	on	
L	H	H	L		H		H	852 + 1 336	"8"	on	
L	H	L	H		H		H	852 + 1 477	"9"	on	
L	H	L	L		H		H	852 + 1 633	"C"	on	
L	L	H	H		H		H	941 + 1 209	"*"	on	
L	L	H	L		H		H	941 + 1 336	"0"	on	
L	L	L	H		H		H	941 + 1 477	"#"	On	
L	L	L	L		H		H	941 + 1 633	"D"	on	

Note 19: Conversation mode.

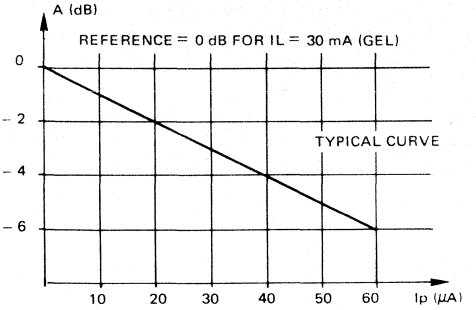
Note 20: Silence setting.



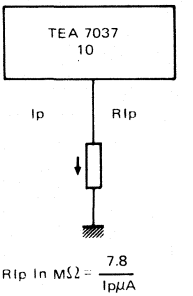
Pin 10: When a resistor is inserted between pin 10 and ground, the transmission and receiving efficiency control and antisidetone variation are inhibited with respect to line current.

The transmission and receiving gains may vary from G_{max}(gel) to G_{max} — 6 dB (Gec) with respect to the resistance value.
The equivalent antisidetone is related to the gain set by RI_p.

TRANSMISSION AND RECEIVING GAIN ATTENUATION



CONSUMPTION ON PIN 10

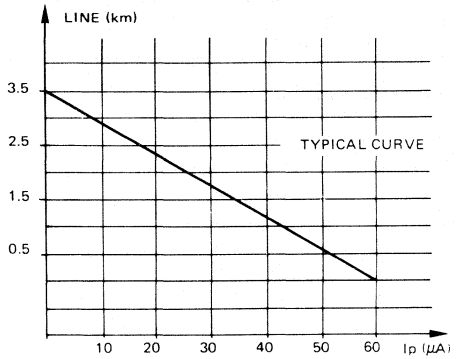


$$RIp\ in\ M\Omega = \frac{7.8}{Ip\mu A}$$

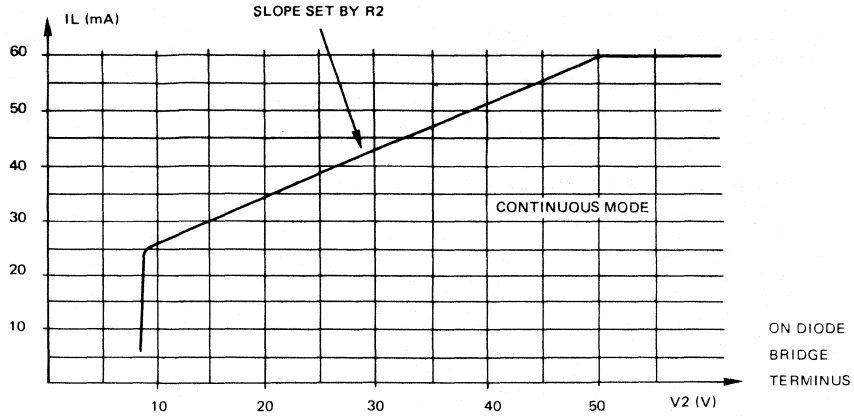
FOR RIp = 390 K TO 1 %

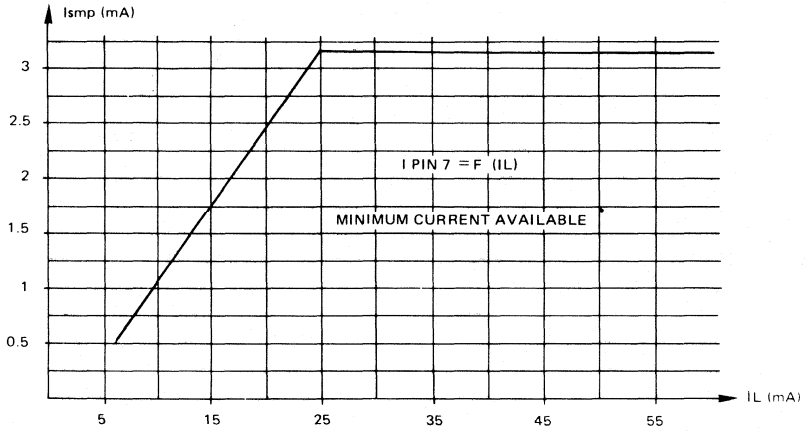
$\Delta G = -2\ dB \pm 0.4\ dB$

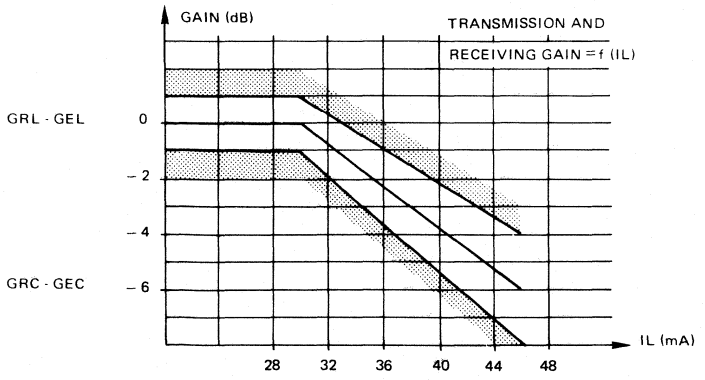
EQUIVALENT ANTILOCAL NETWORK



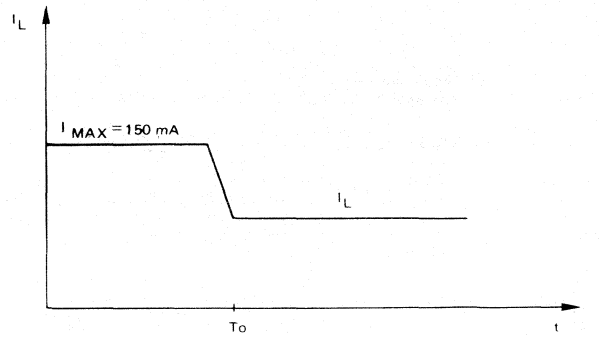
CONSUMPTION ON PIN 10


IL (mA)
SLOPE SET BY R2
60
50
40
30
20
10
CONTINUOUS MODE
ON DIODE
BRIDGE
TERMINUS
10
20
30
40
50
V2 (V)


Ismp (mA)
3
2.5
2
1.5
1
0.5
I PIN 7 = F (IL)
MINIMUM CURRENT AVAILABLE
5
15
25
35
45
55
IL (mA)


GAIN (dB)
TRANSMISSION AND
RECEIVING GAIN = f (IL)
GRL - GEL
0
– 2
– 4
GRC - GEC
– 6
28
32
36
40
44
48
IL (mA)

POWERING



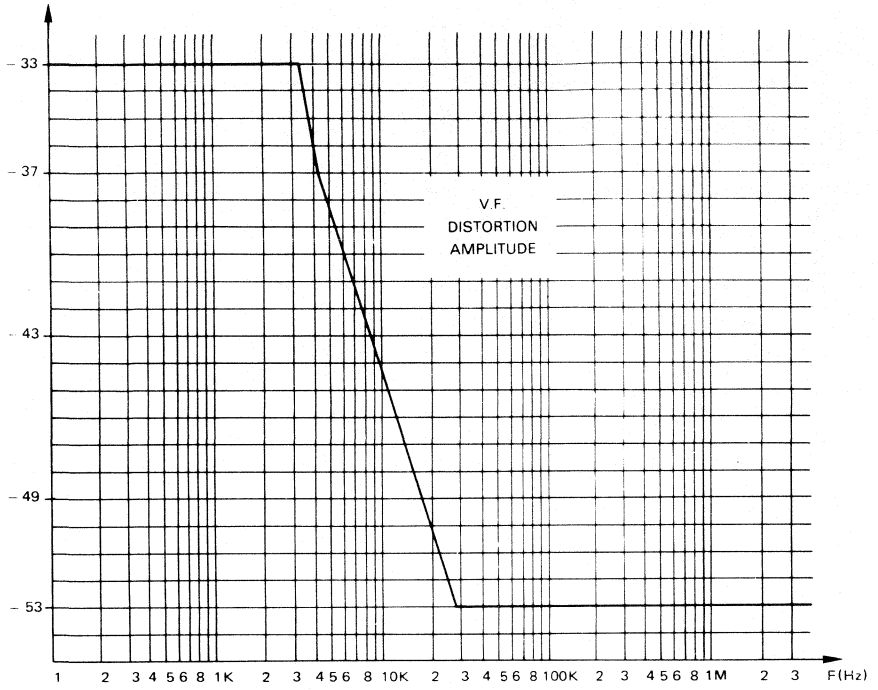
TO IS SET BY : R17.C6 (PIN 4) OR C7 (PIN 2)

The TEA7037 can support the capacitive loads an all its pins, except pin 26 (oscillator).

It is obvious that these capacities can change the circuits alternating and/or transient behavior.

Pin	Name	Max. value (grounded)	Comments
1	Ground		
2	V capa	220 µF	
3	Reset	470 µF	
4	I_L = 120 or 60 mS	2.2 µF	
5	H_V control	Few nF max.	In parallel with the capacitor across pin 28 and pin 1, hence changes impedance & circuit time constants
6	Receiver	100 nF max.	In parallel on the receiver
7	Pow. µP	470 µF	
8	Anti local	10 nF	Receiver signal filter
9			
10	Private/ public	47 nF	
11	Impedance	33 pF max.	Provides a high pass, hence increases DTMF harmonics & noise above cut-out frequency
12	Filter 2	Few pF max.	Changes refilter impedance & time CS[t]
13	Filter 1	82 nF	Should not be changed (preemphasis)
14			
15	Microphone	100 nF	
16	V_{REF}	10 µF	
17	I_{REF}	680 pF max.	
18			
19			
20			
21	Keyboard inputs	10 nF max.	Bear time constants in mind
22			
23			
24			
25			
26	Oscillator	NO	
27	Antinoise	2.2 nF	
28	Vaux	Few nF	Cf. comment pin 5

APPENDIX 1


- 33
- 37
- 43
- 49
- 53
V.F.
DISTORTION
AMPLITUDE
1 2 3 4 5 6 8 1K 2 3 4 5 6 8 10K 2 3 4 5 6 8 100K 2 3 4 5 6 8 1M 2 3 F(Hz)

COMPONENTS VALUES

R1	10 ohms		C1	= 2.2 nF	
R2	1.2 Mohms		C2	= 4.7 nF	
R3	100 kohms		C3	= 1 nF	
R4	4.7 Mohms		C4	= 100 µF	
R5	220 kohms		C5	= *	
R6	5.9 kohms		C6	= *	
R7	*		C7	= *	
R8	*		C8	= *	
R9	16.2 kohms		C9	= ⩽ 1 µF	
R10	*		C10	= ⩽ 1 µF	(depending on uP)
R11	*		C11	= 68 nF	
R12	*		C12	= 1 µF	
R13	*		C13	= 6.8 nF	
R14	220 kohms		C14	= 3.3 µF	
R15	845 ohms		C15	= 2.2 nF	
R16	220 ohms		C16	= 2.2 nF	
R17	820 kohms		C17	= 10 µF	
R18	75 ohms		C18	= 2.2 µF	
RIP	= 390 kohms		C19	= 470 nF	
RuP	= 5.6 kohms				
Zec	= 220 ohms		D1	: ZENER 15 V	
			D2	: BAT43	
T1	: MJE340		D3	: BAT43	
T2	: PBF259				
T3	: PBF493S		QUARTZ	: 3.58 MHz	

- ZL = 600 ohms

-R7	= 0	-C5	= 27 pF
-R8	= 124 kohms	-C6	= 1 nF
-R10	= 0	-C7	= 27 pF
-R11	= 124 kohms	-C8	= 1 nF
-R12	= 3.9 kohms		
-R13	= 3.9 kohms		

- 0.4 mm France cable varying between 0 km and 3.5 km

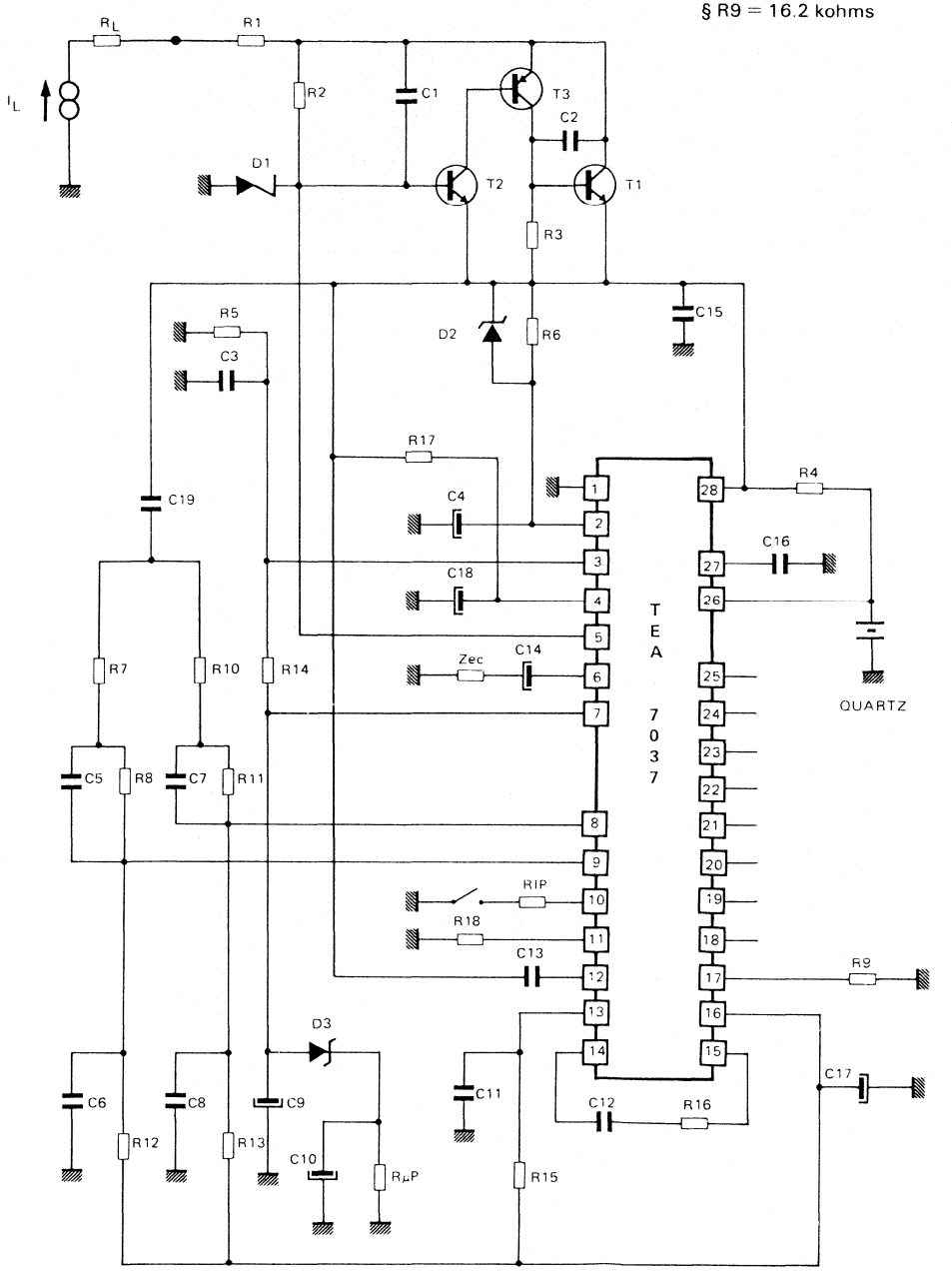
-R7	= 56 kohms	-C5	= 560 pF
-R8	= 124 kohms	-C6	= 4.7 nF
-R10	= 10 kohms	-C7	= 100 pF
-R11	115 kohms	-C8	= 2.2 nF
-R12	4.99 kohms		
-R13	3.6 kohms		

- R12 and R13 enable reception gain adjustment for adaptation to various transducers.
- R16 enable transmission gain equipment for adaptation to various transducers.

NOTE 1.a
V_C, I_{int}, Vref

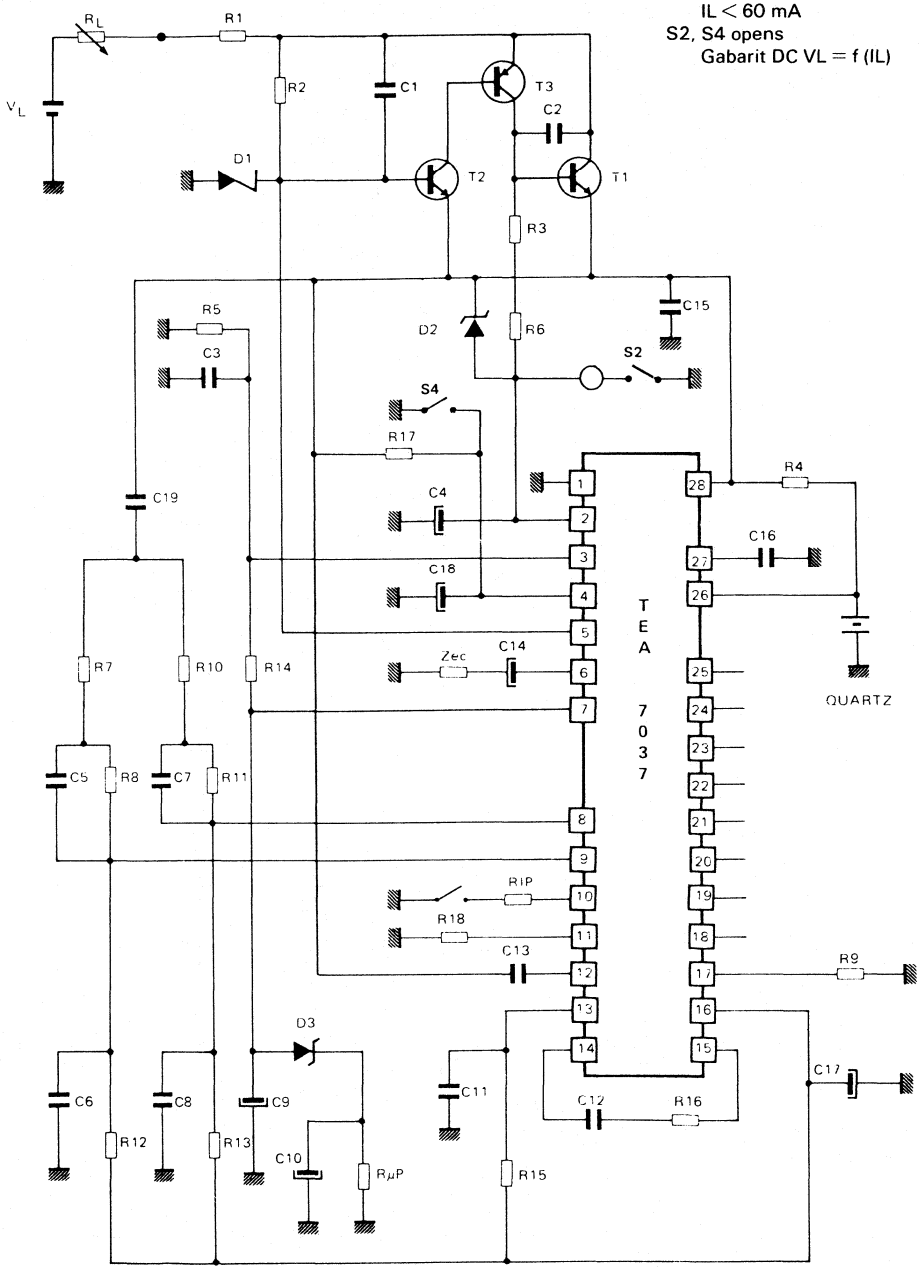
$$I_{int} = \frac{Vpin28\text{-}Vc}{R6}$$

Width § R6 = 5.9 kohms
§ R9 = 16.2 kohms



NOTE 1.b
Idem, Ir

S2, S4 closes
Idem, IL < 150 mA
S2 close, S4 open
IL < 75 mA
S2 open, S4 close
IL < 60 mA
S2, S4 opens
Gabarit DC VL = f (IL)

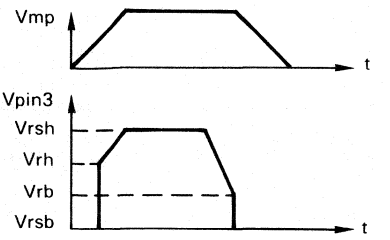


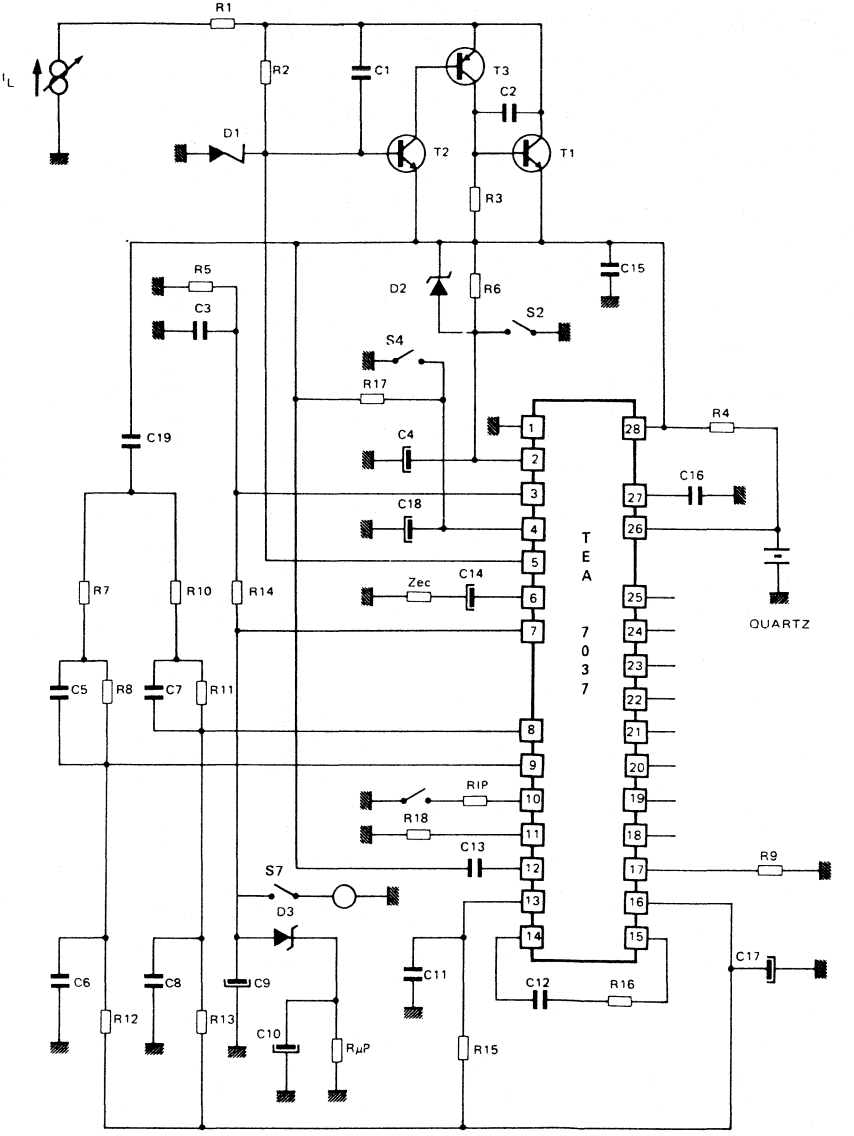
NOTE 2
Icmp, Vmp, Ismp, Iimp
Vrh, Vrb, Vrsh, Vrsb

S2, S4, S7 closes
Icmp
S2, S4, S7 opens
Vmp, Ismp

Iimp by the time discharge of C9 when the line power is cut off.

Reset microprocessor



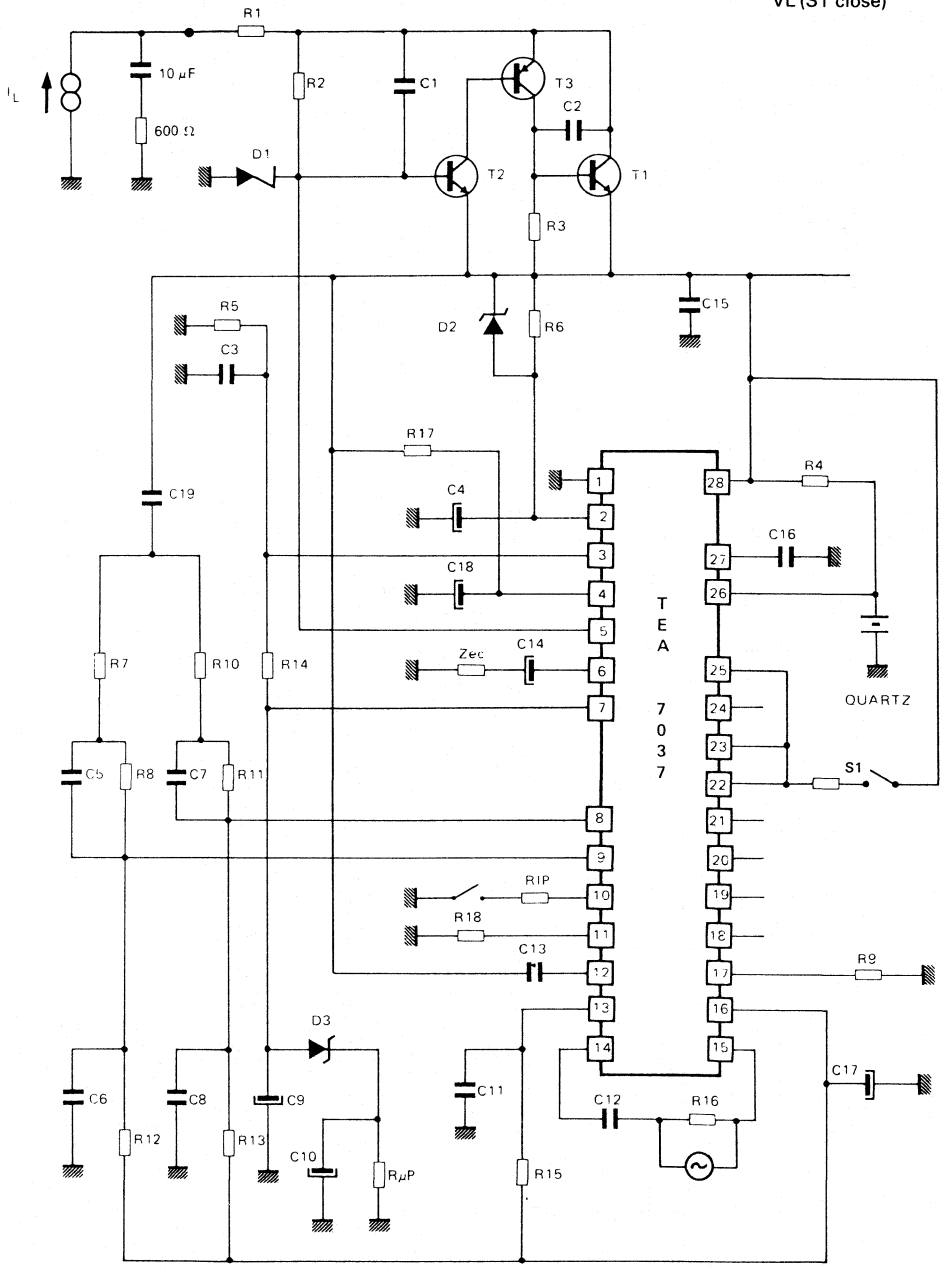


NOTE 3
Gel, Gec, Re, De, Bep

S1 open

$(Gel, Gec) = 20 \log \frac{VL}{VM}$

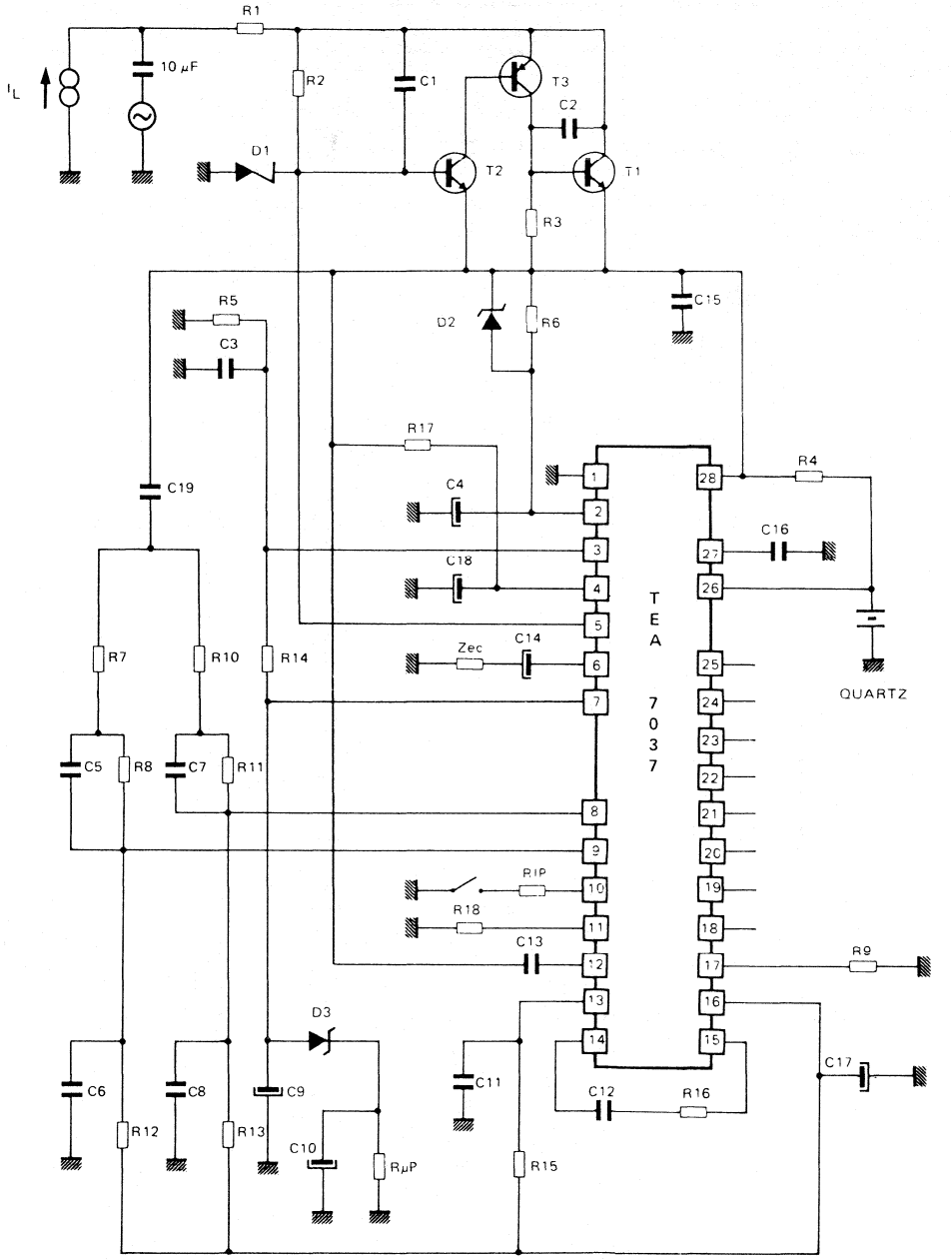
$Re = 20 \log \frac{VL\ (S1\ open)}{VL\ (S1\ close)}$



NOTE 4
Grl, Grc, Dr, Brp

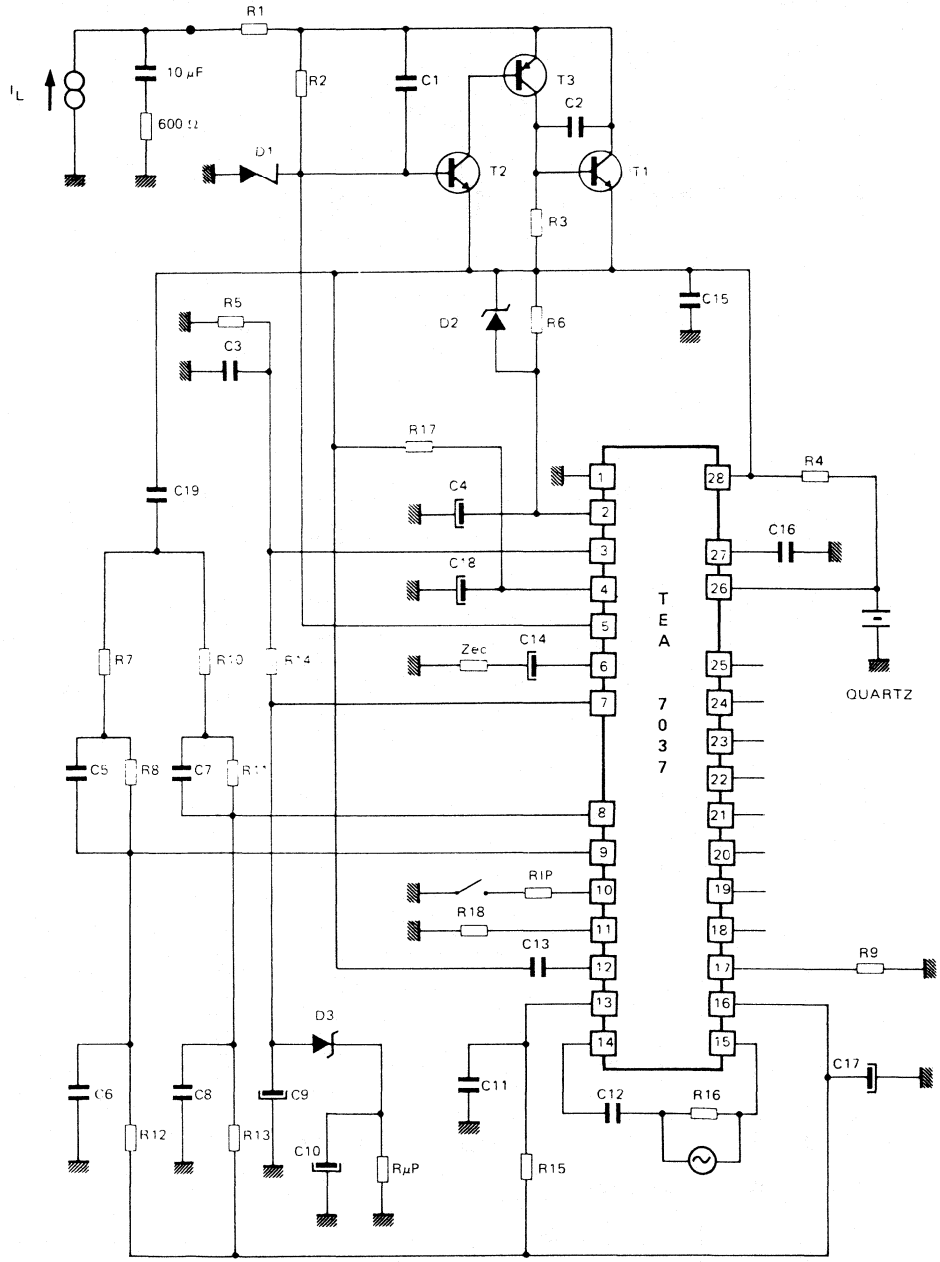
$$Grl = 20 \log \frac{Vpin6}{Vpin8}$$

$$Grc = 20 \log \frac{Vpin6}{Vpin9}$$



NOTE 5
Gal, Gac

$$(Gal, Gac) = 20 \log \frac{Vpin28}{Vpin6}$$



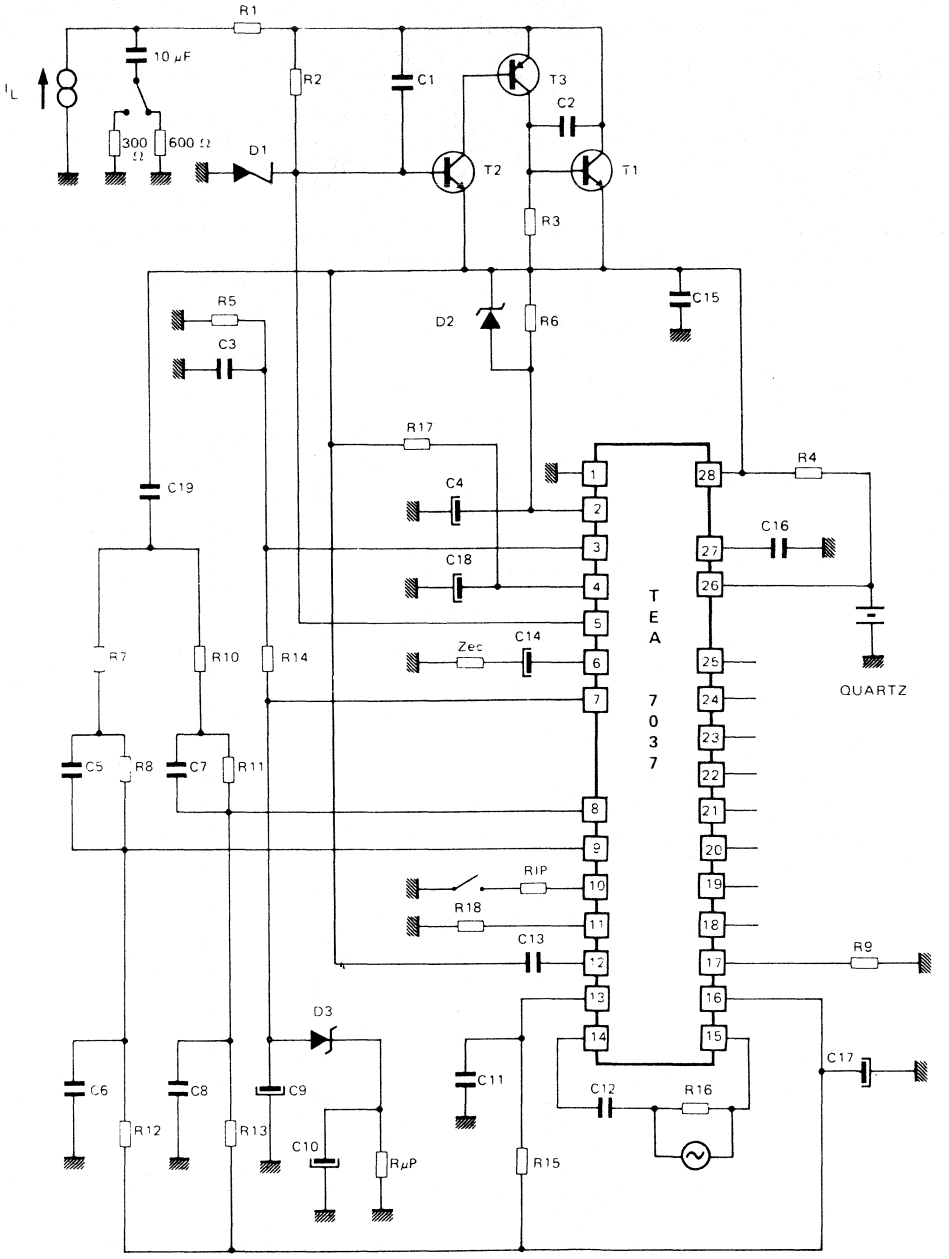
NOTE 6

Zac

$$Zac = RL1 \times RL2 \frac{VL2-VL1}{VL1 \times RL2-VL2 \times RL1}$$

-VL1 for RL1 = 300 ohms
-VL2 for RL2 = 600 ohms

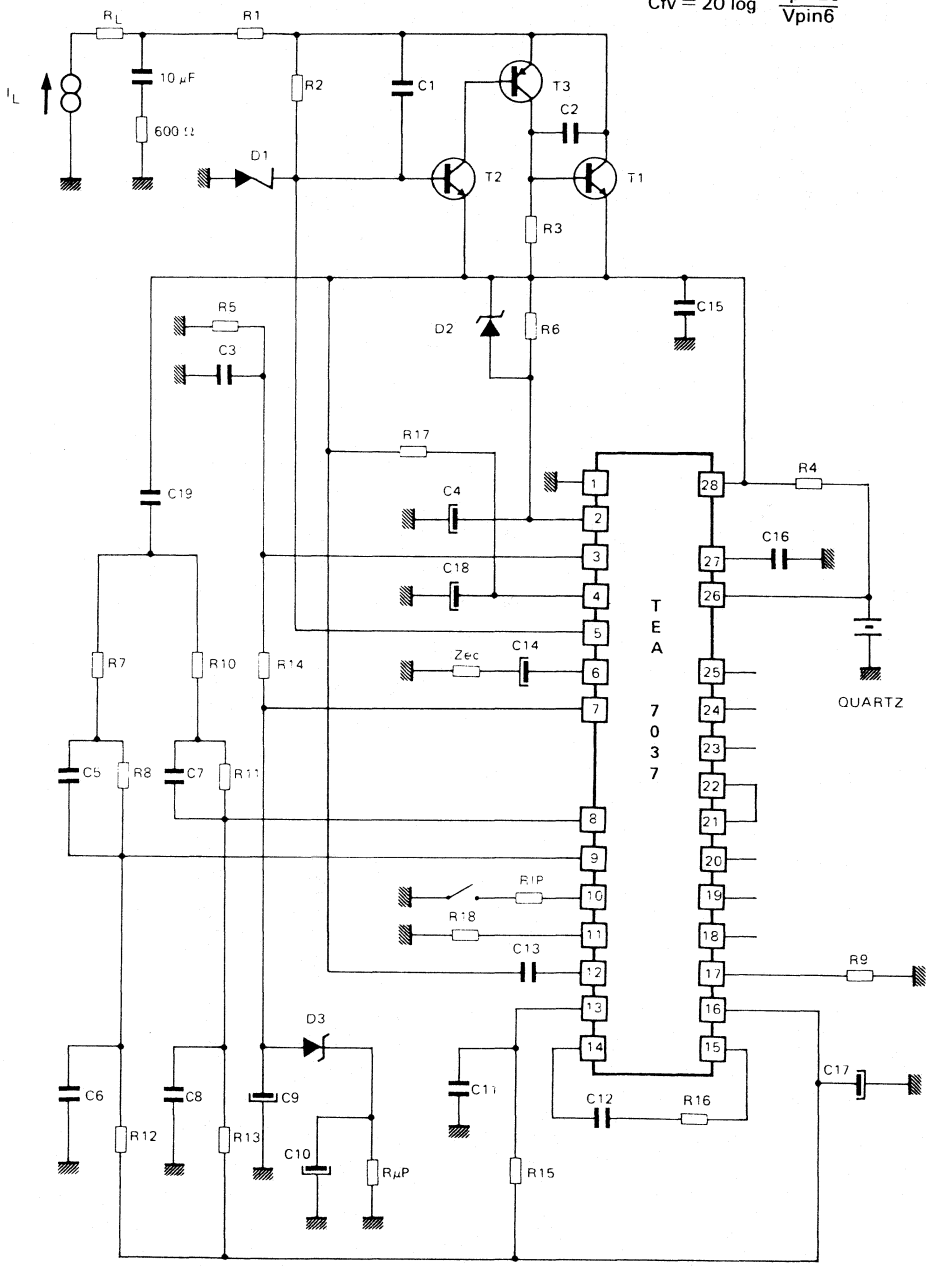
$$Zac = 600 \times \frac{VL2-VL1}{2VL1-VL2}$$



NOTE 7
Nfb, Nfh, Pfv, Cfv

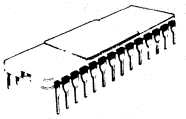
697 Hz + 1209 Hz
Level and preemphasis are measured on pin 28

$$Cfv = 20 \log \frac{Vpin28}{Vpin6}$$

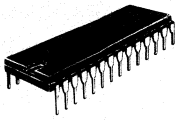


PHYSICAL DIMENSIONS

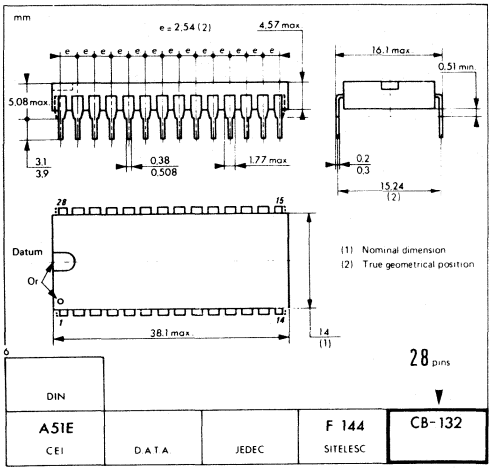
CB-132



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



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Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSTEA7037

HOMSON COMPONENTS
EMICONDUCTEURS

TEA7050

SPEECH FOR HIGH RANGE TELEPHONE SETS

PRODUCT PREVIEW

Specially designed for telephone applications this 28 pins IC provides:

- Transmission and line adaptation.
- Power supply for peripherals and loudspeaker.
- Interface with MCU.

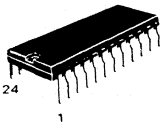
It meets the French specification for handset homologation level 2 and 3.

Major advantages

- Background noise elimination by microphone amplifier threshold (carbon micro like).
- Power supply management and adaptation to line current.
- Overvoltage protection of whole application provided by IC.
- Automatic line length receiving and sending gain control.
- Automatic line length tracking antisidetone system.
- Adjustable microphone and earphone amplifier gain.
- High input impedance.
- PABX position.

BIPOLAR

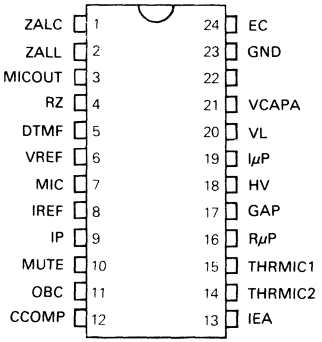
CASE
CB-68



DP SUFFIX
PLASTIC PACKAGE

Also available in SO package
(FP SUFFIX)

PIN ASSIGNMENT



SEPTEMBER 1986 1/5

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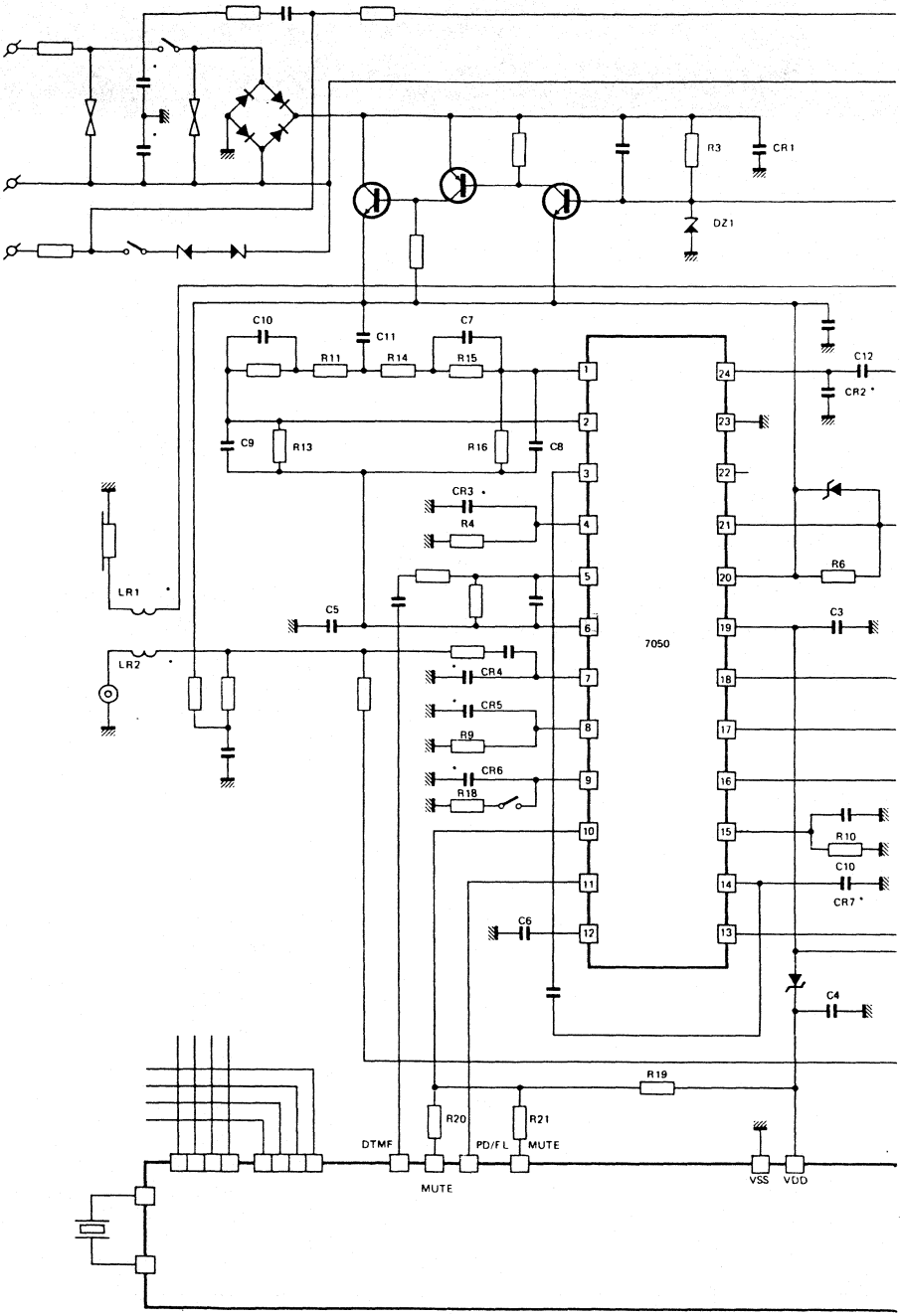
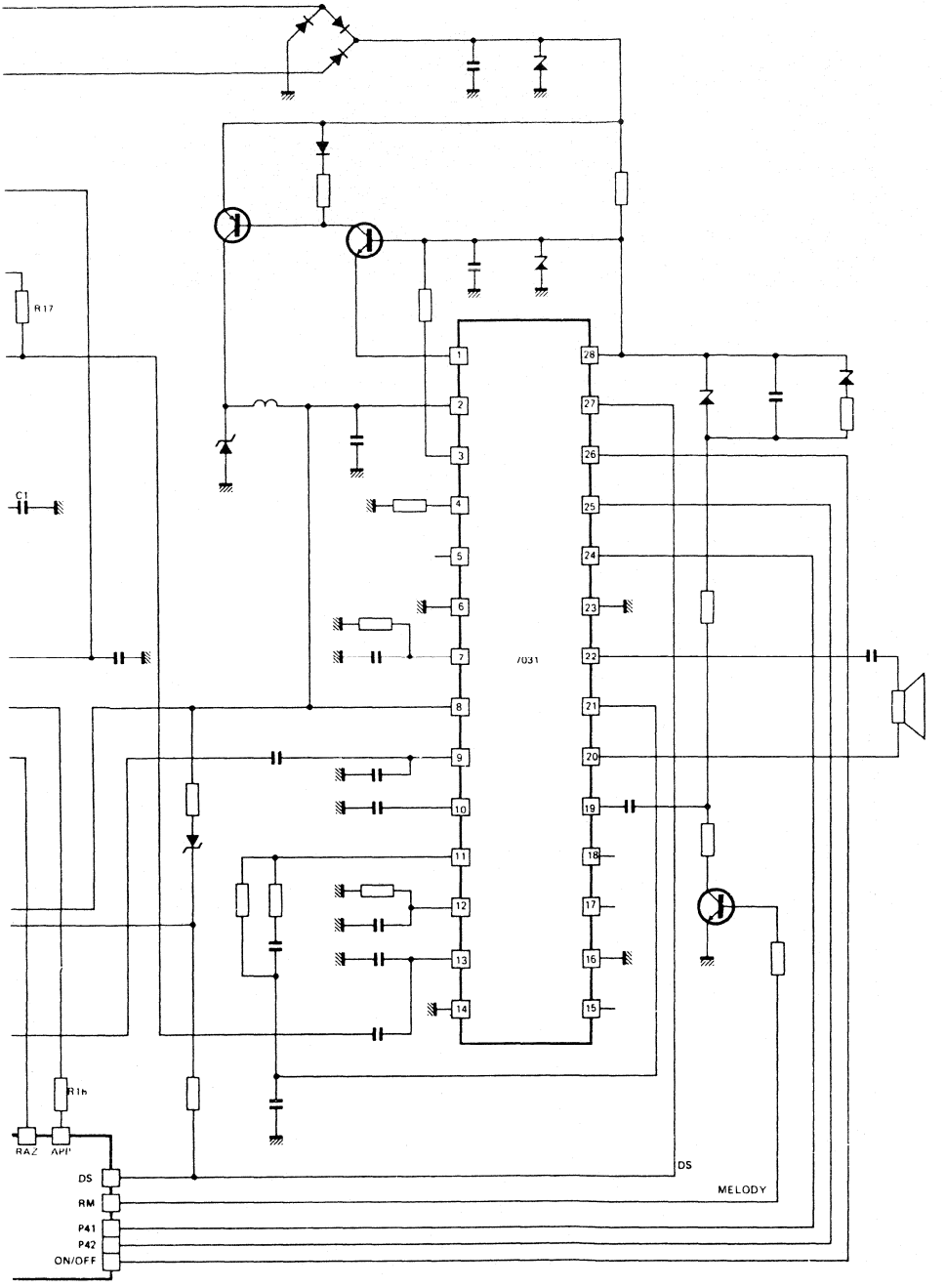
APPLICATION DIAGRAM

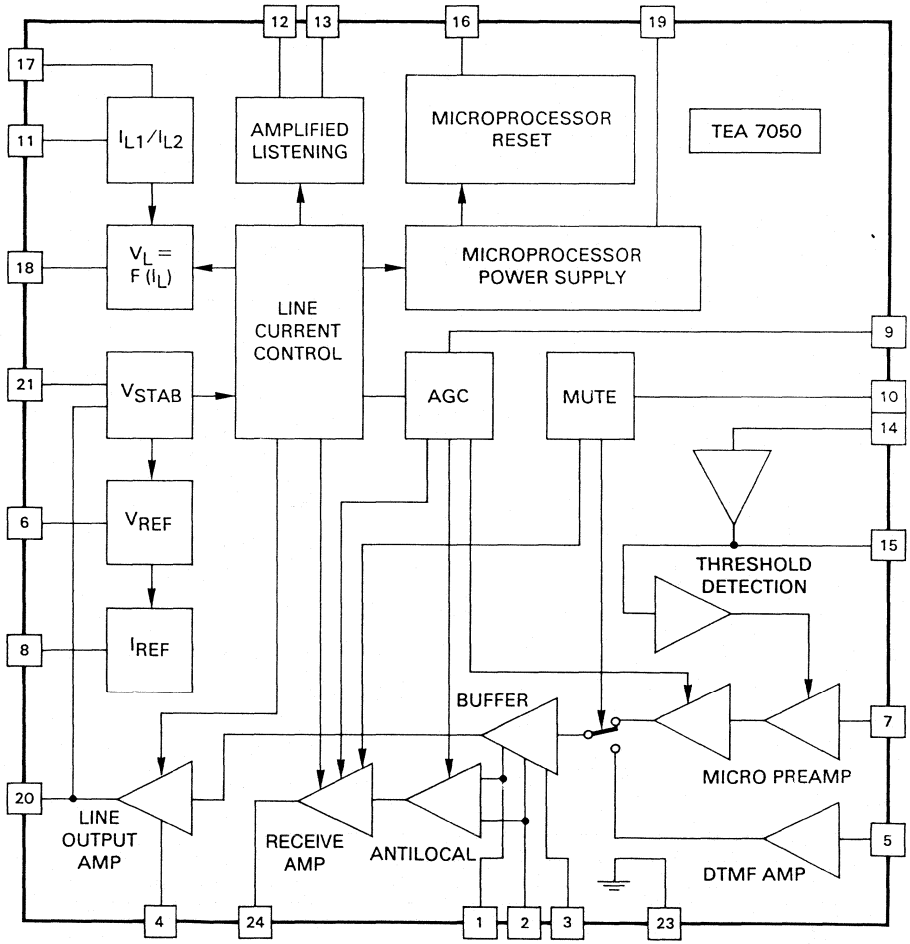




* COMPOSANTS POUR PROTECTIONS RADIO

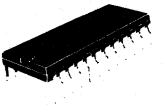
TRANSMISSION CIRCUIT FOR HIGH AND MEDIUM TECHNOLOGY TELEPHONE SETS

1 — ANTILOCAL LC
2 — ANTILOCAL LL
3 — AMPLIFIED TRANSMISSION
4 — IMPEDANCE
5 — DTMF INPUT
6 — V_{REF}
7 — MICROPHONE INPUT
8 — I_{REF}
9 — PRIVATE/PUBLIC
10 — MICRO MUTE/MICRO EARPHONE
11 — DECIMAL DIALLING INPUT
12 — AMPLIFIED LISTENING COMPENSATION
24 — EARPHONE
22 —
23 — GROUND
21 — V_{CAPA}
20 — V_{LINE}
19 — MICROPROCESSOR POWER SUPPLY
18 — HV STAGE CONTROL
17 — HOOK DETECTION
16 — MICROPROCESSOR RESET
15 — MICROPHONE THRESHOLD
14 — MICROPHONE THRESHOLD ADJUSTMENT
13 — I FOR AMPLIFIED LISTENING

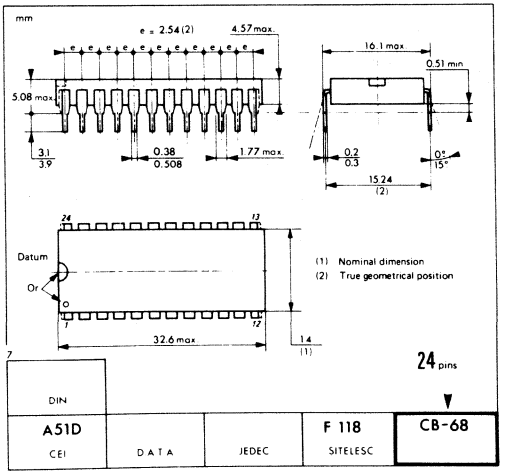


PHYSICAL DIMENSIONS

CB-68



PLASTIC PACKAGE



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HOMSON
COMPONENTS
MICONDUCTEURS

TS7650

DIGITAL TELEPHONE CODEC/FILTER

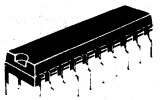
PRODUCT PREVIEW

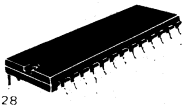
CMOS

MAIN FEATURES:

- CODEC + filter function (similar to ETC5054/ETC5057)
- A-law and μ-law (software selectable)
- Single 5 volts supply power consumption 40 mW typical
- Low power standby mode
- Analog interface for handset and handfree
- Programmable analog receive and transmit gain
- Ring and tone generation included
- DTMF auxiliary input
- Serial MPU interface
- Loudspeaker amplifier auxiliary output
- Transient suppression at speech/dialing switching
- Analog and digital loopback
- Micro-processor selection of B1 or B2 channel for digital data interface
- Automatic gain control allowing for hand-free operation
- 20 pin/28 pin plastic package

CASES





March 1987-1/4

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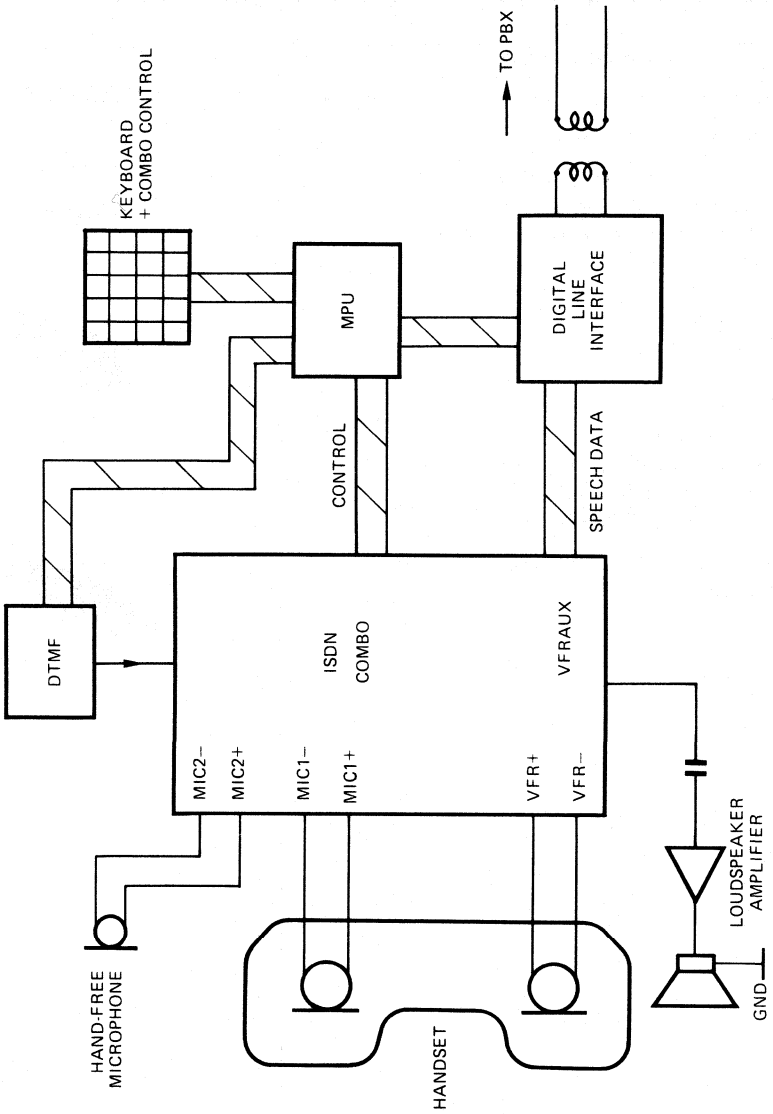
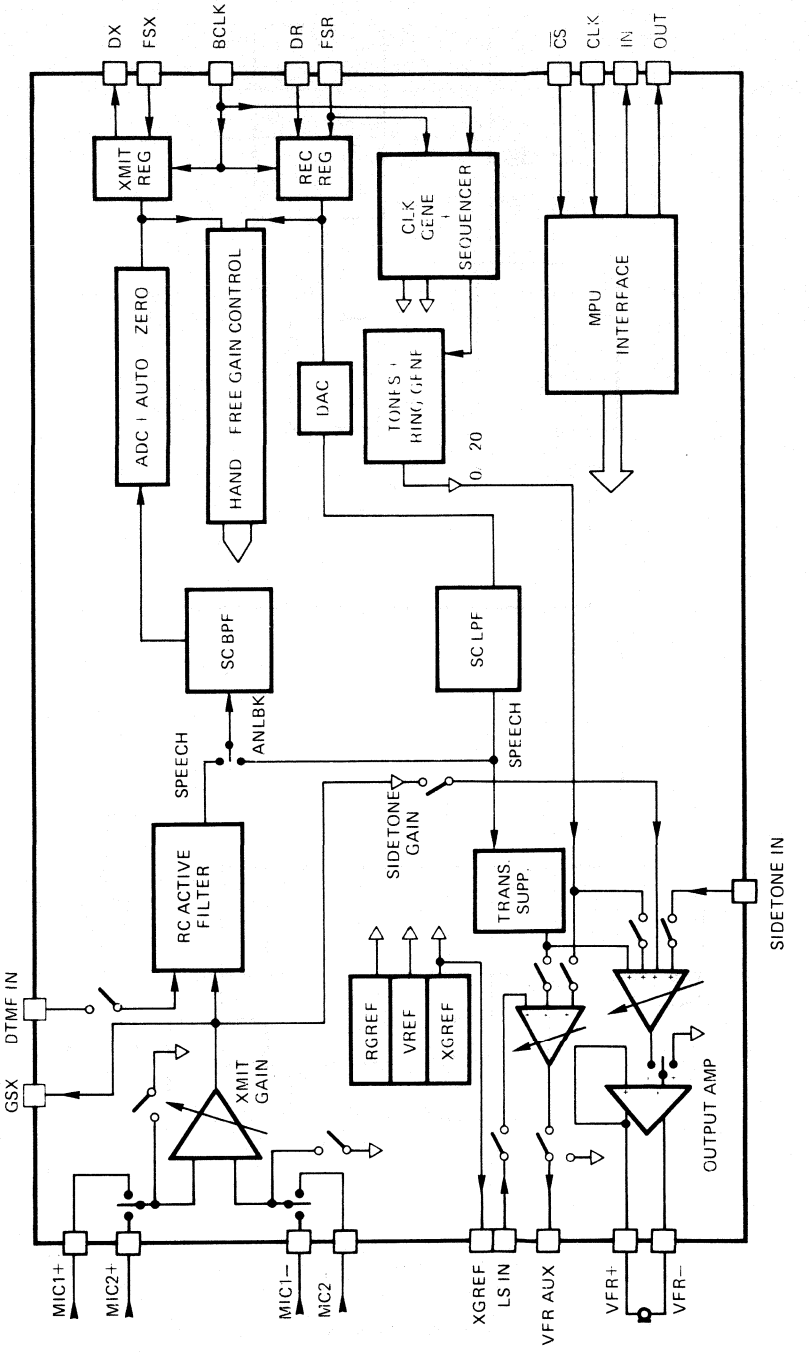
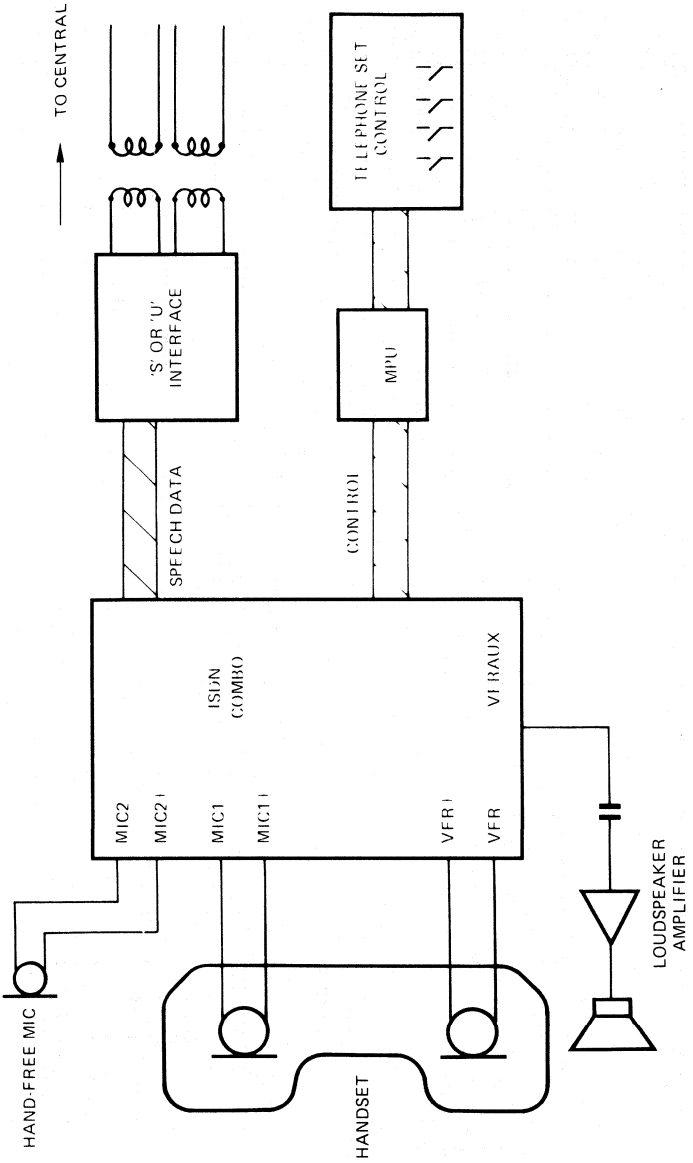
TELEPHONE SET WITH DIGITAL LINE TRANSCEIVER



ISDN COMBO


DX
FSX
BCLK
DR
FSR
CS
CLK
IN
OUT
XMIT REG
REC REG
CLK GENE + SEQUENCER
MPU INTERFACE
ADC + AUTO ZERO
HAND FREE GAIN CONTROL
DAC
TONES + RING GENE
0 20
SC BPF
SC LPF
SPEECH
ANLBK
SPEECH
SIDETONE GAIN
RC ACTIVE FILTER
TRANS. SUPP.
SIDETONE IN
DTMF IN
GSX
RGREF
VREF
XGREF
XMIT GAIN
OUTPUT AMP
MIC1+
MIC2+
MIC1−
MIC2
XGREF
LS IN
VFR AUX
VFR+
VFR−

DIGITAL TELEPHONE WITH "S" OR "U" INTERFACE



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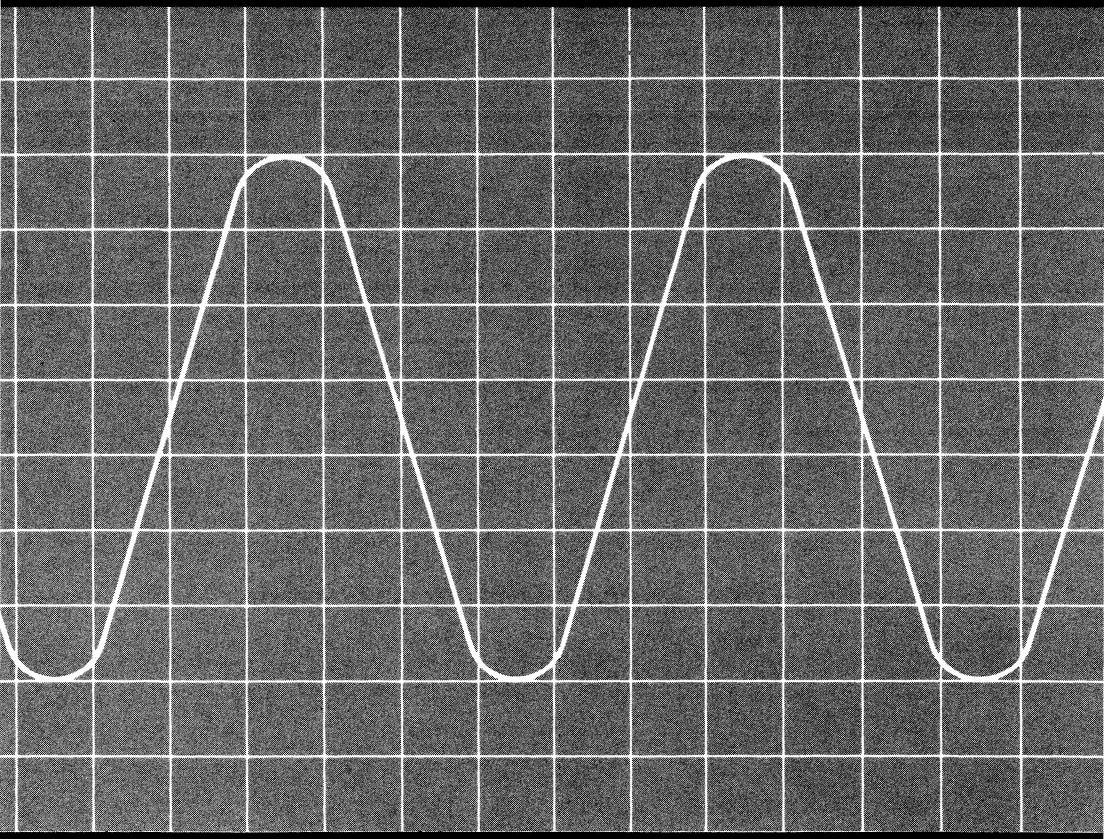
Printed in France

Ref. DSTS7650

TEA 3046
TELEPHONE LOW COST MONOCHIP

APPLICATION NOTE AN-055

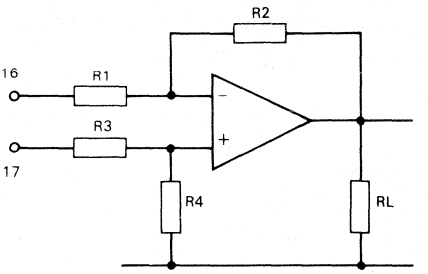


THOMSON
COMPONENTS
SEMICONDUCTEURS

SPEECH MODE

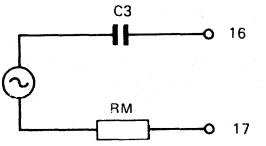
MICROPHONE AMPLIFIER

The microphone amplifier inputs can be driven either in symmetrical or asymmetrical mode. A schematic diagram of the microphone preamplifier is shown below:



For the TEA3046: R1 = R3 = 1 kΩ and R2 = R4 = 6 kΩ

Symmetrical mode



Using the schematic diagram of the preamplifier, the calculation of the preamplifier gain becomes straightforward:

$$G1 = \frac{-R2}{\frac{R_M}{2} + R1}$$

The maximum gain is obtained for $R_M = 0$.

$$G1_{max} = -\frac{R2}{R1}$$

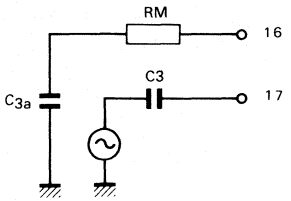
The input impedance is also easy to obtain:

$$Z_{IN} = 2R1$$

For the TEA3046 in symmetrical mode we obtain:

$$G1_{max} = -6 \text{ and } Z_{IN} = 2\ k\Omega$$

Asymmetrical mode



In this case the preamplifier is given by:

$$G1 = -\frac{R2}{R1 + R2}\left(1 + \frac{R2}{R_M + R1}\right)$$

The maximum gain is obtained for $R_M = 0$.

$$G1_{max} = -\frac{R2}{R1}$$

In this case, the input impedance of the preamplifier is:

$$Z_{IN} = R1 + R2$$

For the TEA3046 in asymmetrical mode we obtain:

$$G_{max} = -6 \text{ and } Z_{IN} = 7\ k\Omega$$

We can see that both in asymmetrical and symmetrical modes, the gain of the preamplifier can be decreased by the use of an external resistor R_M.

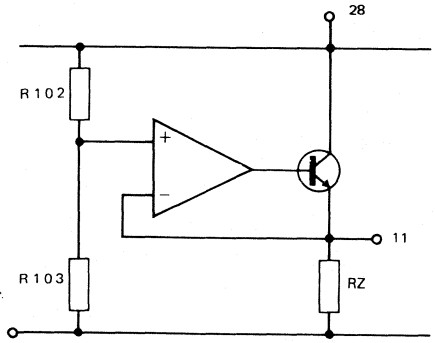
OUTPUT IMPEDANCE

The main part of the circuit impedance is set by the output stage. Also to be included is a parasitic impedance R_p corresponding to all, the other stages of the circuit seen from the line, the protection resistor R_L and the capacitor CF3 connected on the line.

Output stage impedance: Z_{out}

$$Z_{out} = R_Z \frac{R102 + R103}{R103}$$

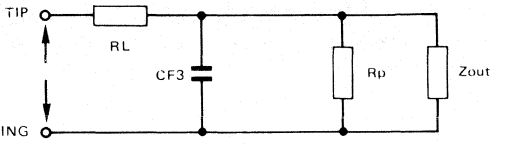
$$\frac{R102 + R103}{R103} = 8.925$$



R102 and R103 are internal resistors hence Z_{out} is set by R_Z.
The application set impedance is given by:

$$Z_{AC} = R_L + (Z_{CF3} // R_p // Z_{out})$$

Equivalent circuit seen from the line



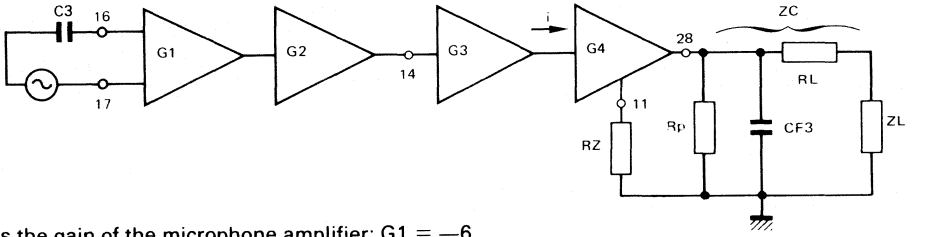
Numerical example:

$R_Z = 75\ \Omega$, $R_L = 12\ \Omega$, CF3 = 10 nF, $R_p = 4\ k\Omega$

$Z_{out} = 670\ \Omega$ and $|Z_{AC}| = 585\ \Omega$ at f = 800 Hz

OVERALL MAXIMUM GAIN

This calculation is done with $R_M = 0$ and inhibited gain control. A schematic representation of the transmission circuit is:



G1 is the gain of the microphone amplifier: G1 = —6.
G2 is the maximum gain of the automatic gain control stage: G2 = —4.
G3 is a transconductance corresponding to the buffer stage: G3 = 1/4 kΩ.

$$i = V14/4\ k\Omega$$

G4 is the transresistance of the output stage:

$$G4 = -K \frac{Z_C}{Z_C + Z_{out}}$$

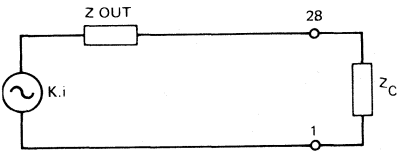
When Z_C represents the impedance seen by the output stage:

$$Z_C = R_p // Z_{CF3} // (Z_L + R_L)$$

and K is a constant defined by internal components:

$$K = 145$$

An equivalent circuit of the transmission chain can be defined:



$$G_{max} = -725\left(\frac{Z_C}{Z_C + Z_{out}}\right)$$

Numerical example

With the components specified in the calculation of Z_{AC} and Z_L = 600 Ω we obtain:

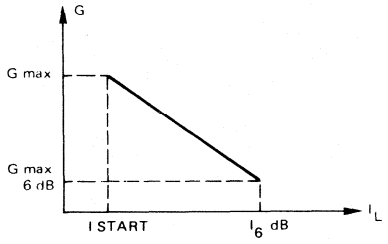
$$G_{max} = 330 \text{ or } G_{max} = 50.3 \text{ dB at } f = 800 \text{ Hz}$$

TRANSMISSION CIRCUIT CUT-OFF FREQUENCY

The external capacitor CF2 connected on pin 14 associated with a 4 kΩ internal resistor produces a first order filter whose recommended cut-off frequency is 3 800 Hz in order to obtain satisfactory preemphasis in DTMF mode.

GAIN CONTROL SYSTEM (in both transmission and receiving)

The gains of transmission and receiving circuits depend on line length; i.e. the gain control system is driven by the line current.
A fixed amount I_0 of the line current is drained for the proper operation of the circuit, the rest of the current (I_L - I_0) is measured and the result is used in the AGC. In the TEA3046, I_0 = 13 mA.
Two resistors define the currents for maximum gain (G_{max} for I_{start}) and minimum gain (G_{max} — 6 dB for I_{6dB}).



Gain = G_{max} for $I_L < I_{start}$

Gain decreases for $I_{start} < I_L < I_{6dB}$

Gain = G_{max} — 6 dB for $I_L = I_{6dB}$

When I_{start} and I_{6dB} are defined, there are two relations for calculating the corresponding resistors. RCG1 and RCG2.

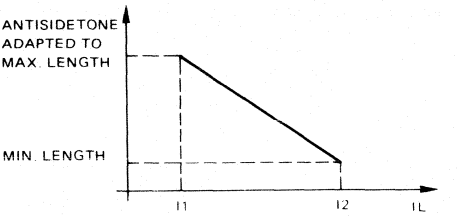
$$RCG1 = \frac{800}{I_{start} - I_0}$$

$$RCG2 = \frac{800}{I_{6dB} - I_{start}}$$

In these relations, the currents are in mA and the resistances in kΩ.

ANTISIDETONE CIRCUIT

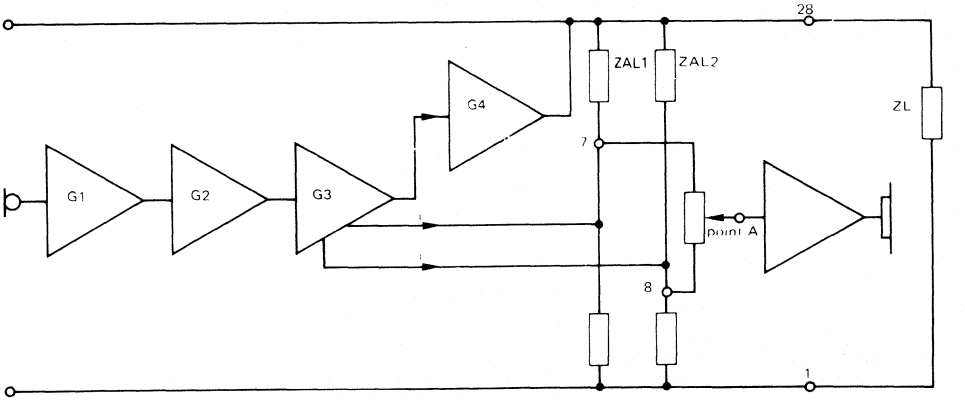
TEA3046 has double antisidetone circuitry so as to be adaptable to both the maximum and the minimum line length. Adaptation is operated by measuring the line current and balancing the circuitry with respect to this current.



I_1 and I_2 are the currents defined as I_{start} and I_{6dB} in the AGC chapter; they are set by RCG1 and RCG2 (pins 10 and 9).

Basic principle of the antisidetone circuitry

Transmission and receiving circuitry diagram



- ZAL1 is the short line antisidetone circuit.
- ZAL2 is the long line antisidetone circuit.

The impedance seen from the point A is a linear combination of the two antisidetone circuits ZAL1 and ZAL2. This combination depends on the line current and the values of RCG1 and RCG2. In fact, there is only one antisidetone circuit when seen from the point A: ZAL

$$\text{with: } ZAL = \beta ZAL1 + (1 - \beta)\, ZAL2 \qquad (0 < \beta < 1)$$

Calculation of the antisidetone circuit

For perfect antisidetone efficiency, the signal on point A must be null in transmission, i.e.:

$$i + \frac{V_L}{ZAL} = 0 \qquad (1)$$

V_L is the AC voltage on the line.
In transmission, V_L is given by:

$$V_L = G4\ i = -\ Ki\ \frac{Z_C}{Z_C + Z_{out}} = -\frac{K}{Z_{out}}\ i\ (Z_C // Z_{out}) \qquad (2)$$

The combination of (1) and (2) gives:

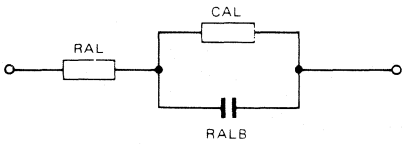
$$ZAL = \frac{K}{Z_{out}}\ (Z_C // Z_{out}) = \gamma\ Z_C // Z_{out} \text{ with } \gamma = \frac{K}{Z_{out}}$$

ZAL must be proportional to $Z_C // Z_{out}$

The value of ZAL is:

$$ZAL = \gamma\ [(Z_L + R_L) // Z_{CF3} // R_p // Z_{out}]$$

This calculation must be performed twice to obtain the two antisidetone networks corresponding to maximum and minimum line length.
It is obvious that this calculation is not easily performed. Consequently we have developed a program which computes all the external components of the application set and especially the two antisidetone networks for every type of line. Please contact our application engineer for more detailed information.
This program calculates the two
antisidetone networks as shown:



RECEIVING GAIN

The typical gain of the earphone amplifier is 20 dB.
You can adjust receiving gain in your application using the two resistors REC1 and REC2 connected between pins 7 and 8 respectively, and the ground. For your working frequency, the gain of the receiving circuit between the line and the earphone (without AGC) is given by:

$$G_{max} = 20\ dB - 20\ \log \frac{REC1}{REC1 + |ZAL1|}$$

This gain must be adjusted for max and min line length.
Two capacitors CEC1 and CEC2 are designed to have the same cut-off frequency and are used to adjust the bandwidth in reception.

DTMF SIGNAL AMPLITUDE

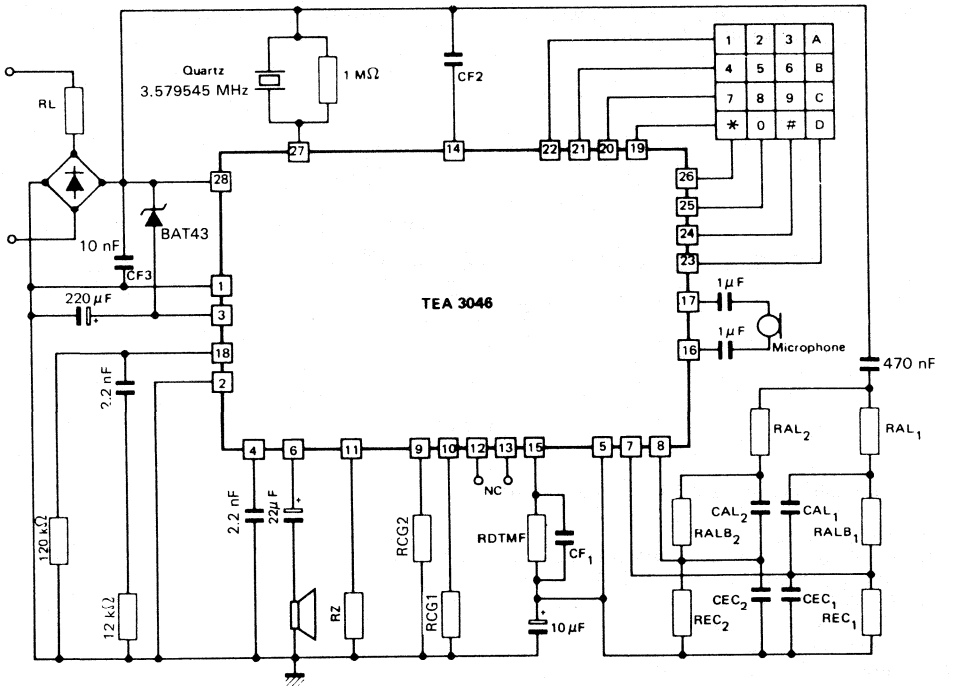
The amplitude of the DTMF signal is set by an external resistor R_{DTMF} connected between pins 5 and 15.
The preemphasis for high group tones is typically 2 dB and the reference level is defined by the amplitude of low group tones.
If NdB is the level desired for low group tones, R_{DTMF} is given by:

$$R_{DTMF} = 1.095 \times 10^5 \times 10^{[(NdB - 35.5)/20]}$$

The levels in DTMF mode are obtained if the cut-off frequency of the two filters 1 and 2 have the right value:

- Filter 1: CF1, R_{DTMF}, fc1 = 2 200 Hz.
- Filter 2: CF2, and internal resistor 4 kΩ, fc2 = 3 800 Hz.

Application diagram: public line



External components

$R_L = 12\ \Omega$		
$R_Z = 75\ \Omega$, CF3 = 10 nF, CF2 = 10 nF		→ Z = 600 Ω
RCG1 = 60 kΩ	RCG2 = 14 kΩ	→ G_{max} for I_L = 30 mA G_{max} — 6 dB for I_L = 87 mA
RAL1 = 0	RAL2 = 28 kΩ	Variable antisidetone for line length
RALB1 = 56 kΩ	RALB2 = 51 kΩ	between 0 km and 3.5 km with a
CAL1 = 47 pF	CAL2 = 1.15 nF	diameter = 0.4 mm
REC1 = 4.7 kΩ	REC2 = 6.8 kΩ	→ 0 dB receiving gain
CEC1 = 3.9 nF	CEC2 = 2.2 nF	
R_{DTMF} = 1 kΩ	CF1 = 75 nF	→ — 5 dBm DTMF signal on line

TYPICAL APPLICATION

THOMSON SEMICONDUCTEURS integrated circuits TEA3046 (phone, line adaptation), ETC9410 (microcontroller) in addition to a few components can directly interface a phone line and give the customer new facilities for a low price.

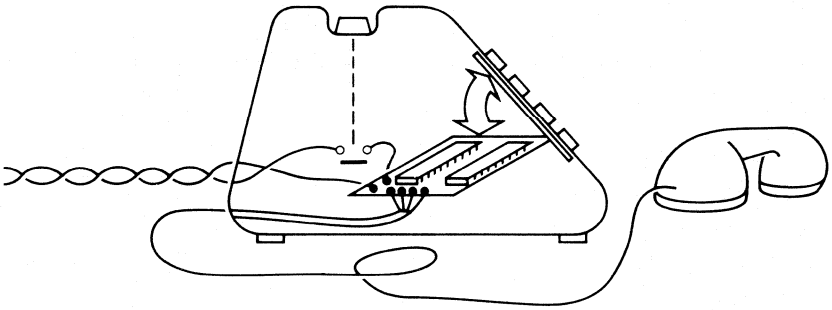


FIGURE 1

This simple board has the following features:

- DTMF or pulse dialing.
- Automatic gain control and antisidetone system.
- Fully decoded and debounced 4 x 4 matrix keyboard.
- Software programmable keyboard.
- 18 digits redial capability.
- Line monitoring.
- Telephone specific functions.

DTMF OR PULSE DIALING

By wiring (or not) strap S2 (FIG. 6) the user chooses between:

- DTMF dialing.
- Pulse dialing.

DTMF signal lasts 80 ms for one digit. This time is constant but can be software modified to any other value ($\leqslant$ 300 ms).

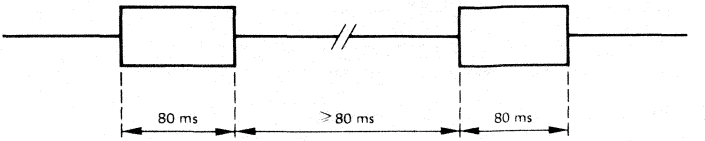


FIGURE 2

Pulse dialing is a 60/40 ms (—5%) duty cycle pulse with a 800 ms pre-pulse time.

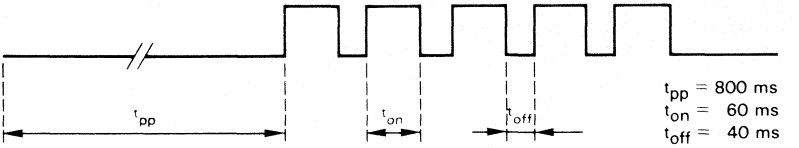


FIGURE 3: DIALING OF DIGIT "5"

Remark:
"*" and "=" keys are coded only in DTMF dialing mode.

AUTOMATIC GAIN CONTROL AND ANTISIDETONE SYSTEM

Depending on the line length, the interface IC (TEA3046) will automatically adjust audio amplifier gain and tune up the outside tone network at the best possible value.

KEYBOARD

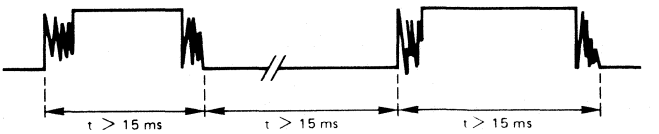
Microcontrolller takes care of everything.

Keyboard is a simple single-contact 4 x 4 matrix, without external components (like pull-up resistors).

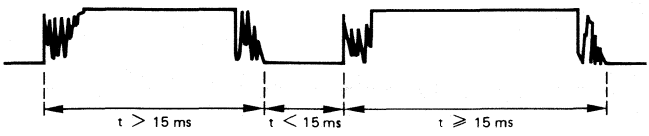
Keyboard decoding is not related to physical key location, i.e. keys (digit and function) can be located anywhere on the matrix, software will properly decode them (by scanning a 16 bytes table).

In addition, software is such that:

- A key should be depressed for 15 ms (or more) to be properly decoded.
- Two keys depressed at the same time will not be decoded.
- The minimum time length between two key-hitting is 15 ms (if less than 15 ms, the second key is not decoded).
  (see FIG. 4).



2 keys are decoded



First key decoded

FIGURE 4

REDIAL

Everytime you hang-up, the last phone number dialled is saved in RAM.
Later on, when you pick-up telephone, an automatic redial of the last saved phone number can be done by depressing the "F2" key (see FIG. 5).

Redial can handle 18 digits (including pauses).
These digits are saved during the 30 mn following hanging-up.

1	2	3	F1
4	5	6	F2
7	8	9	F3
*	0	#	F4

FIGURE 5: KEYBOARD

LINE MONITORING

Microcontroller is continuously watching the line DC level (picking-up level is around 10 V, hanging-up level is about 48 V).
If the line is around 48 V for less than 160 ms, the board goes on running.
For a line at around 48 V for more than 160 ms (user has therefore hung-up) microcontroller saves the data and goes in "HALT" mode (low power consumption allows data retention for 30 mn).

FUNCTIONS

Some specific functions were tested on the board. One should note that, depending on specifications required by the customer, other functions can be implemented in the microcontroller program.

As an example:

PAUSE: when dialing a phone number, user may have to wait for an audio signal (stating that the outside phone network is ready) before going on depressing keys. In order to use the redial function, a software timer clocks the time between two key-hitting (when user is dialing) and a "pause" is stored in RAM as soon as this measured time exceeds 1.5 s. In redial mode, this pause is understood as a waiting time of 1.5 s.

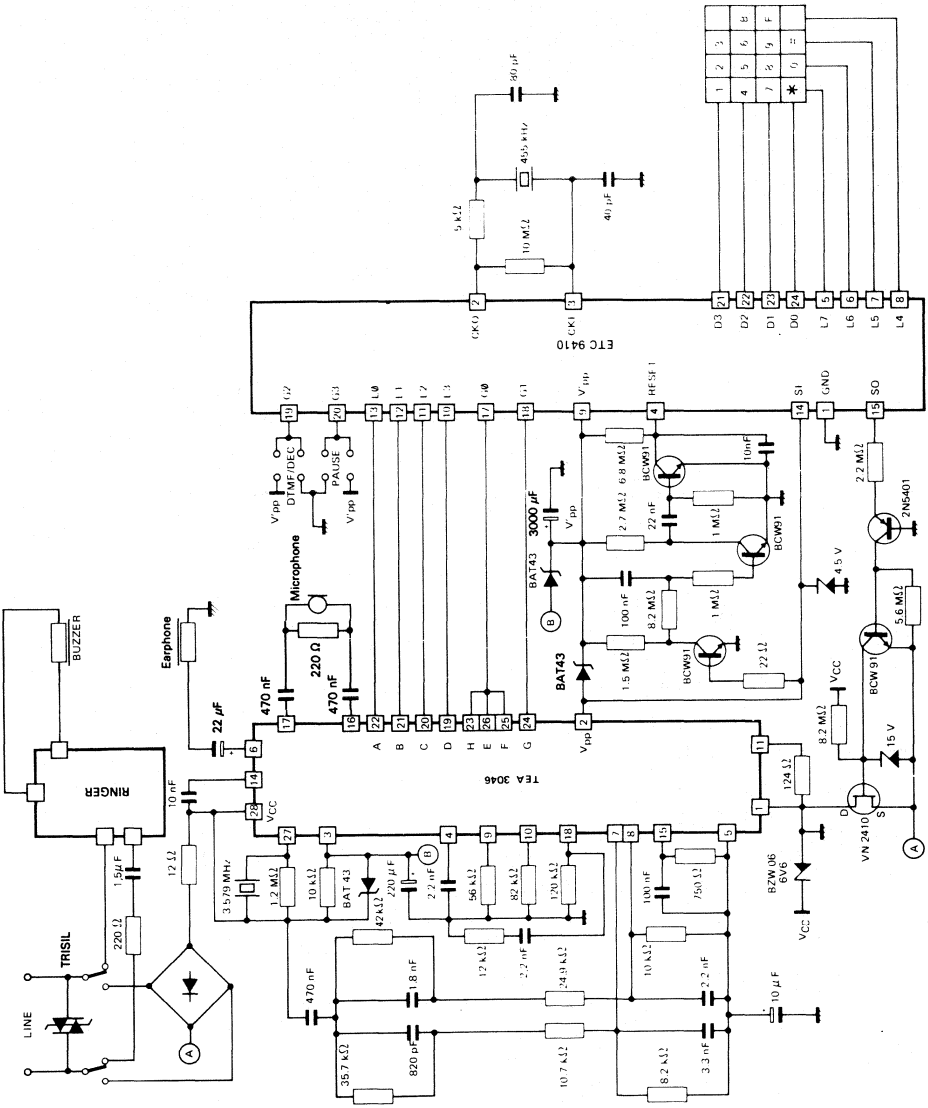
Pause length is either 1.5 s or 3 s depending on strap S3.

CALIBRATED PULSE : in pulse dialing mode, outside phone network can understand a time calibrated pulse as a specific function.
On this board, depressing F3 key is equivalent to send a 80 ms pulse (according to German standard).

DTMF AND PULSE DIALING TELEPHONE SET (TEA3046 + ETC9410)

This application has been carefully checked and is considered to be entirely reliable. However, no responsibility is assumed for inaccuracies.

This application has been realized to meet specific characteristics. Components around the application have to be adjusted to meet other specs.



DTMF AND PULSE DIALING TELEPHONE SET (TEA3046 + ETC9410)

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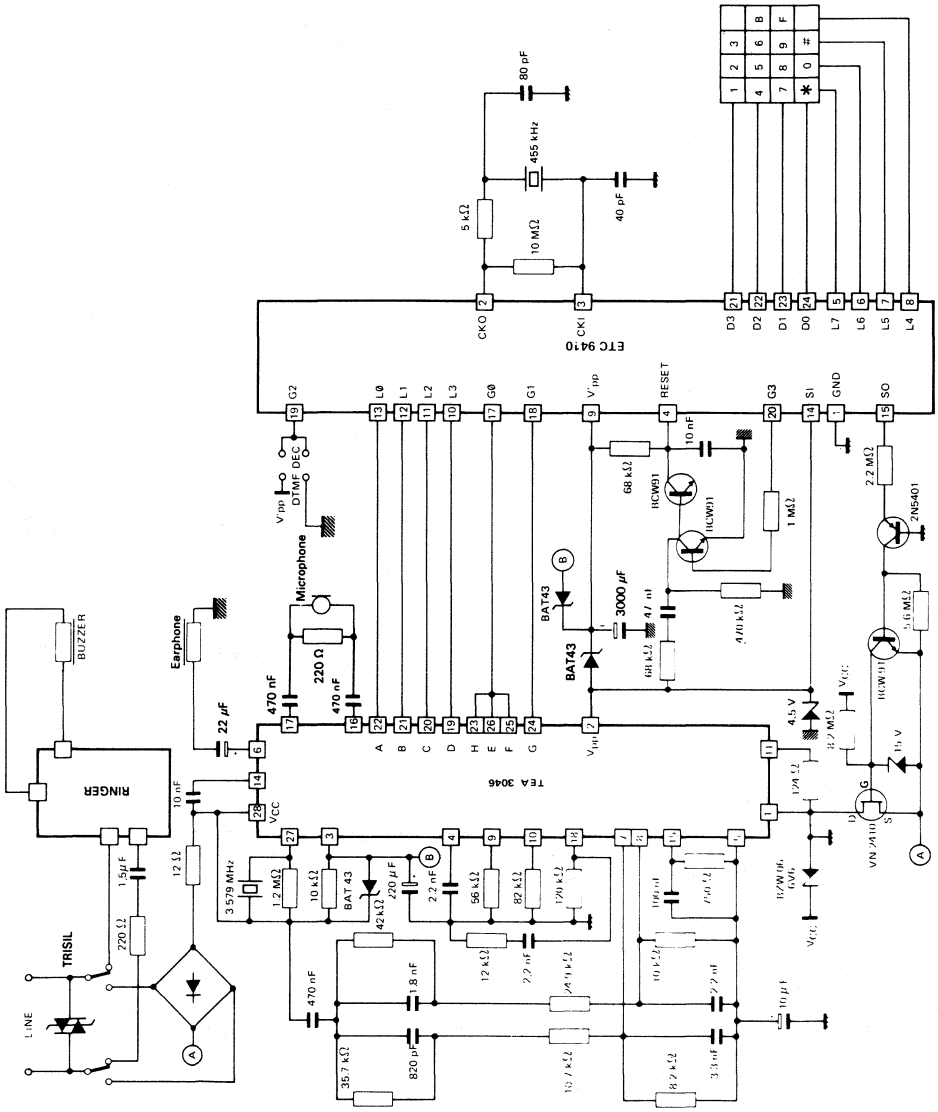
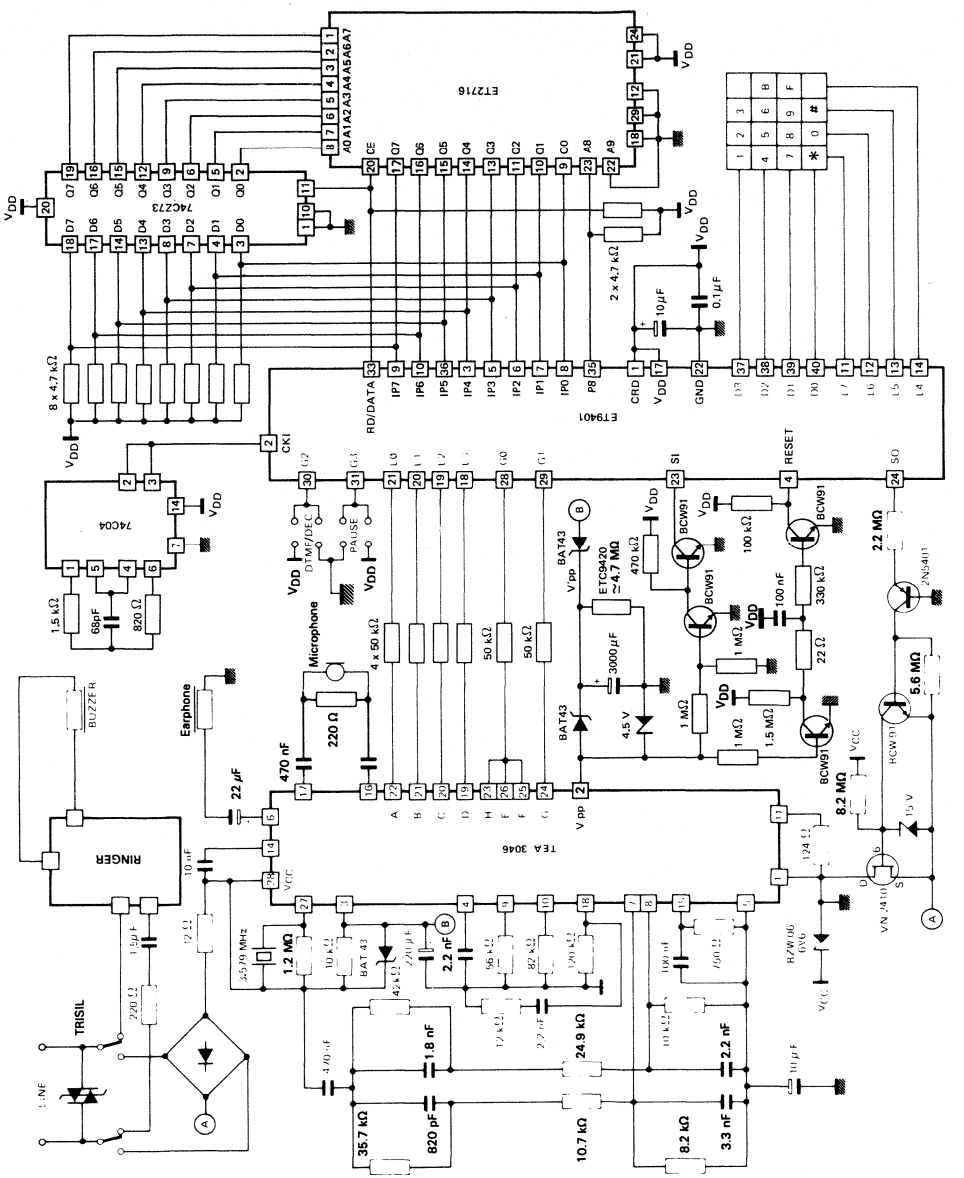
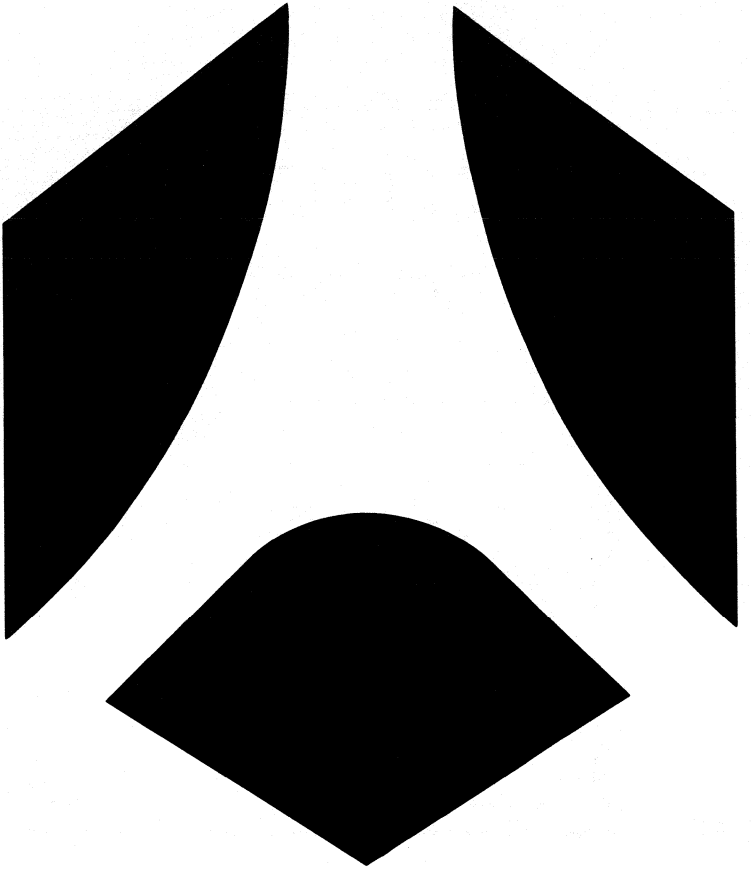


DTMF AND PULSE DIALING TELEPHONE SET (TEA3046 + ET9401)

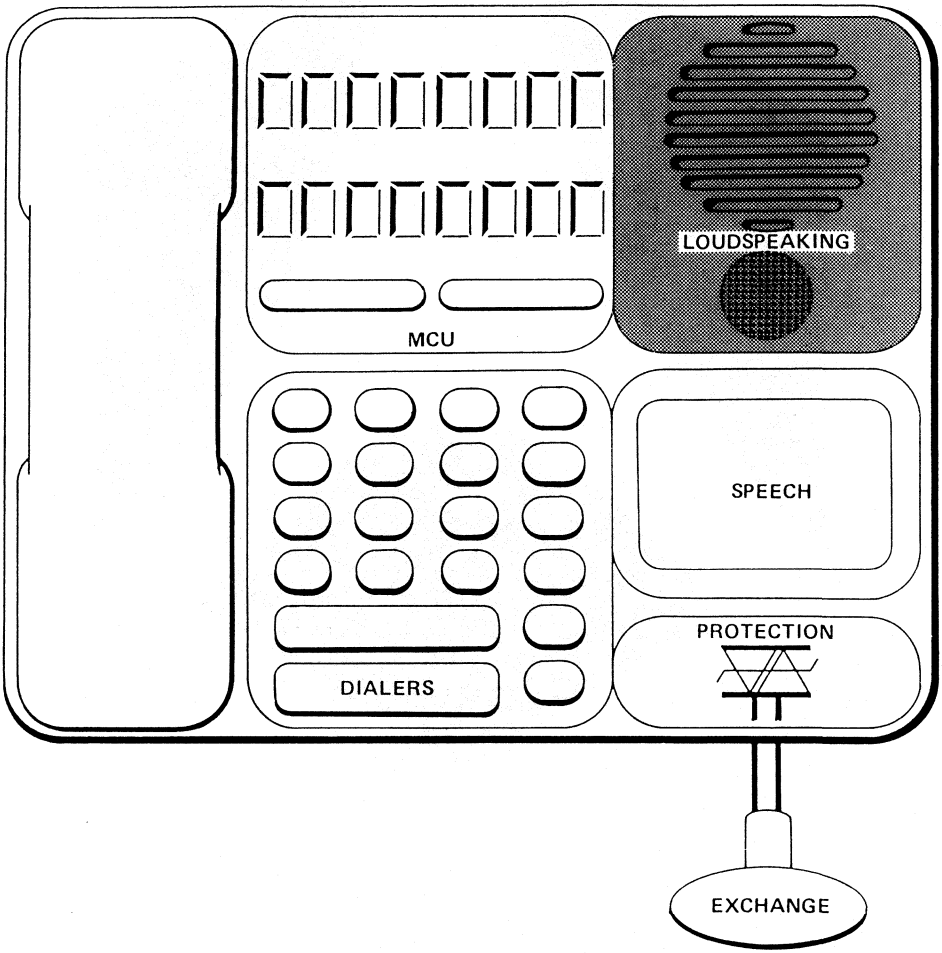
This application has been carefully checked and is considered to be entirely reliable. However, no responsibility is assumed for inaccuracies.
This application has been realized to meet specific characteristics. Components around the application have to be adjusted to meet other specs.

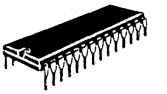
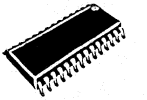
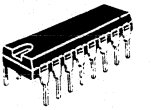
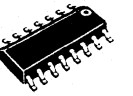
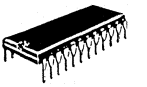
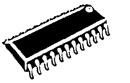


These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.



Loudspeaking ICs


LOUDSPEAKING
MCU
SPEECH
PROTECTION
DIALERS
EXCHANGE

Function	Part number	Characteristic	Package		Page
Monitor amplifier ringer	TEA7031	Loudspeaker amplifier, anti-acoustic feedback system (anti-Larsen), direct microcomputer supply and switching regulator.	DIL 28		3-5
			SO 28		
Monitor amplifier	TEA7531	Loudspeaker amplifier, anti-acoustic feedback system (anti-Larsen), anti-distorsion system.	DIL 16		3-23
			SO 16		
Handsfree	TEA7540	Noise/speech discimination in emission and reception, integrated signal gain compressor and programmable attenuators in both mode	DIL 24		3-35
			SO 24		

THOMSON COMPONENTS SEMICONDUCTEURS

TEA7031

MONITOR AMPLIFIER AND RINGER

This 28 pins IC is used with a microcomputer and provides :

- Signal amplification for monitoring (Loudspeaker).
- Ringing melodies.

Loudspeaker amplifier

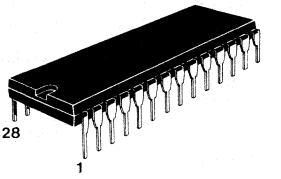
- Anti-acoustic feedback (antilarsen).
- Antidistorsion by automatic gain adaptation.
- Programmable gain in steps of 6 dB or linearly.
- ON/OFF position
- Low voltage.
- Power: 100 mW at 5 V

Ringer

- Switching regulator to transform high into low voltage in ring mode
- Microcomputer supply with reset, halt and ring detection signal.
- Tune generation by MCU and ringing by loudspeaker

BIPOLAR

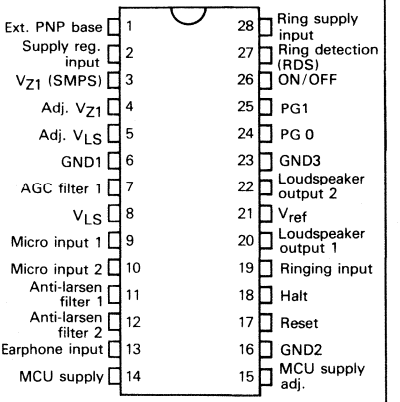
CASE
CB-132



DP SUFFIX
PLASTIC PACKAGE

Also available in SO package
(FP SUFFIX)

PIN ASSIGNMENT



43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY/FRANCE - Tel. : (1) 39.46.97.19 - Telex TCSF 204780F - Telecopie : (1) 39.46.52.64

PIN DESCRIPTION

Name	No	Description
BPN	1	Base drive to external switching transistor of the switchmode power supply
INRV	2	Switchmode power supply regulation input
VZ1	3	3.5 V Reference voltage to switchmode power supply
B	4	Adjust VZ1
C	5	Adjust VLS
GND 1	6	Ground
FAGC	7	Gain control filter
VCS	8	Supply voltage
MC 1	9	Microphone input 1
MC 2	10	Microphone input 2
FAL 1	11	Antilarsen filter 1
FAL 2	12	Antilarsen filter 2
INEAR	13	Earphone input
V_{ZMP}	14	Microprocessor supply voltage, internally zener stabilized (3.3 V)
A	15	Adjust V_{ZMP}
DND 2	16	Ground
RS	17	Microprocessor reset output
Halt	18	Microprocessor halt output
INRG	19	Input ringing signal
LS 1	20	Loudspeaker output
VREF	21	Internal reference
LS 2	22	Loudspeaker output
GND 3	23	Ground
PGL 0	24	GAIN LEVEL PROGRAMMING
PGL 1	25	GAIN LEVEL PROGRAMMING
ON/ OFF	26	Loudspeaker ON/ OFF
DS	27	Ring signal indication
Vs +	28	Rectified ring signal input

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (adjustable)	V_{LS}	6	V
Input voltage rectified ring signal	V_{S+}	22	V
Supply current	I_{LS}	60	mA
Power dissipation	P_{tot}	360	mW
Microprecesseur short regulator voltage	V_{ZMP}	6	V
Microprocesseur short regulator current	I_{ZMP}	30	mA
Operating temperature range	Toper	− 5 to + 45	°C
Storage temperature range	T_{STO}	− 55 to + 125	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$

Characteristic				Symbol	Min	Typ	Max	Unit
Shunt voltage regulator				V_{LS}	–	–	–	V
$I_{LS} = 2$ mA				–	2.65	2.8	3.2	–
$I_{LS} = 30$ mA				–	2.7	2.9	3.3	–
Voltage reference (fig. 1)				V_{ref}	–	1.1	–	V
Min. supply current (fig. 2)				I_{LS} MIN	–	–	–	mA
$V_{LS} = 2.6$ V				–	–	–	1.5	–
Gain control current								
$I_{LS} = 30$ mA (fig. 1)				I_{AGC} off	–	–	1	µA
$V_{LS} = 2.6$ V (fig. 2)				I_{AGC} on	–	− 4	− 2.5	µA
Loudspeaker amplifier								
Gain = $\frac{V22 - V21}{V13}$ (fig 3)				G	–	–	–	dB
F = 800 Hz, $V_{out} = 0.8\ V_{RMS}$								
$V_{LS} = 3$ V	ON/OFF	P_{G0}	P_{G1}					
	G_{ND}	G_{ND}	G_{ND}	–	12	14	16	–
	G_{ND}	G_{ND}	V_{LS}	–	18	20	22	–
	G_{ND}	V_{LS}	G_{ND}	–	24	26	28	–
	G_{ND}	V_{LS}	V_{LS}	–	30	32	34	–
	V_{LS}	G_{ND}	G_{ND}	–	− 20	− 30	–	–
Distortion (fig 3)				–	–	–	–	%
300 Hz to 10 kHz at G_{MAX}								
$V_{LS} = 3$ V, $V_{OUT} = 0.8\ V_{RMS}$								
	ON/OFF	P_{G0}	P_{G1}					
	V_{LS}	V_{LS}	V_{LS}	–	–	–	2	–
Ringing gain = $\frac{V22 - V21}{V19}$ (fig 4)				G_{RING}	–	–	–	dB
	ON/OFF	P_{G0}	P_{G1}					
	V_{LS}	G_{ND}	G_{ND}	–	12	14	16	–
	V_{LS}	G_{ND}	V_{LS}	–	18	20	22	–
	V_{LS}	V_{LS}	G_{ND}	–	24	26	28	–
	V_{LS}	V_{LS}	V_{LS}	–	30	32	34	–

ELECTRICAL OPERATING CHARACTERISTICS (Continued)

$T_{amb} = +25°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Microphone input impedance	–	–	4	–	kΩ
Earphone input impedance	–	–	2.5	–	kΩ
Ringing input impedance	–	–	1	–	kΩ
Input current on state (V_{LS} = 5.5 V) (fig. 3)	–	–	–	–	µA
V24 = 0 V25 = V26 = 5.5 V	I_{PG0}	−10	−5	–	–
V25 = 0 V24 = V26 = 5.5 V	I_{PG1}	−10	−5	–	–
V26 = 0 V24 = V25 = 5.5 V	$I_{ON/OFF}$	−10	−5	–	–
Input current off state (V_{LS} = 5.5 V)	–	–	–	–	µA
(fig. 3)	I_{PG0}	–	–	1	–
V24 = V25 = V26 = 5.5 V	I_{PG1}	–	–	1	–
	$I_{ON/OFF}$	–	–	1	–
Anti-acoustic feed-back system					
Microphone gain = 20 $\log_{10}$ [(V11/V9) − V10] (fig. 5)	G_{MIC}	18	22	26	dB
V_{LS} = 2.8 V, V9 − V10 = 10 mV_{rms} f = 2 kHz					
Efficiency = 20 log [V21 − (V22/V13)]	A_{NT} RMS	–	–	–	dB
V_{LS} = 2.8 V (fig. 6)					
V13 = 20 mV_{RMS}, V12 = 0.3 V	–	20	–	–	–
V13 = 20 m V_{RMS}, V12 = 0.6 V	–	–	–	−20	–
Microcomputer shunt power supply					
Supply voltage (fig. 9)					
I_{ZMP1} = 3 mA	–	3	3.3	3.6	V
Supply current (fig. 10)					
V_{ZMP} = 0.8 V_{ZMP1}	–	–	0.3	–	mA
Output current (fig 10)	–	–	–	–	µA
V17 = V18 = O_V					
Reset: ON, V14 = V_{ZMP1}	–	–	–	1	–
Reset: OFF, V14 = 0.8 V_{ZMP1}	–	–	−150	−75	–
Halt: ON, V14 = V_{ZMP1}	–	–	–	1	–
Halt: OFF, V14 = 0.5 V_{ZMPA}	–	–	−150	−75	–
Switch mode power supply					
Max input voltage (fig. 7)					
I_{VS} = 1 mA, V14 = O_V	–	22	–	–	V
Voltage reference (fig. 7)					
V_S = 22 V, V_{LS} = 2.8 V	–	3.2	3.5	3.8	V
Output current to PNP base (fig. 8)					
V14 = O_V, V2 = 3 V, PNP on	–	1	2	–	mA
V14 = O_V, V2 = 4 V, PNP off	–	–	–	–	µA
V4 (fig 8)					
V14 = O_V, V2 = 4 V	–	–	1.1	–	V
Ring detection (fig. 8)					
V14 = 3.5 V	–	0.8	1.4	–	mA
V14 = V_{ZMP1}	–	–	–	1	µA

FIGURE 1
TEST VLS , VREF , I AGC , V (5)

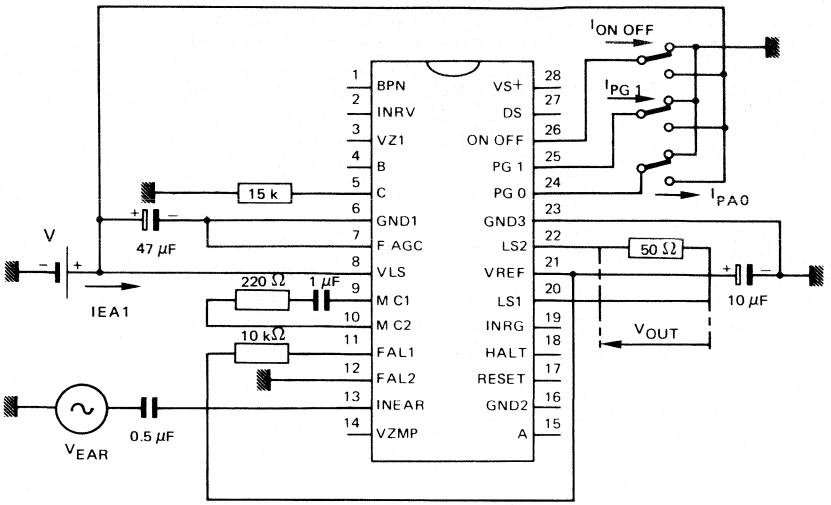


FIGURE 2
TEST POWER SUPPLY - ILS - I AGC

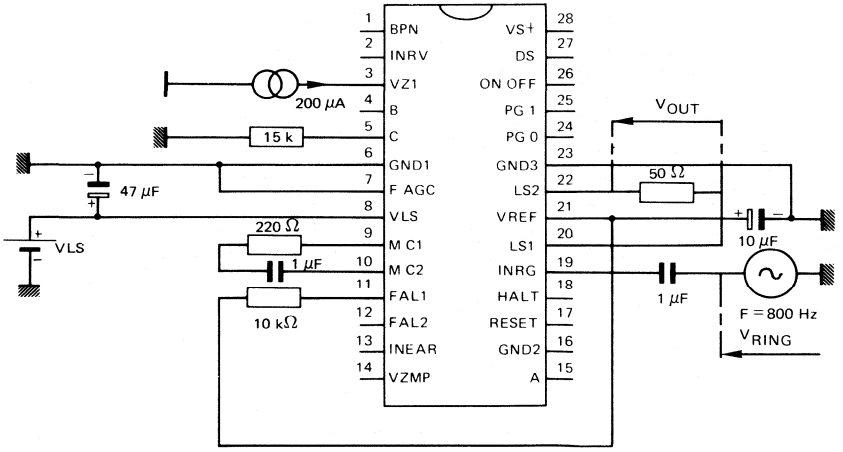


FIGURE 3
TEST LOUDSPEAKER AMPLIFIER - GAIN - DISTORTION - ILS

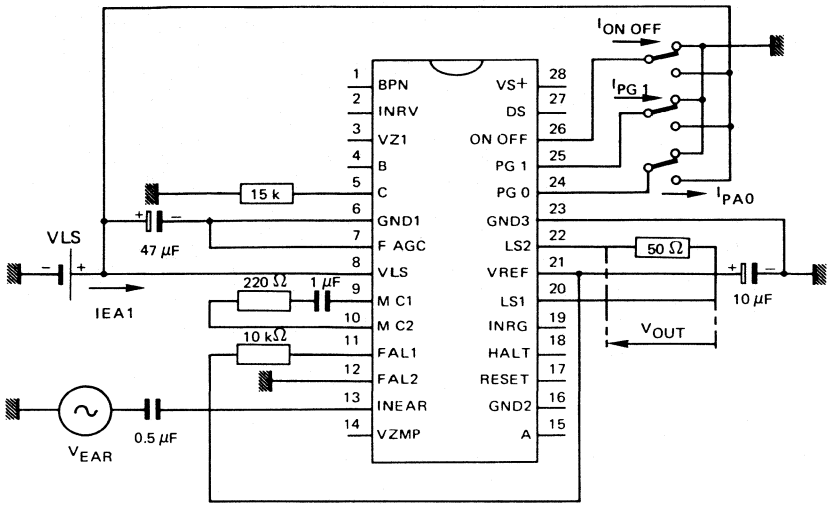


FIGURE 4
TEST AMPLIFIER

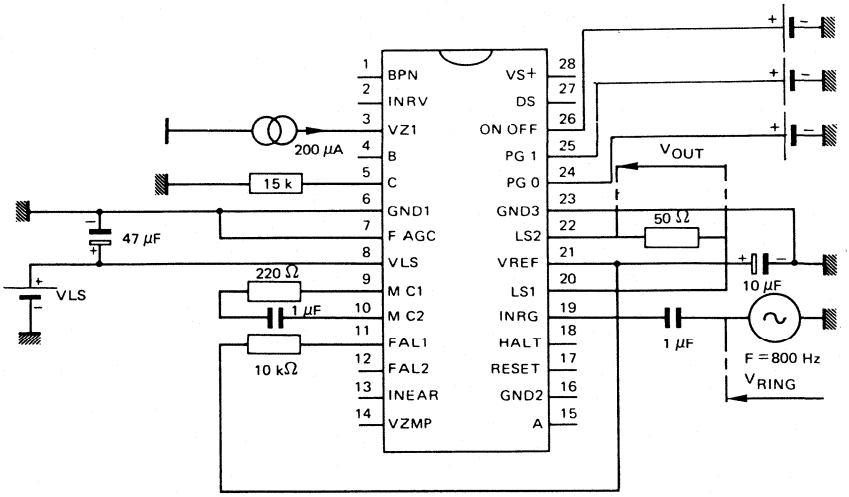


FIGURE 5
TEST ANTIACOUSTIC SYSTEM EFFICIENCY

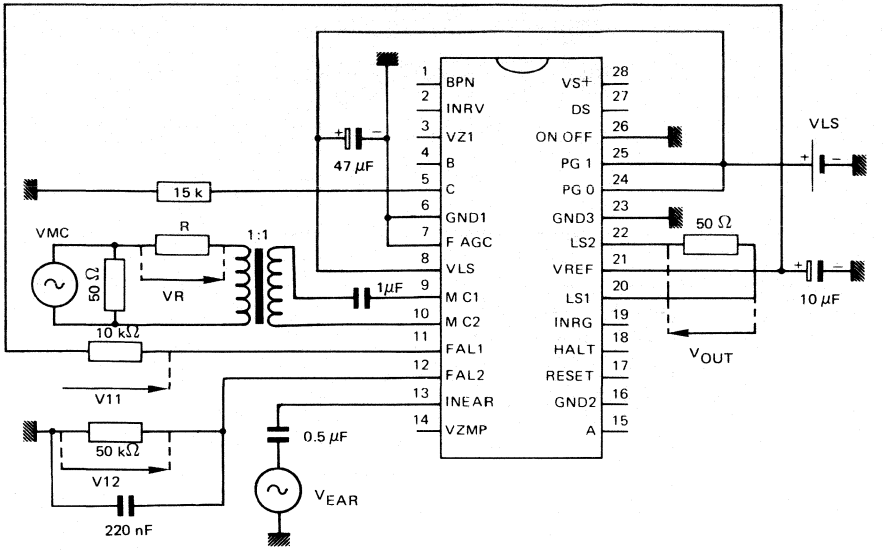


FIGURE 6
TEST ANTIACOUSTIC SYSTEM EFFICIENCY

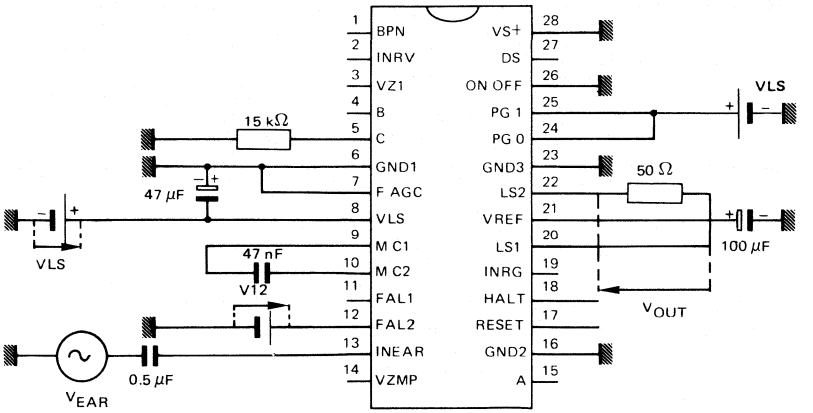


FIGURE 7
TEST POWER SUPPLY IN RING MODE - VZ1 - IBPN - IDS

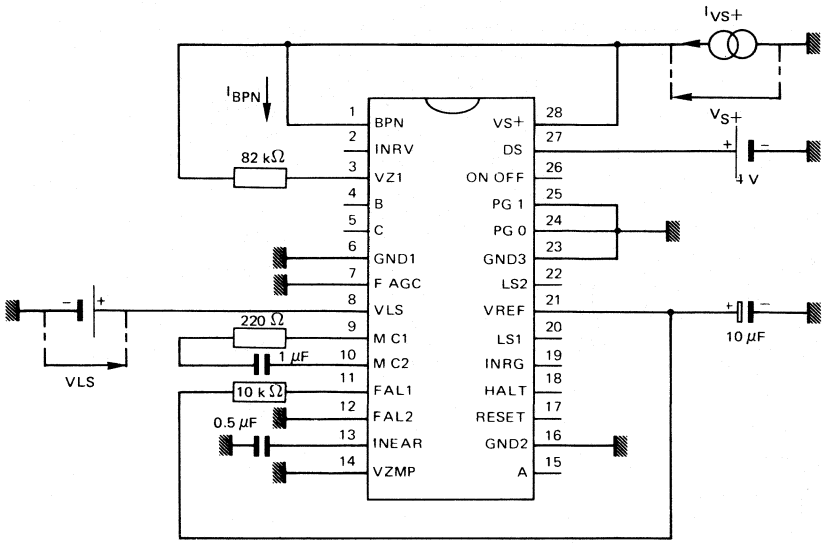


FIGURE 8
TEST POWER SUPPLY IN RING MODE - VB + MAX

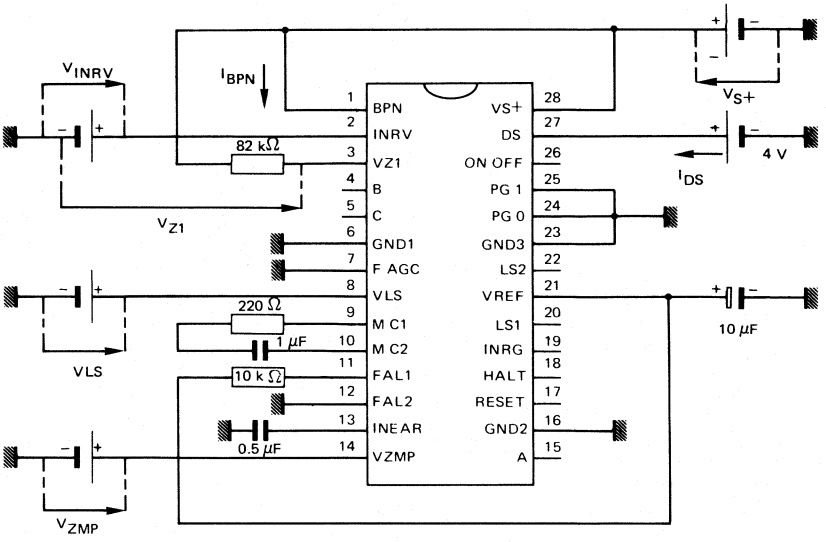


FIGURE 9
TEST MICROPROCESSOR SUPPLY - VZMP

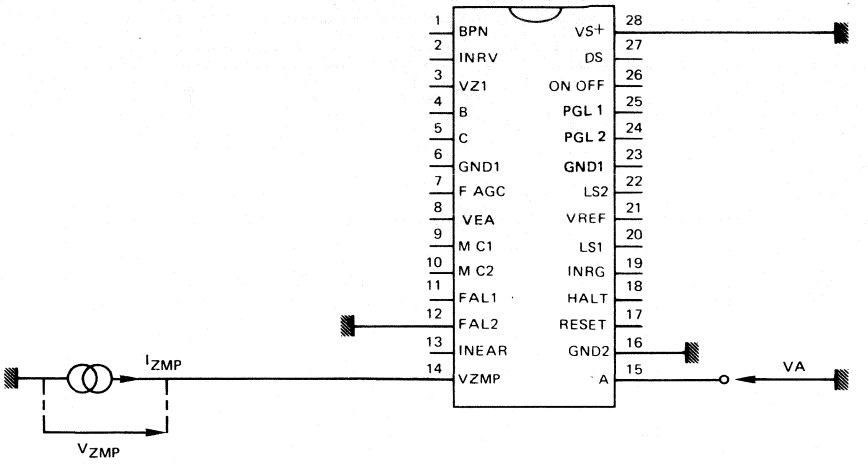
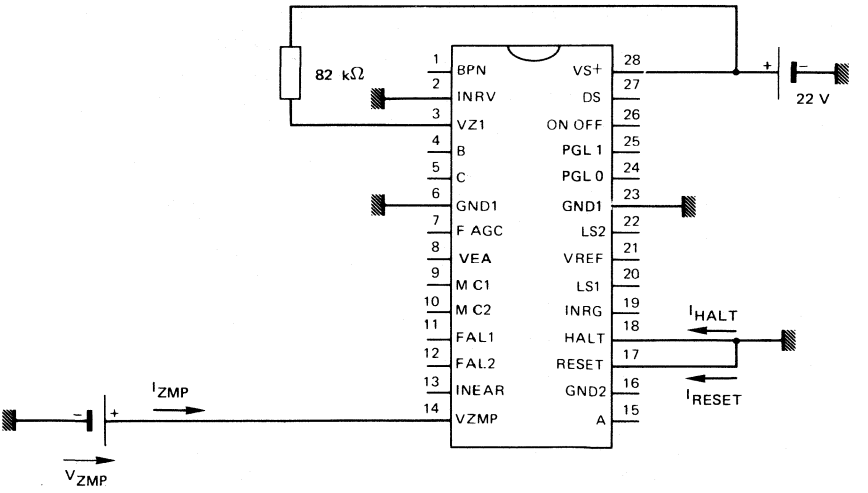
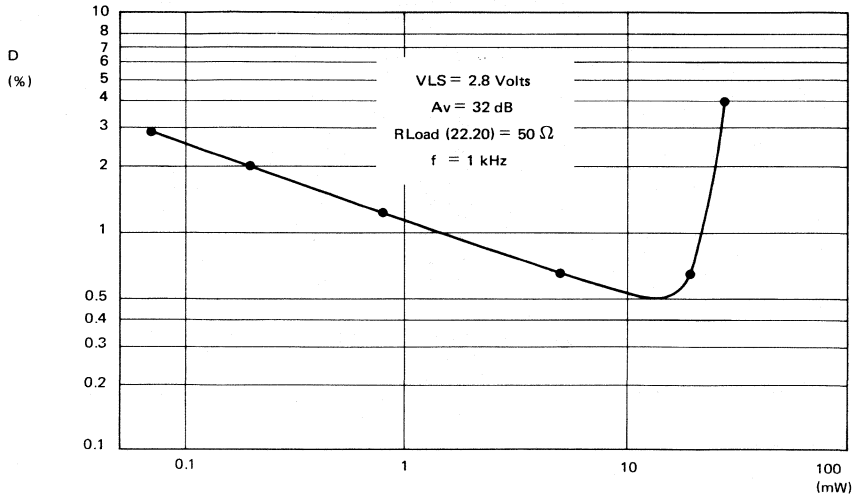


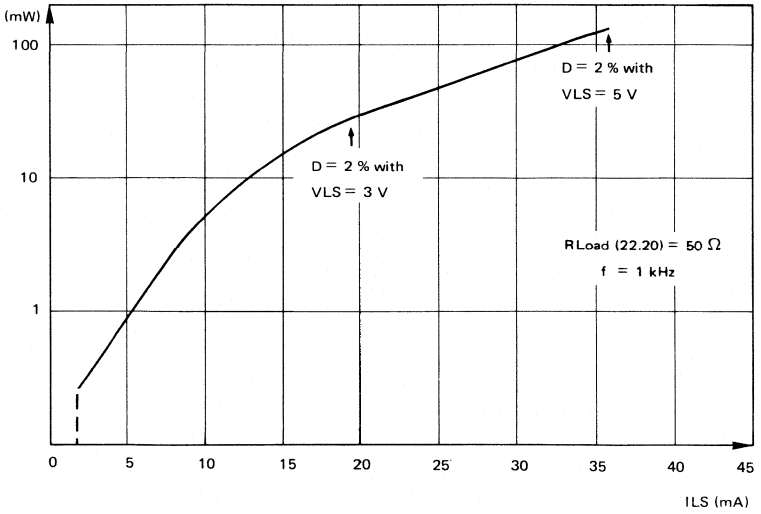
FIGURE 10
TEST MICROPROCESSOR SUPPLY - IZMP - IHALT - IRESET



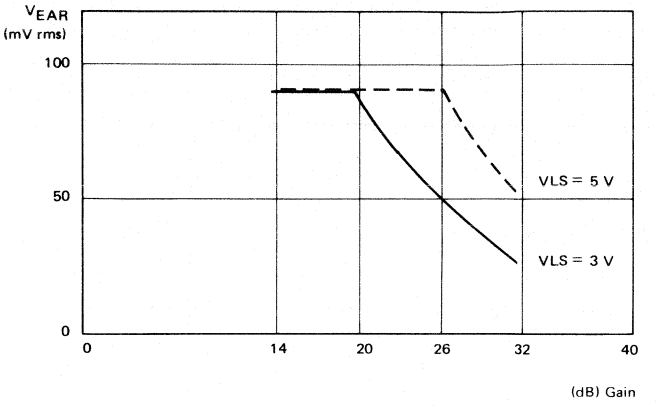
TYPICAL DISTORTION VERSUS OUTPUT POWER



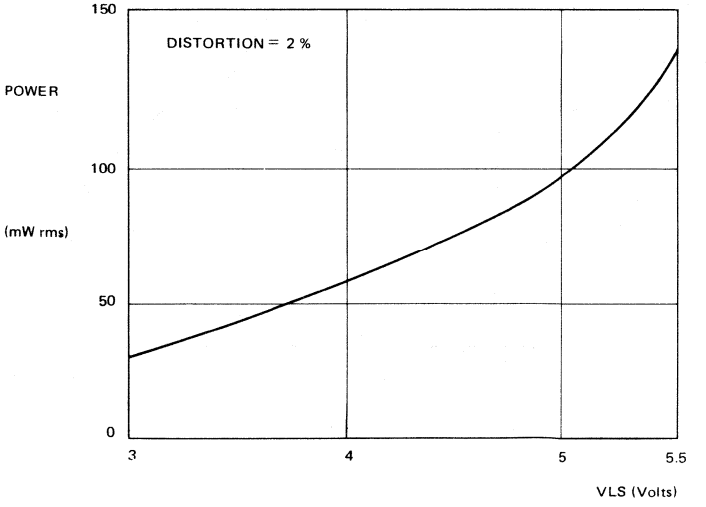
TYPICAL OUTPUT POWER VERSUS SUPPLY CURRENT



MAXIMUM AC INPUT VOLTAGE VERSUS GAIN AMPLIFIER TYPICAL CURVE

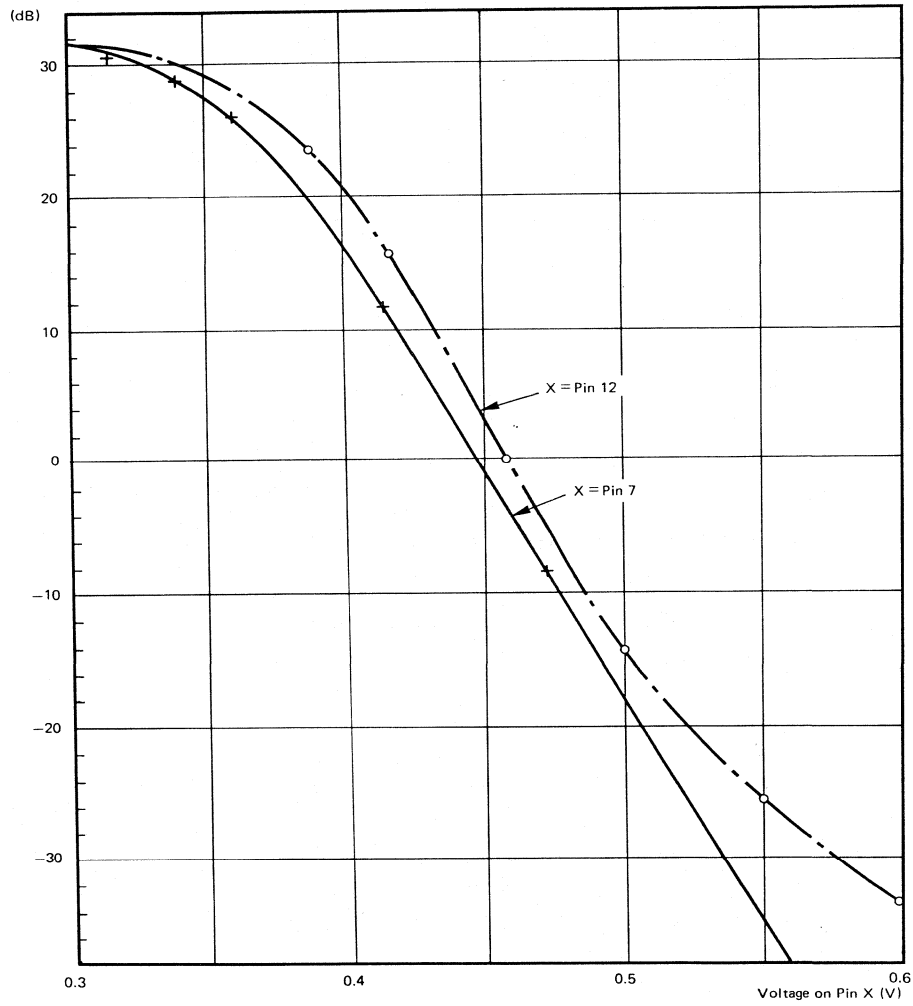


MAXIMUM POWER AVAILABLE ON LOUDSPEAKER VERSUS VLS TYPICAL CURVE

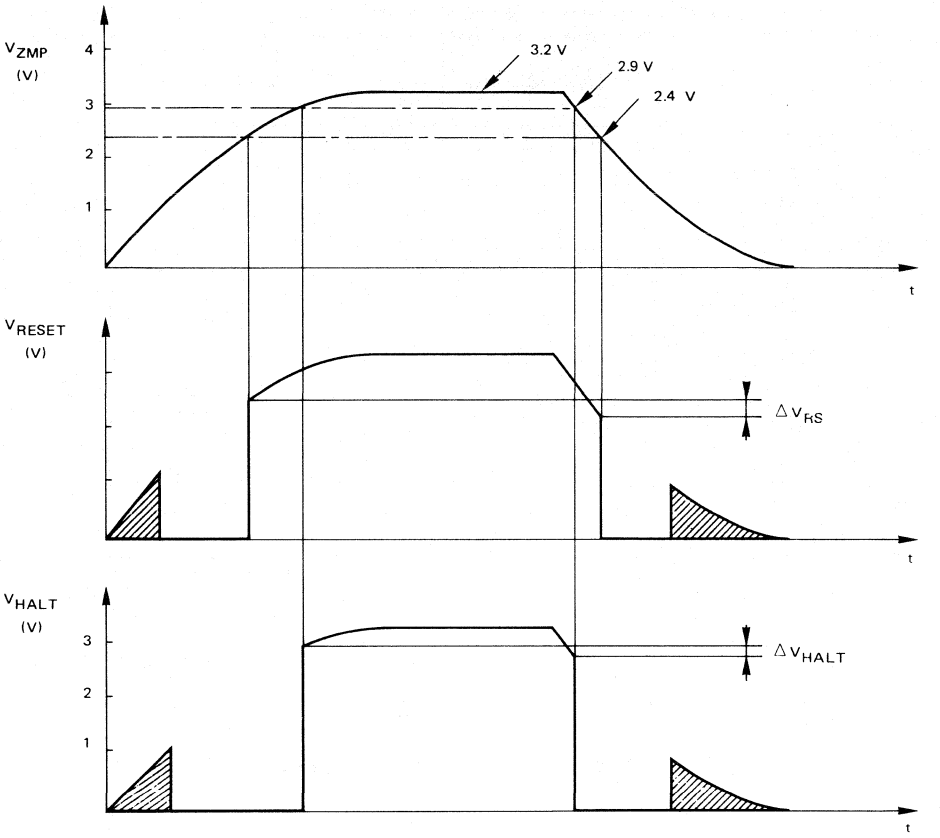


LOUDSPEAKER GAIN VERSUS VOLTAGE ON PIN (7)-(12)
TYPICAL CURVE

$$20 \log_{10} \left[\frac{V20 - V22}{V(x)} \right]$$



MICROPROCESSOR POWER SUPPLY WAVEFORM

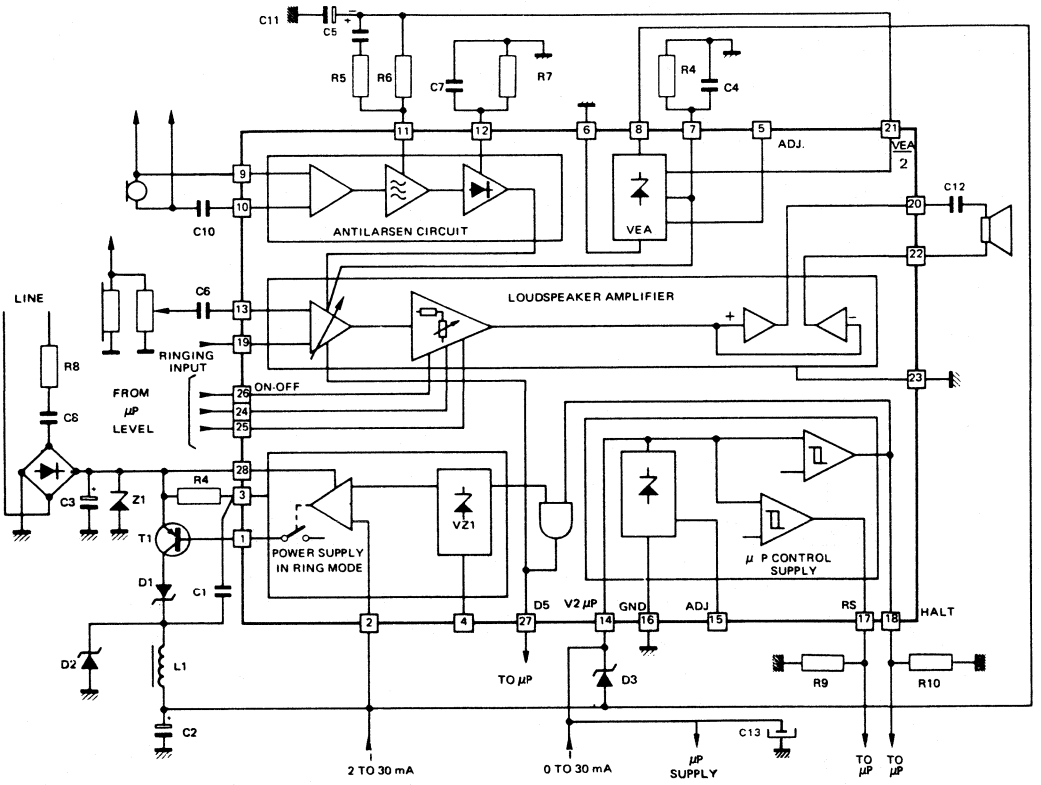


Typically $\Delta V_{RESET} = 0.2$ V

$\Delta V_{HALT} = 0.2$ V

= Undefined

TYPICAL APPLICATION

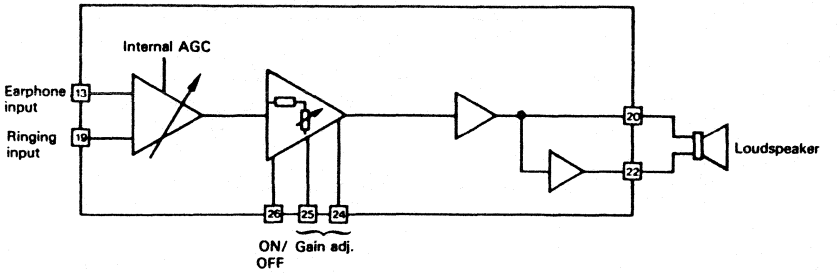


RECOMMENDED COMPONENTS

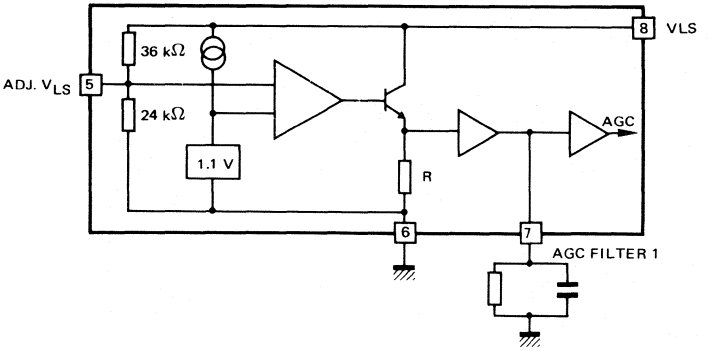
R1 82 kΩ	C1 22 pF	C10 66 nF	Z1 1N4148
R4 220 kΩ	C2 220 μF/6 V	C11 10 μF/6 V	L1 0.5 mH
R5 1 kΩ	C3 10 μF/35 V	C12 22 μF/6 V	
R6 10 kΩ	C4 33 μF/6 V	C13 33 μF/6 V	
R7 330 kΩ	C5 68 nF	T1 BCW 93	
R8 1 kΩ/1 W	C6 220 nF	D1 BAT48	
R9 1.0 kΩ	C7 220 nF	D2 BAT48	
R10 100 kΩ	C8 1 μF/160 V	D3 BAT48	

LOUDSPEAKER AMPLIFIER

- Internal AGC is used for anti-larsen and anti-distortion systems.
- Logic input: ON/OFF
  Gain adjustment (pins 24-25): 4 levels in steps of 6 dB.
- The gain can be linearly adjusted by a potentiometer on the input 13.
- On-chip bridge-output allows high output level with low DC supply voltage.



SHUNT DC SUPPLY FOR THE AMPLIFIER, AND AGC CONTROL

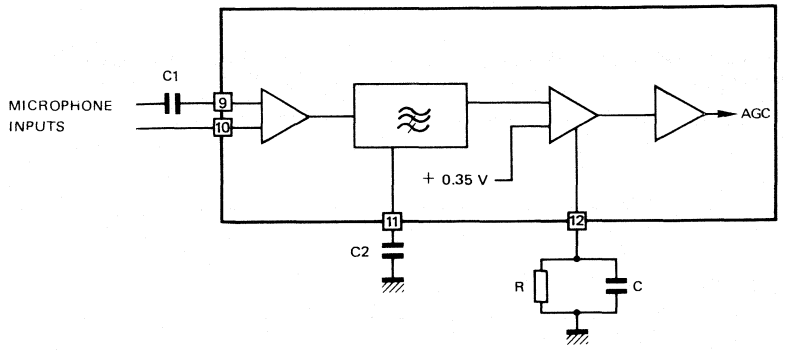


- DC voltage is internally adjusted at 2.8 V

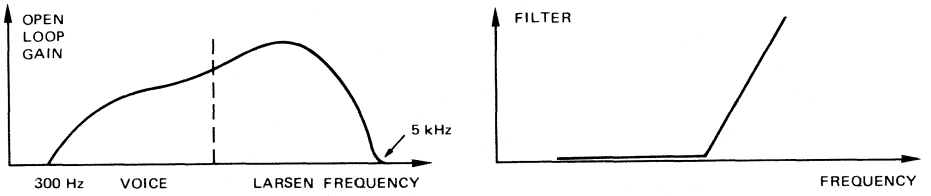
$$1.1 \times \frac{36 + 24}{24}$$

- This voltage can be externally adjusted by resistors on pin 5.
- Resistor R detects when the loudspeaker amplifier does not have enough power to drive the loudspeaker, hence causing distortion. The loudspeaker gain decreases until the power required by the loudspeaker adapts to that available on the amplifier.
- The RC network on pin 7 determines the time constant of the AGC.

ANTI-LARSEN SYSTEM

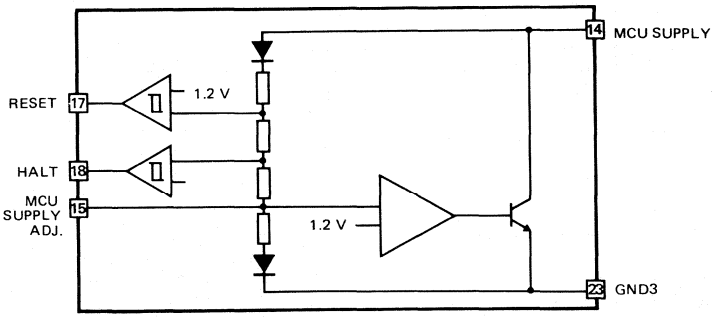


MICROPHONE RESPONSE CURVE (CEPT)



- A 2nd order filter (e.g. at 1 kHz) formed by C1 and C2 separates the voice from the acoustic feed-back signals.
- The RC network on pin 12 determines the times constant of the anti-larsen system.

SHUNT MICROCOMPUTER SUPPLY

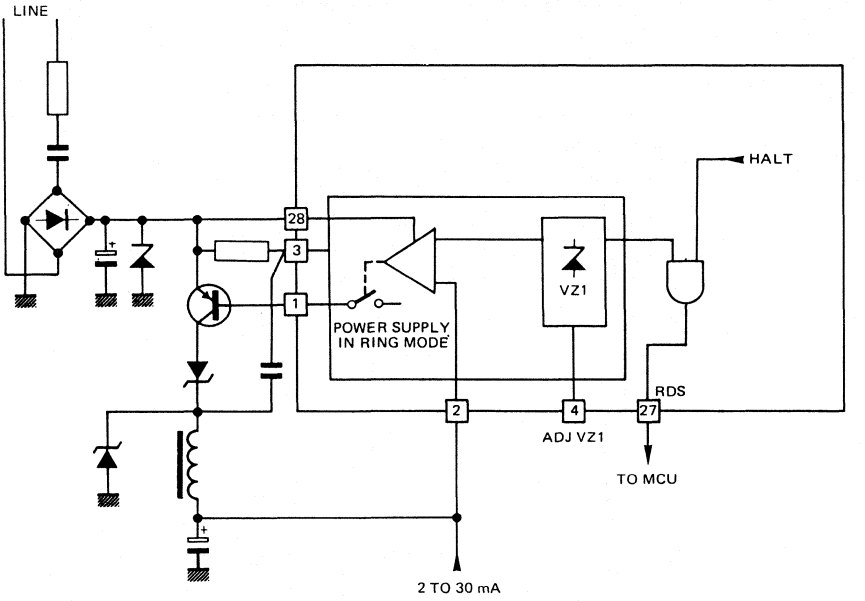


- The supply voltage is internally adjusted at 3.3 V. It can be externally adjusted through pin 15.
- Reset signal is "ON" at 2.4 V.
- Halt signal is "ON" at 2.9 V.

SWITCHING SUPPLY

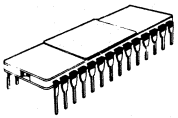
- This supply allows the circuit to be used for a ringer.
- It converts the high voltage to high current on the loudspeaker and powers the IC. So the same circuit can be used both as voice amplifier and ringer amplifier.
- When the switching regulator is operating properly and the microcomputer power supply is satisfactory, the circuit will send and active "RDS" signal to the microcomputer to instruct it to generate a melody signal. Conversely, the microcomputer will return the melody signal which is then processed internally by the TEA7031 and applied to the loudspeaker.

Application for telephone set

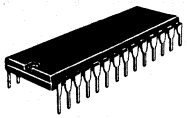


PHYSICAL DIMENSIONS

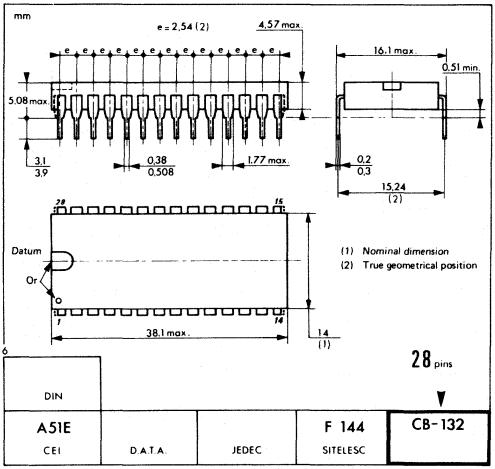
CB-132



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

TEA7531

MONITOR AMPLIFIER

This 16 pins IC is designed for monitor (loudspeaker) telephone set and provides:

- Signal amplification for monitoring (loudspeaker).
- Antiacoustic feedback (antilarsen).
- Antidistorsion by automatic gain adaptation.

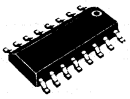
Major characteristics

- Programmable gain in steps of 6 dB or linearly.
- ON/OFF position.
- Low voltage.
- Power: 100 mW at 5 V.

BIPOLAR

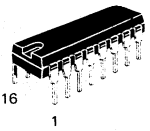
CASES

SO16



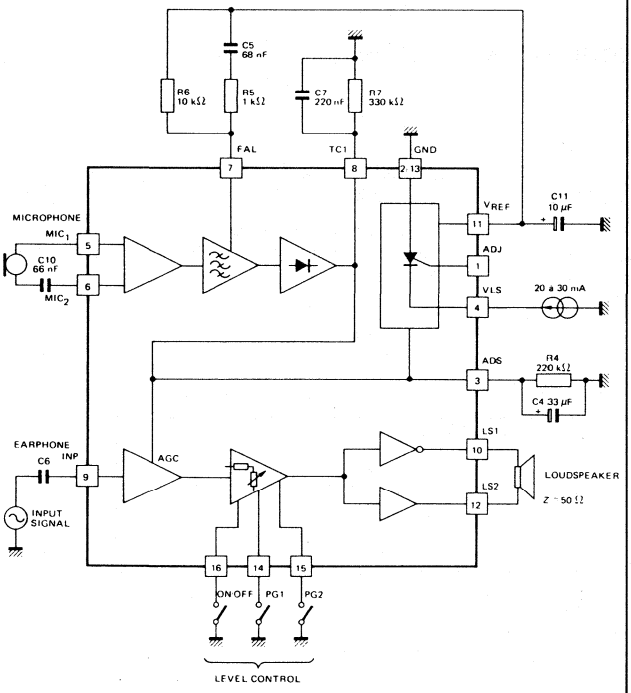
PLASTIC PACKAGE

CB-79

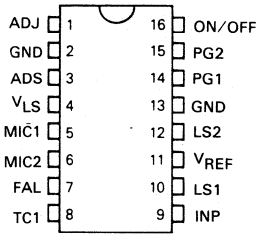


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



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PIN DESCRIPTION

No.	Symbol	Description
1	ADJ	Adjust internal reference V_{LS}
2	GND	Ground
3	ADS	Antidistortion
4	V_{LS}	Supply
5	MIC1	Microphone input
6	MIC2	Microphone input
7	FAL	Antilarsen filter
8	TC1	Antilarsen time constant
9	INP	Input signal
10	LS1	Output loudspeaker 1
11	V_{REF}	Internal resistance
12	LS2	Output loudspeaker 2
13	GND	Ground
14 15 16	PG1 PG2 ON/OFF	Inputs program level to loudspeaker

FUNCTIONAL DESCRIPTION

TEA7531 performs the following functions:

The circuit amplifies the incoming signal and feeds it to the loudspeaker. PG0 and PG1 inputs are used to set the loudspeaker gain in a range of 32 dB to 14 dB in 6 dB steps.

The TEA7531 inputs (PG0, PG1, PG2) permit the loudspeaker to be cut-off thus ensuring privacy of communication.

- The antilarsen (antiacoustic feedback) system is incorporated.
- The maximum power available on a 50 ohms impedance loudspeaker is 25 mW at 3 volts and 100 mW at 5 volts.

MAXIMUM RATINGS

$T_{amb} = +27°C$

Rating	Symbol	Value	Unit
Temperature range		— 5 to + 45	DG C
Supply voltage (V_{LS})		6	V
Supply current (I_{LS}) for T = 300 ms		60 150	mA mA
Voltage level (Pins: ONOF, PG1, PG2)		— 0.6 > to V_{LS} + 0.6	V

Limit values for external components:

R3 min = 5 kohms (R3 adjust V_{LS})
R7 max = 390 kohms

R6 min = R7/35

R max between pin 5 and 6 = 10 kohms + C min = 10 nF

ELECTRICAL OPERATING CHARACTERISTICS:

$T_{amb} = +25°C$

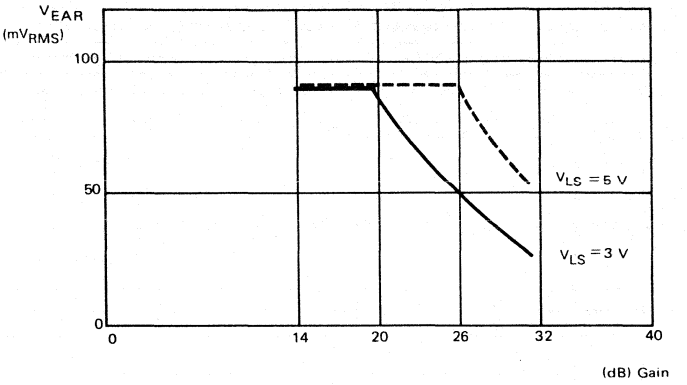
Characteristic	Symbol	Min	Typ	Max	Unit
Shunt voltage regulator					
V_{LS} supply without R1	V_{LS1}	2.6	2.8	3	V
V_{LS} maximum	V_{LSM}	—	—	5.5	V
Voltage reference with $V_{LS} = 2.8$ V	V_{ref}	1	1.1	1.2	V
Minimum supply current with $V_{LS} = 2.7$ V	I_{LSMIN}	—	—	1.5	mA
Loudspeaker amplifier					
• Gain $G = \frac{V_{(10)} - V_{(12)}}{V_{(9)}}$ (fig. 1)	G	—	—	—	—
$F = 800$ Hz $V_{LS} = 2.8$ V					
$V_{out} = 0.8\ V_{RMS}$ ($V_{out} = V_{(10)} - V_{(12)}$)					
ON/OFF = GND, PG0 = GND, PG1 = GND	G000	12	14	16	dB
ON/OFF = GND, PG0 = GND, PG1 = V_{LS}	G001	18	20	22	dB
ON/OFF = GND, PG0 = V_{LS}, PG1 = GND	G010	24	26	28	dB
ON/OFF = GND, PG0 = V_{LS}, PG1 = V_{LS}	G011	30	32	34	dB
ON/OFF = V_{LS}, PG0 = X, PG1 = X	G100	−20	−30	—	dB
• Distortion					
300 Hz to 10 kHz at G011		—	—	2	%
$V_{LS} = 2.8$ V $I_{LS} = 20$ mA					
$V_{out} = 0.8\ V_{RMS}$ (fig. 1)					
• Impedance					
Microphone input	Z_{MIC}	3.2	4	4.8	kΩ
Earphone input	Z_{INP}	2	2.5	3	kΩ
• Output offset					
$V_{(10)} - V_{(12)}$ (fig. 1) $V_{LS} = 2.8$ V at G011	V_{OFFS}	−30	—	+30	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

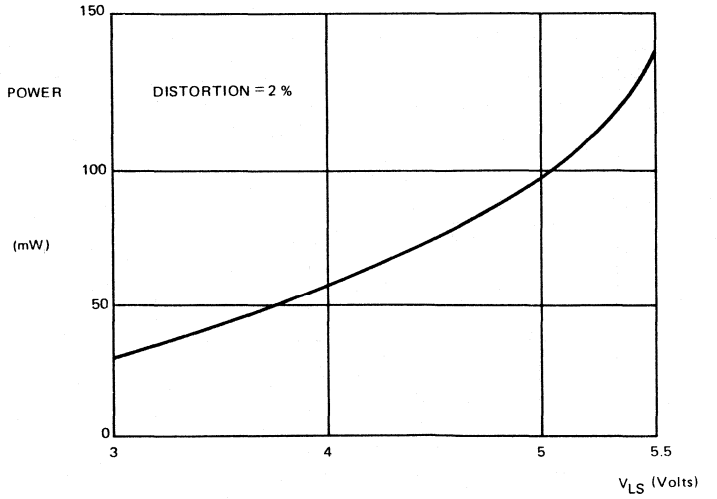
$T_{amb} = +25°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Input current					
in on-state	$I_{ON/OFF}$	−10	−5	—	μA
$V_{LS} = 2.8$ V (fig. 1)	IPG1	−10	−5	—	μA
$V_{PGi} = 0$ V	IPG2	−10	−5	—	μA
in off-state	$I_{ON/OFF}$	—	—	1	μA
$V_{LS} = 2.8$ V (fig. 1)	IPG1	—	—	1	μA
$V_{PGi} = V_{LS}$	IPG2	—	—	1	μA
Logic level voltage					
in high state	$V_{IHON/OFF}$ V_{IHPG1} V_{IHPG2}	1.5	—	—	V
in low state	$V_{ILON/OFF}$ V_{ILPG1} V_{ILPG2}	—	—	0.45	V
Antiacoustic feedback system					
$V_{LS} = 2.8$ V F = 2 kHz G011					
$V_{MIC} = 10\ mV_{RMS}$ (fig. 2)					
Microphone gain = $V_{(7)}/V_{(MIC)}$	G_{MIC}	22.5	23.5	24.5	dB
$V_{(8)}$	$V_{(8)}$	0.48	0.675	0.750	V DC
$\text{Gain} = \frac{V_{(10)} - V_{(12)}}{V_{(9)}}$ with $V_{(8)} = 0.6$ V	G	—	−30	−20	dB
Gain with $V_{(8)} = 0.4$ V	G	20	30	—	dB
Theorical value $V_{(8)} = V_{(7)} \times \frac{2 \times \sqrt{2}}{\pi} \times \frac{R7}{R6} \times r_0$					
with $0.8 < r_0 < 1$ R6 = 10 kΩ R7 = 50 kΩ					

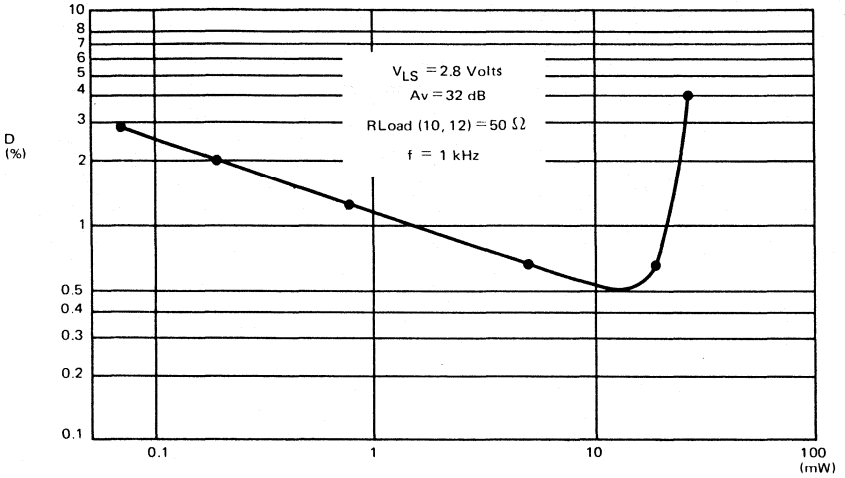
MAXIMUM AC INPUT VOLTAGE VERSUS GAIN AMPLIFIER TYPICAL CURVE



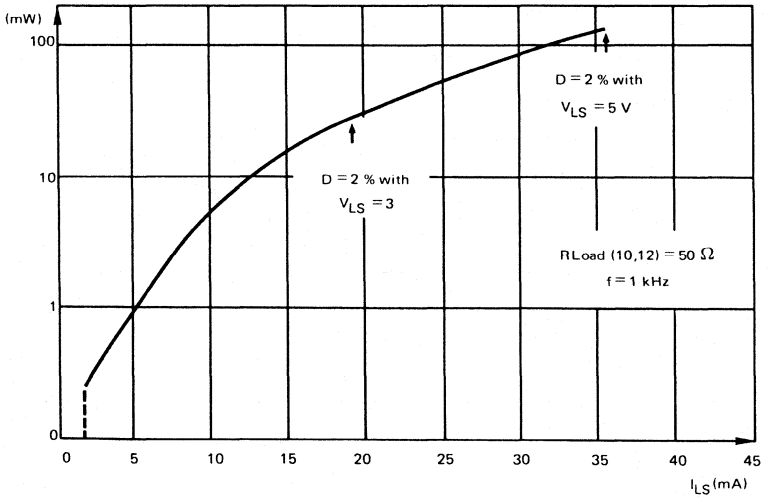
MAXIMUM POWER AVAILABLE ON LOUDSPEAKER VERSUS V_{LS} TYPICAL CURVE



TYPICAL DISTORTION VERSUS OUTPUT POWER



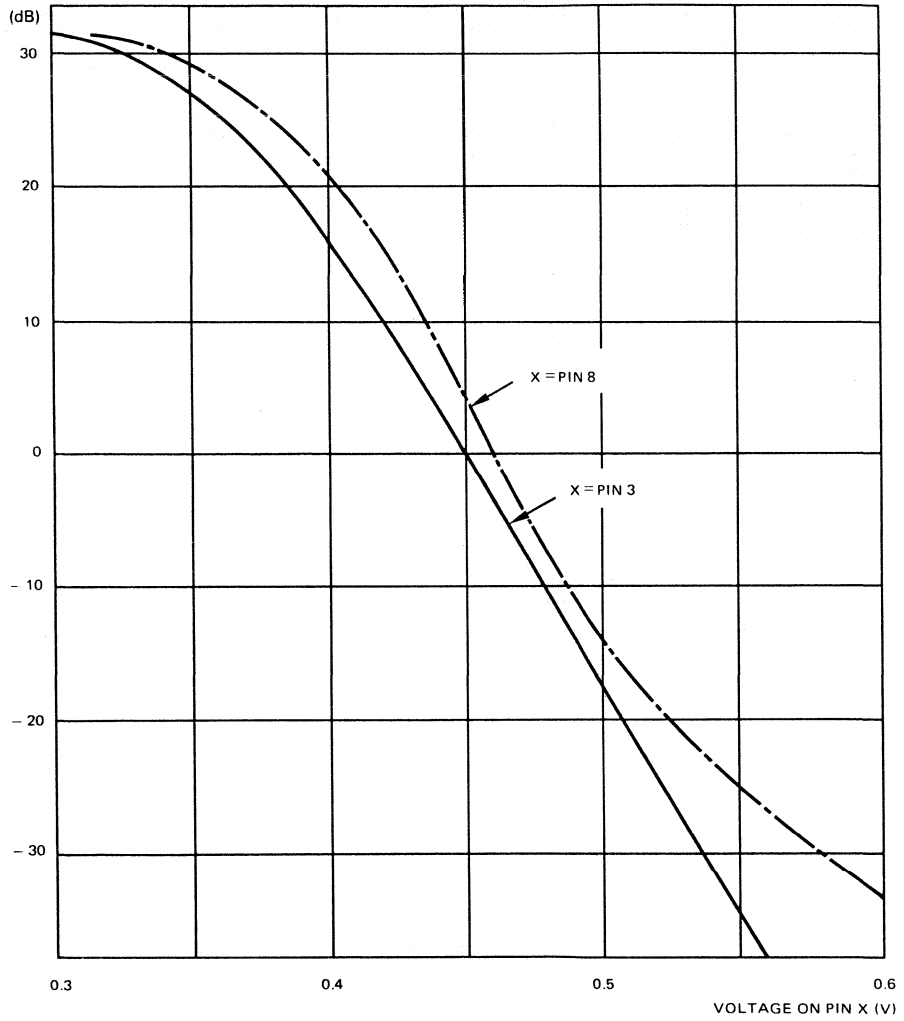
TYPICAL OUTPUT POWER VERSUS SUPPLY CURRENT

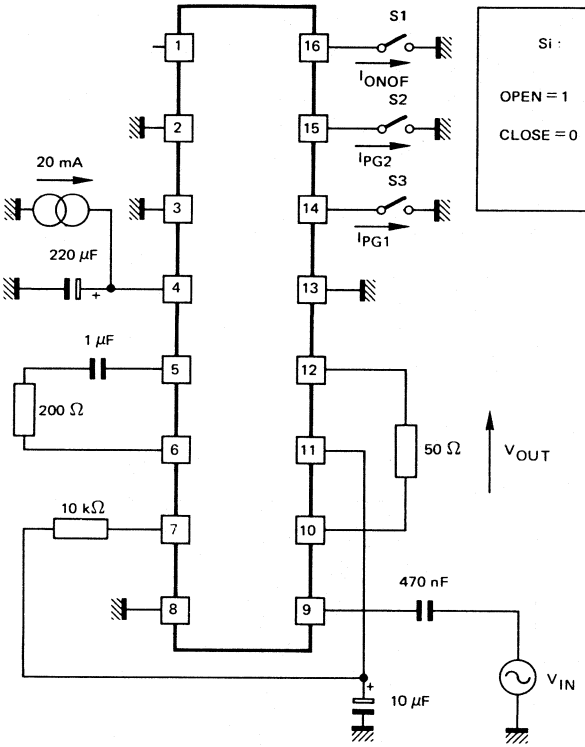


LOUDSPEAKER GAIN VERSUS VOLTAGE ON PIN (3) - (8)

TYPICAL CURVE

$20 \log_{10} \left[\frac{V10 - V12}{V(X)} \right]$





Si :

OPEN = 1

CLOSE = 0

	S1	S2	S3
G1XX	1	X	X
G000	0	0	0
G010	0	0	1
G001	0	1	0
G011	0	1	1

FIGURE 1 - LOUDSPEAKER AMPLIFIER : GAIN/DISTORTION/OUTPUT OFFSET/INPUT IMPEDANCE

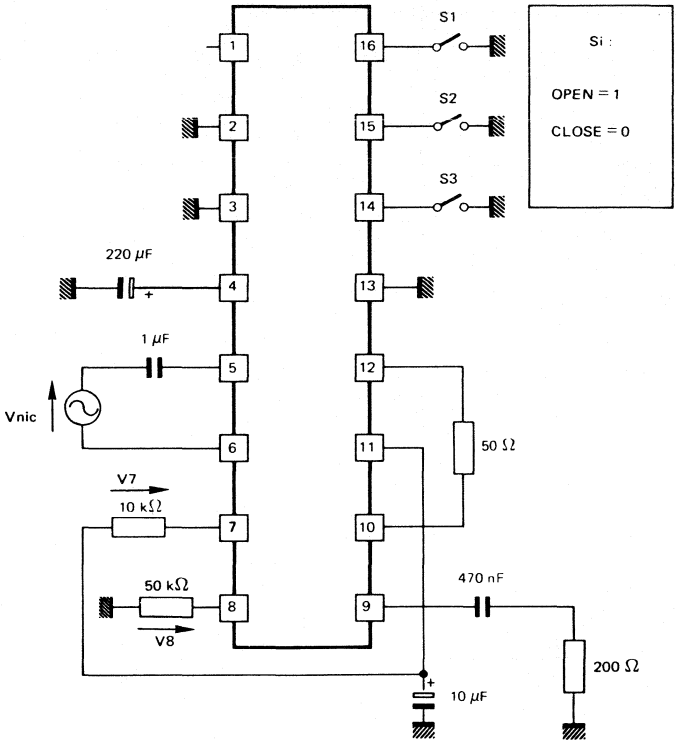


FIGURE 2 - ANTILARSEN SYSTEM

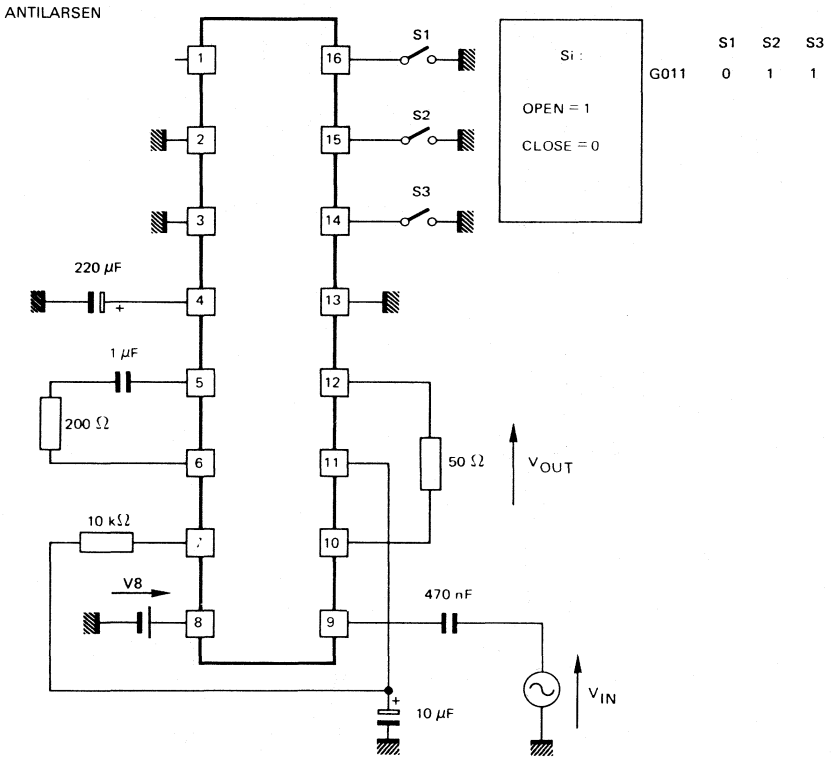
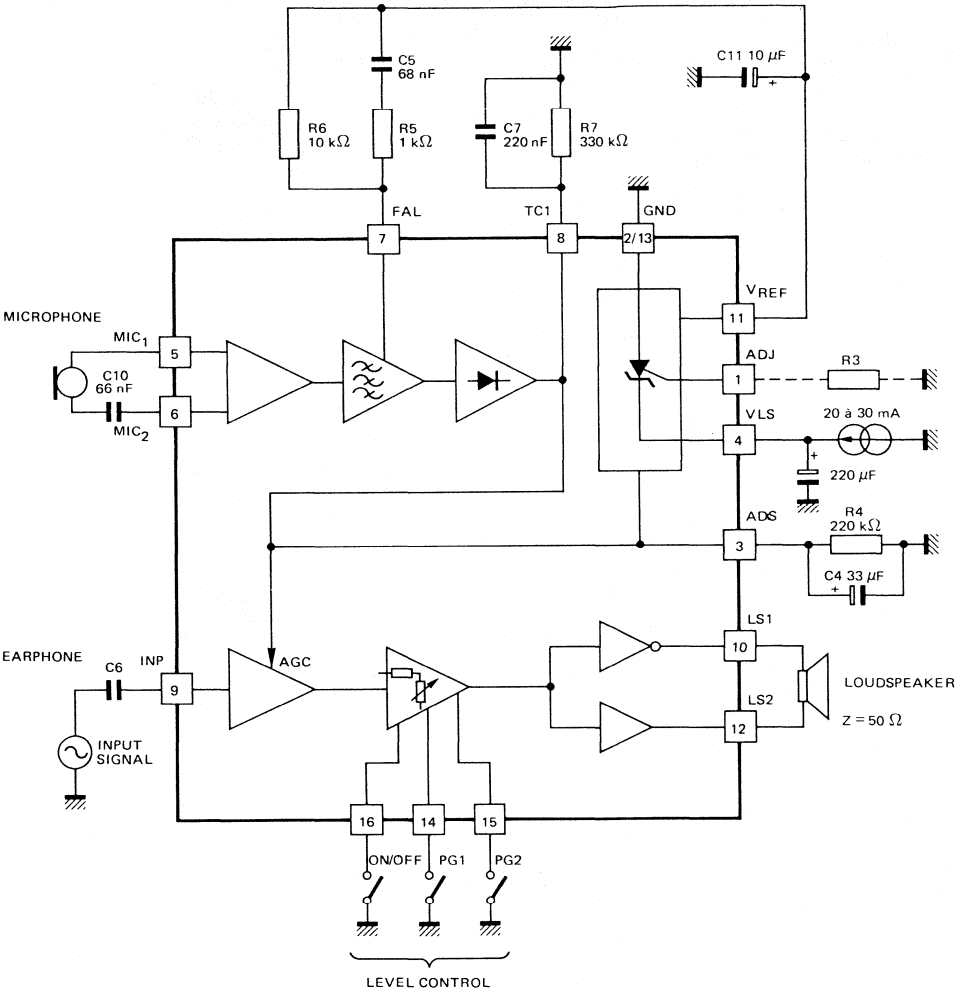
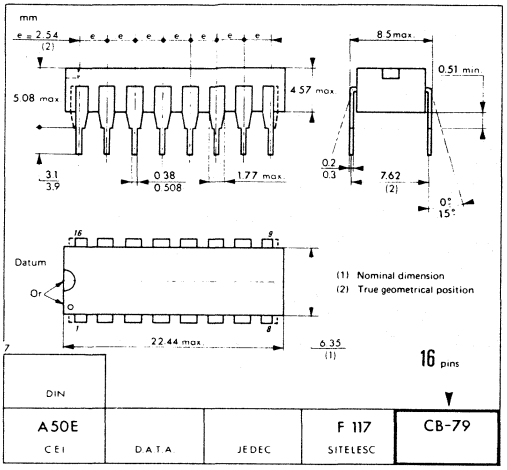


FIGURE 3 - ANTILARSEN SYSTEM

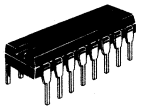
TYPICAL APPLICATION



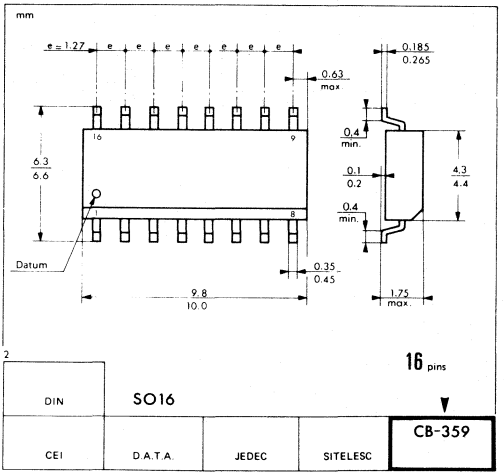
PHYSICAL DIMENSIONS



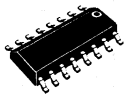
CB-79



PLASTIC PACKAGE



SO16



PLASTIC PACKAGE

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Printed in France

Ref.DSTEA7531

PRODUCT PREVIEW

BIPOLAR

This 24 pins IC is an innovative approach to quality handsfree telephone sets. It results from an extensive research on speech signal.

Its major functions are:

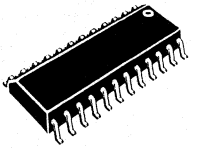
- Noise/speech discrimination in emission and reception
- Integrated signal gain compressor in both modes
- Programmable attenuators in both modes

Additional features:

- Adapted to acoustic parameters of all cabinets
- Low operating voltage 2.5 V
- Low operating current 1.7 mA
- Chip select between handsfree and monitoring modes

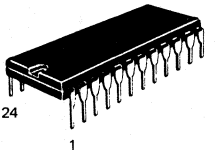
CASES

SO24



FP SUFFIX
PLASTIC PACKAGE

DIL 24



DP SUFFIX
PLASTIC PACKAGE

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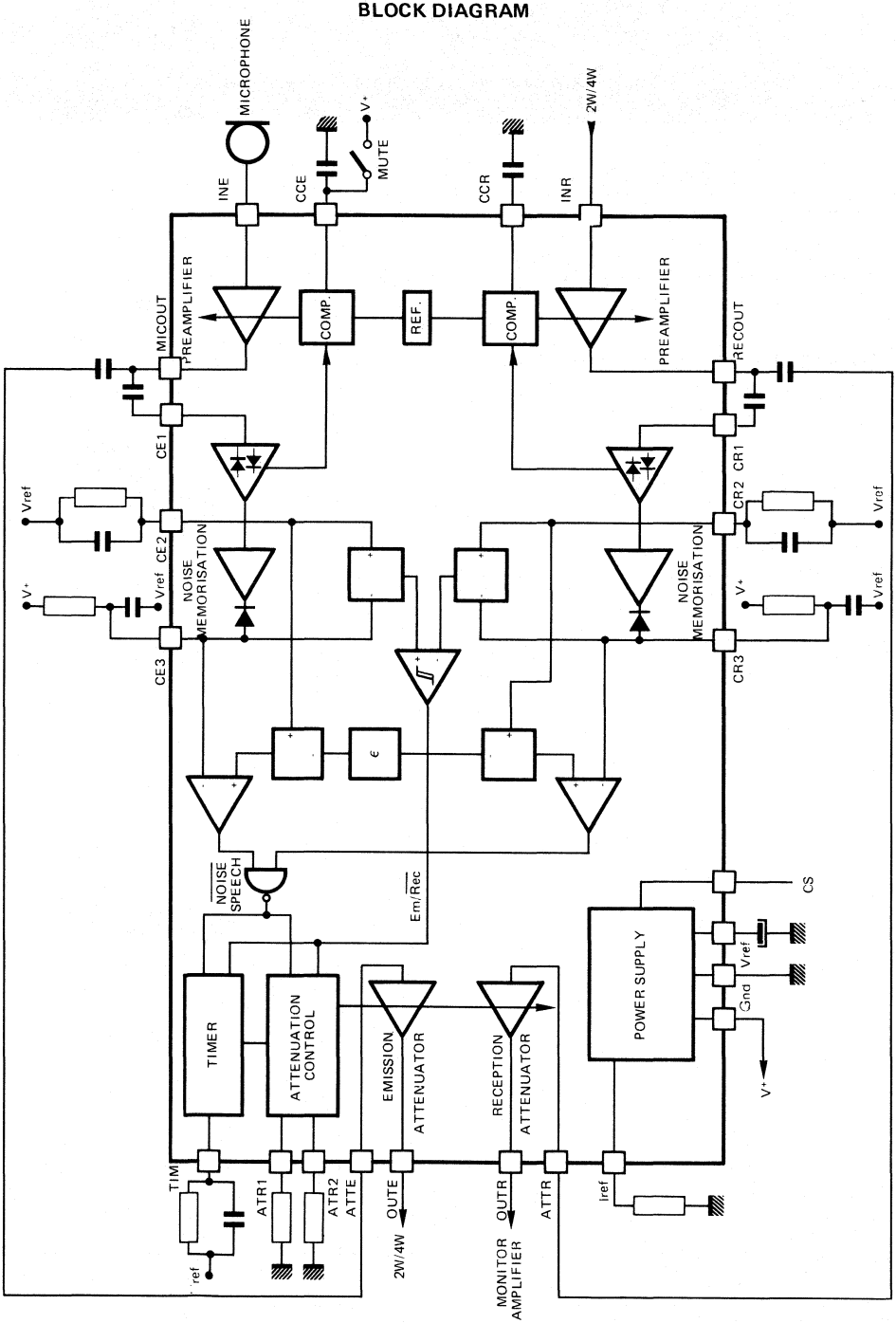
BLOCK DIAGRAM



PIN DESCRIPTION

POWER SUPPLY

NAME	PIN TYPE	No	DESCRIPTION
V^+	S		Voltage power supply from a shunt regulator or a zener diode
GND	S		Ground
I_{REF}	S		Internal current source
V_{REF}	S		Internal reference voltage

CHIP SELECT

CS	I		Chip select for monitoring mode

SIGNAL COMPRESSORS

INE	I		Microphone preamplifier input
MICOUT	O		Microphone preamplifier output
CCE	I		Time constant for the compressor of the microphone preamplifier A short circuit to V^+ on this pin mutes the preamplifier
INR	I		Reception input from 2/4 wires
RECOUT	O		Reception preamplifier output
CCR	I		Time constant for the compressor of the reception preamplifier

SIGNAL PROCESSING

CE1	I		Input of the emission full wave rectifier
CE2	I		Peak detection of the microphone signal
CE3	I		Background noise memorisation
CR1	I		Input of the reception full wave rectifier
CR2	I		Peak detection of the reception signal
CR3	I		Background noise memorisation

ATTENUATION CONTROL/TIMER

ATR1	I		External resistor } Fixe the maximum attenuation
ATR2	I		External resistor }
TIM	I		An external RC fixes the two time constants of the attenuation switch

ATTENUATORS

ATTE	I		Emission attenuator input
OUTE	O		Emission attenuator output
ATTR	I		Reception attenuator input
OUTR	O		Reception attenuator output

FUNCTIONAL DESCRIPTION

SWITCHED ATTENUATORS

Fig. 1 represents a block diagram of a handsfree subset with attenuators in signal mode. To prevent the system from howling, the total loop gain, including acoustic feedback through the housing and sidetone coupling, must be less than 0 dB. For this purpose, two switched attenuators are inserted in each mode (emission and reception).

The attenuation is shifted from one mode to the other, resulting from the speech level comparison between each way.

To prevent the circuit to switch continuously in one way, the operation of the IC must be fully symetrical in both ways. This involves signal comparison, attenuation value.

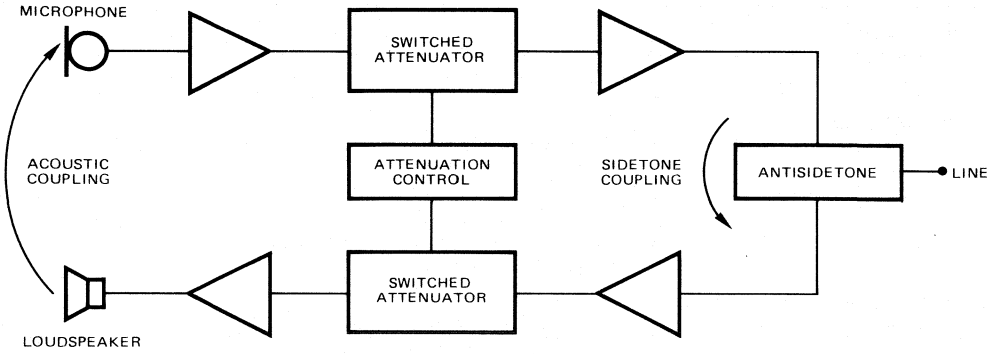


FIGURE 1

GAIN COMPRESSORS

In TEA7540, two signal compressors are inserted in each mode before the signal comparison, so the signal coming from each end has the same level (100 mV peak), the losses in each way (for instance losses resulting from the line lenght in receiving mode) are compensated and the signal comparison is fully symetrical. The time constant of each signal compressor is fixed by an external capacitor, but the gain of the compressor decreases 100 times quickly than it increases to prevent from noise increasing between words. The compressing depth is 38 dB.

BACKGROUND NOISE DISCRIMINATION

An additional feature provided in TEA7540 is background noise level discrimination in each way. The IC stores the background sound level with a long time constant (3 to 5 seconds depending on an external RC) and compares it with the incoming signal in order to distinguish a usefull signal (speech) from the background noise. This background noise memorisation is also used to compensate the noise in each mode before signal comparison: the noise level in each mode is substracted from the incoming signal before the comparison. So a very high noise level in one mode cannot trouble the comparison between the usefull signals.

The result of the comparison manages the attenuators in the following way:

- The maximum attenuation is switched on the mode where the speech signal is the lowest. The maximum attenuation is fixed by two external resistors (maximum 52 dB). The time constant of the switch is fixed by the timer via an external capacitor.
- When neither party is talking both attenuators are set to a medium attenuation. Thus each mode is in idle mode. The time constant of the switch from active mode to idle mode must be long enough to prevent from switching to idle mode between two words (see fig. 2). This time constant is fixed by an external RC.

The minimum attenuation of each attenuator is 0 dB.

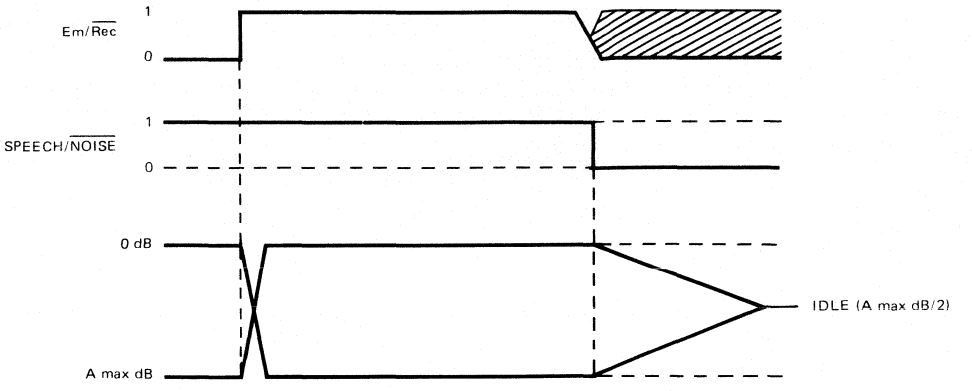


FIGURE 2

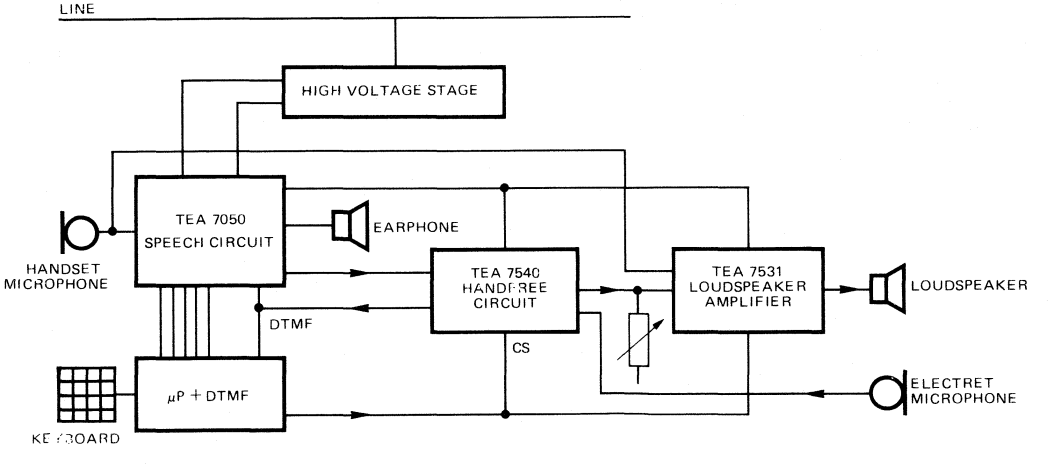
TEA7540 OPERATION

TEA7540 is powered through an external shunt regulator (for instance the shunt regulator of the monitor amplifier TEA7531) or an external zener diode. It can work at a very low voltage (2.5 volts) over the circuit and it has a low current consumption (1.8 mA).

It's also possible via the chip select pin to put the handsfree function in standby to use the circuit in monitoring mode with the handset microphone.
TEA7540 is designed to work with all kinds of microphones, including Electred.

APPLICATION DIAGRAM

Example of high range telephone set using TEA7540.



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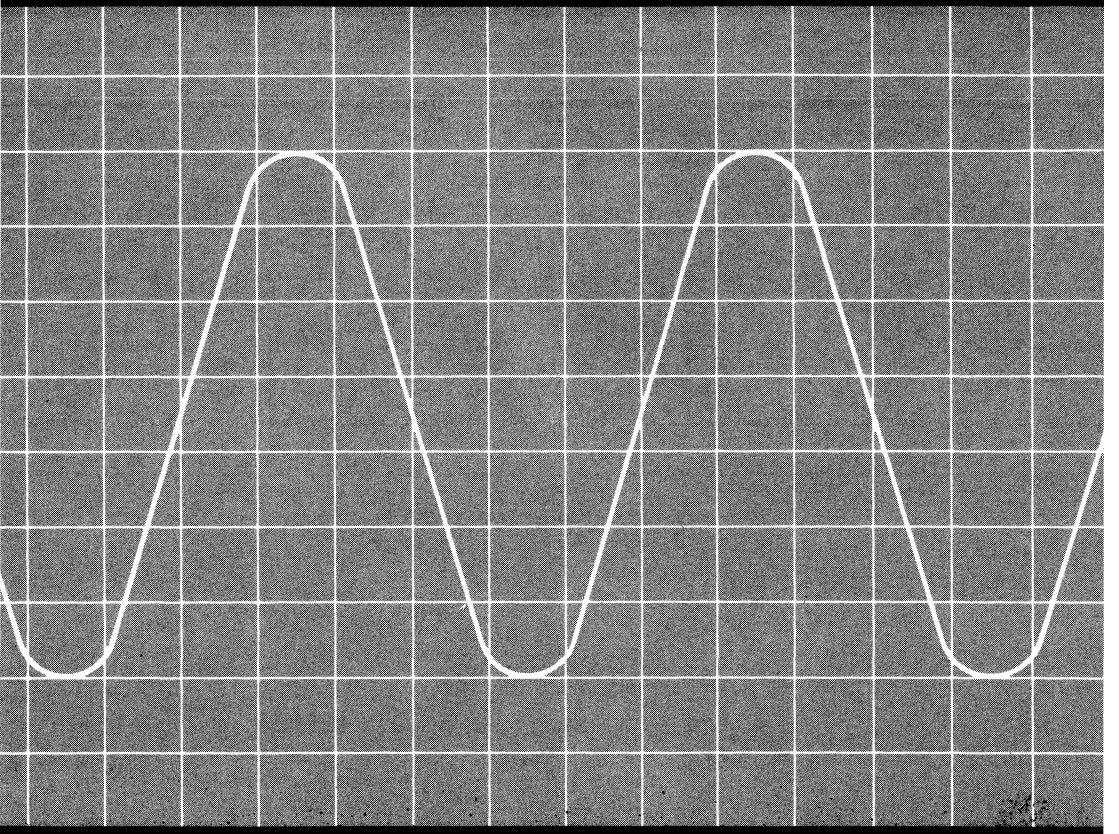
TEA 7031
MONITOR AMPLIFIER

APPLICATION NOTE AN-056



THOMSON
COMPONENTS
SEMICONDUCTEURS

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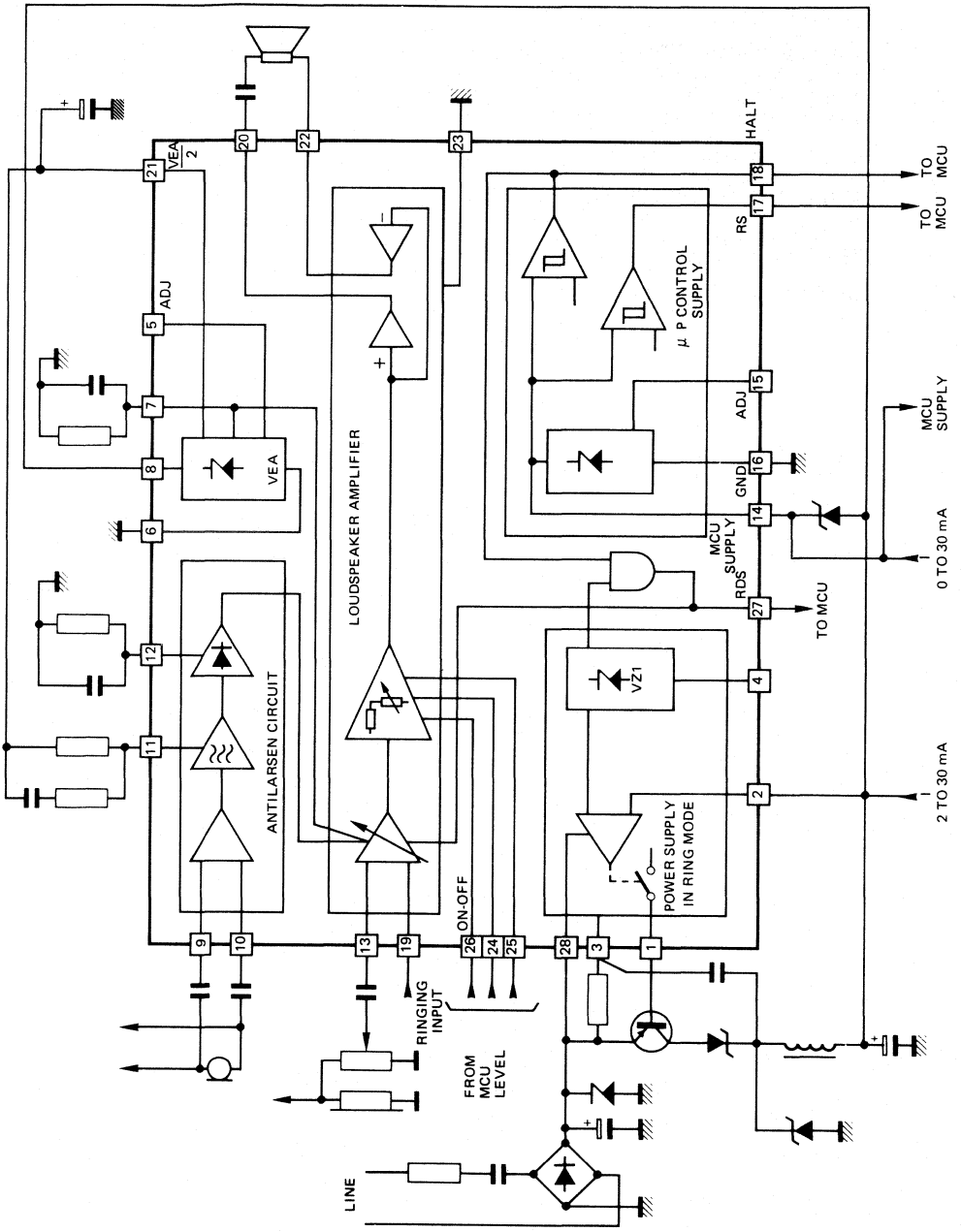
BLOCK DIAGRAM



TEA7031 circuit offers a low-cost design solution, employing a minimum of external components for loudspeaker-type telephone sets and other applications where amplified monitoring is needed.

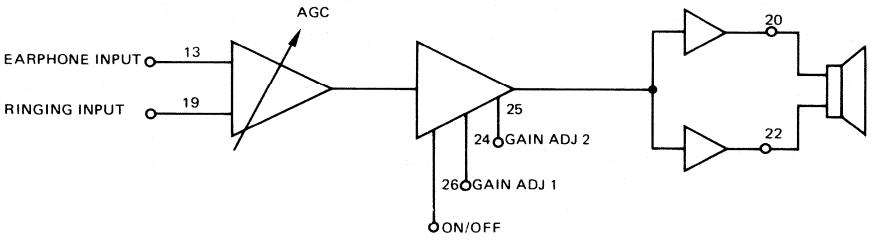
1 — DESCRIPTION

TEA7031 I.C. is a 28-pin DIL integrated circuit providing the following facilites:

- Loudspeaker amplifier.
- Anti-acoustic feed-back system (anti-Larsen system).
- Microprocessor supply and control.
- Switching regulator control.

These facilities are generally electrically separated; hence selective use of the functions provided is possible.

1.1 — Loudspeaker amplifier



The amplifier is divided into 3 main sections:

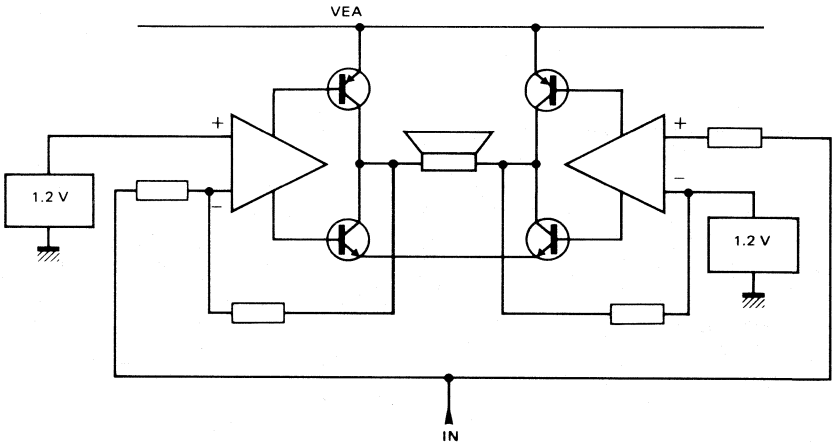
a) Automatic Gain Control (AGC).
b) Preamplifier.
c) Push-pull amplifier (bridge structure).

a) The AGC section is used for the anti-Larsen and anti-distortion system.

- When used in a telephone set to avoid Larsen effect the AGC automatically decreases loudspeaker amplifier gain.
- When the required output level exceeds the capabilities of the available current, the AGC decreases the loudspeaker amplifier gain to avoid distortion.

b) The preamplifier permits step control of amplifier gain in steps of 6 dB, using pins GAIN ADJ 1 and 2, which may be controlled using switches or by a microprocessor.
The amplifier may be muted using the ON/OFF control signal (pin 26).

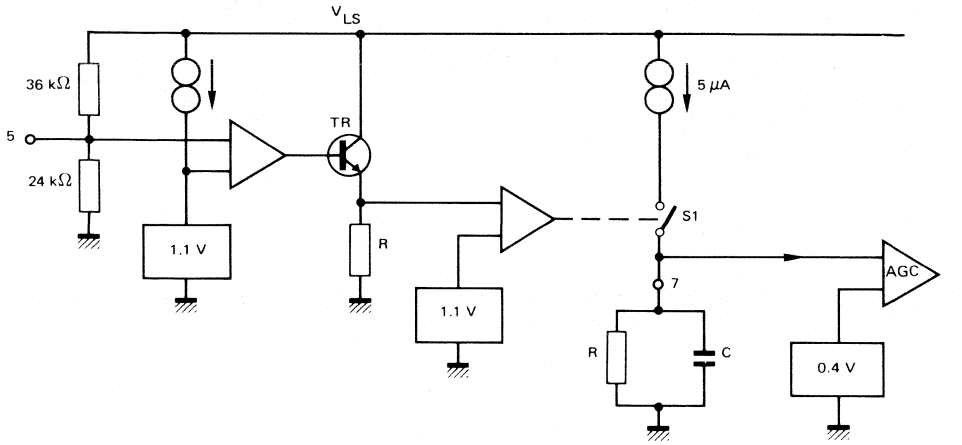
c) The output amplifier uses a double push-pull configuration (H bridge) to get maximum dynamic range under limited supply conditions.



Amplifier DC supply

In transmission mode, the supply voltage is controlled by the internal shunt DC regulator. For this reason, the TEA7031 should be supplied from a current source (see: supply considerations).

An anti-distortion system is embodied which provides AGC control to avoid loudspeaker distortion under current-limited conditions.



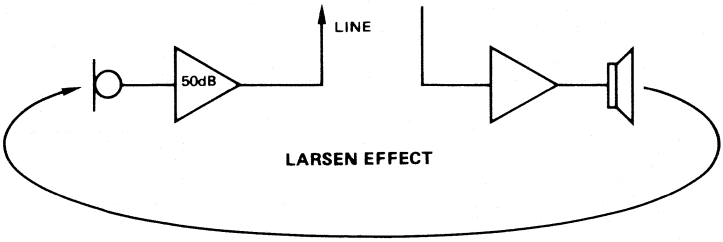
Circuit action

When the supply voltage is unsufficient, the voltage at pin 5, falls below the reference voltage 1.1 V, resulting in transistor (TR) being switched off, resulting in zero current flow in resistor R. This state enables the gain control system. Under these conditions, the shunt DC supply will switch at a rate determined by the time constant of the RC network on pin 7.

This switching action accomodates normal speech characteristics under low supply conditions.

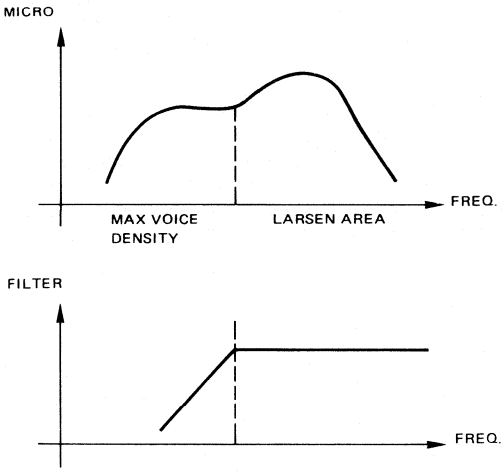
1.2 — Antiacoustic feedback system (antilarsen system)

The purpose of this system is to control AGC action, in order to avoid acoustic feedback between the loudspeaker and the microphone, when used in a telephone set.

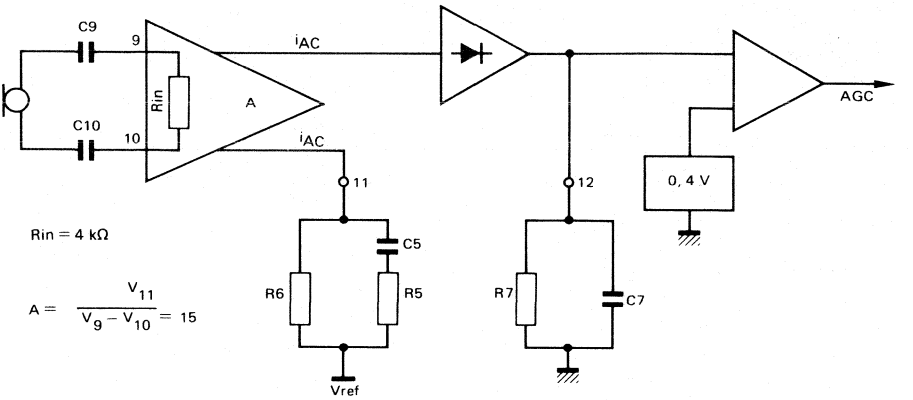


Principal of operation

When examining, the spectral density of the voice area and the Larsen area, it may be seen that the dominant features of each exist in different frequency bands.



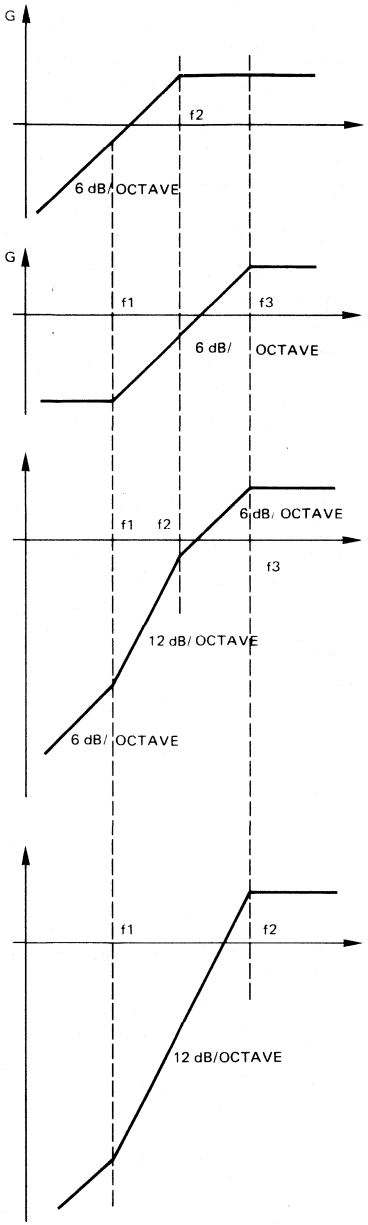
To extract the Larsen component, the microphone signal is first filtered by a second order filter (formed by two first order filters), then amplified and rectified in order to produce the AGC control signal.



$$i_{AC} = \frac{V_{pin\ 11}}{Z_{pin\ 11}} \quad \text{with} \quad \frac{1}{Z_{pin\ 11}} = \frac{1}{R6} + \frac{1}{R5 + \frac{1}{C5j\omega}}$$

$$V_{DC\ pin\ 12} = \frac{i_{AC\ (RMS)} \cdot 2\sqrt{2}}{\pi} \cdot R7$$

The first filter is generated by the capacitors on pins 9 and 10 and the input resistor Rin; the second filter by the RC network on pin 11.



- Filter on pins 9-10:

$$f2 = \frac{C9 + C10}{2\pi.Zin.C9.C10}$$

- Filter on pin 11:

$$f1 = \frac{1}{2\pi\,(R6 + R5)\,C5}$$

$$f2 = \frac{1}{2\pi\,R5\,C5}$$

- Anti-Larsen system filter response.

- Theoretical result.
  If f2 = f3 the anti-Larsen system filter is equivalent to a second order filter.

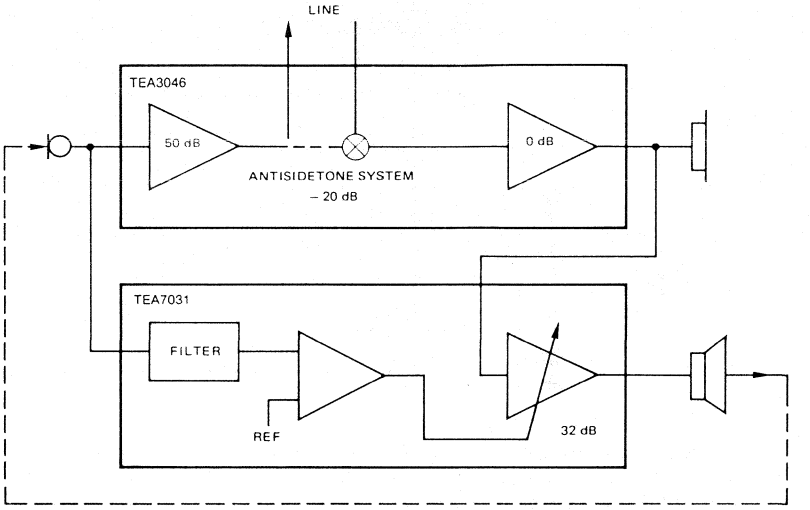
$$f2 = f3$$

$$\frac{C9 + C10}{2\pi.Zim.C9.C10} = \frac{1}{2\pi\,R5C5}$$

A complete telephone set has two anti-Larsen systems:

- one in the transmission circuit (for example: TEA3046 - TEA7050 - TEA7047) antisidetone network;
- one in the loudspeaker amplifier (for example: TEA7031).

Together these form a high efficiency anti-Larsen system.

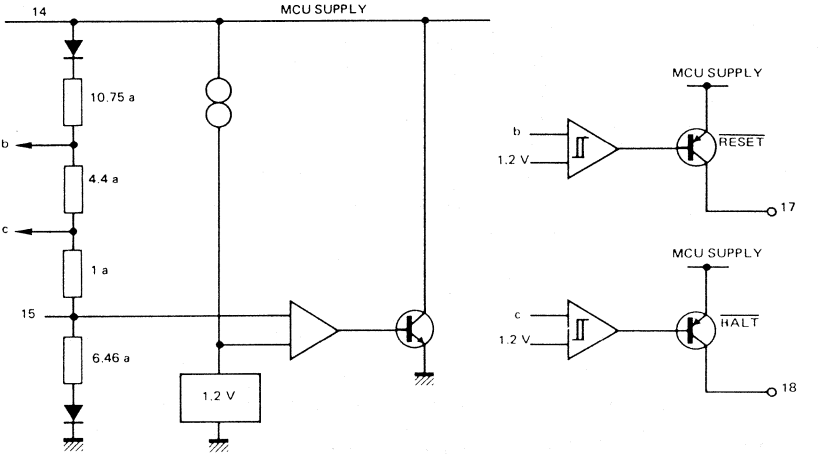


1.3 — Microprocessor control

TEA7031 provides the following signals for an associated microprocessor:

- halt and reset signal,
- a regulated supply.

The MCU shunt supply voltage is internally fixed at 3.2 V but can be adjusted via pin 15.

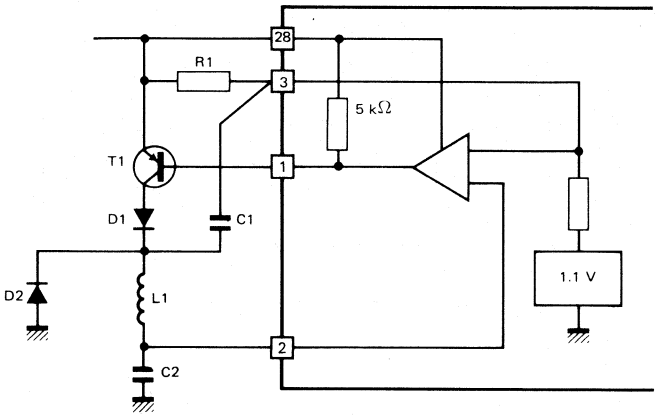


$2\ k\Omega < a < 8\ k\Omega$.

Note: Reset and Halt outputs, which are open collector outputs, require external resistors to zero volt .

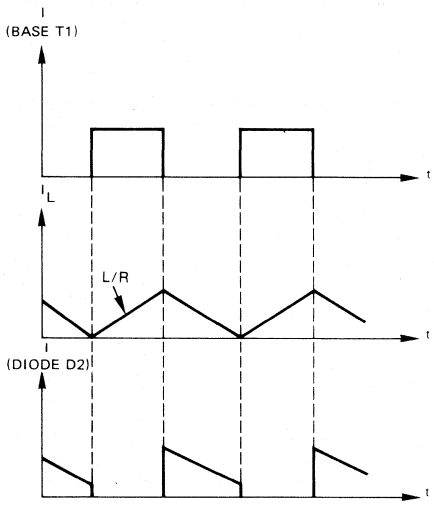
1.4 — Switching converter

Under ringing conditions the line supply available has a high voltage (≃ 22 V), low current (≃ 6 mA) characteristic. In order to be used by the I.C., this supply has to be converted to a low voltage (≃ 3.5 V) and higher current (15 — 20 mA), using a switching converter.



Transistor T1 is switched either ON/OFF via pin 1 in accordance with the result of a comparison between an internal reference voltage and the I.C. supply voltage (pin 2). When transistor T1 is off, the diode D2 provides a return current path for L1.

Under speech conditions, the switching converter has to be isolated from the main supply VLS by D1, to prevent reverse current.



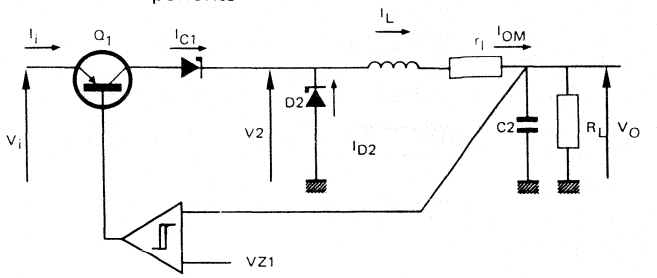
Internal conditions during switching converter operation:

- the internal zener diodes VLS, MCU supply are automatically disconnected,
- the Earphone input is OFF and ringing input is ON.

Note: For better converter efficiency, it is advisable to use schottky diodes for D1 and D2.

Switching power supply efficiency

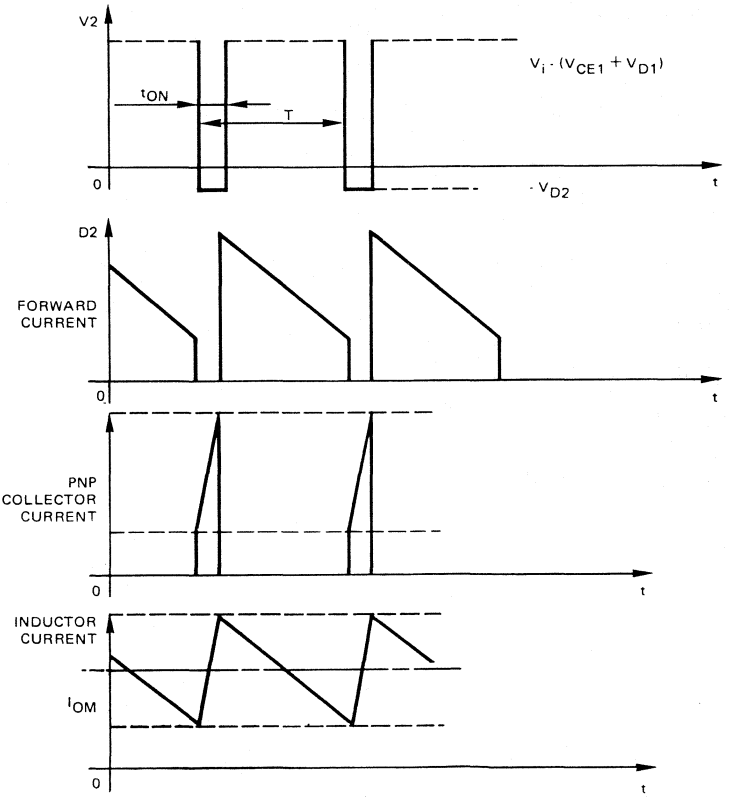
Contribution of external components



Equivalent drawing:

Efficiency calculation hypotheses:

- I_{OM} average output current
- $R_L \cdot C_2 \gg T$. T = switching period
- Duty cycle $\tau_r = \frac{t_{on}}{T}$
- Be careful that resonance frequency of L.C_2 must be lower than switching frequency.



If Po = load output power
Pe = input power

If Ppo = dissipated power in D2 and L
Ppe = dissipated power in Q_1 and D1

$$Po = Pe - Ppo - Ppe$$

The efficiency is $\rho = \frac{Po}{Pe} = 1 - \frac{Ppo + Ppe}{Pe}$

Dissipated power in D2 and L

$$Ppo \cdot (V_{D2} + r\rho \cdot I_{OM}) \cdot I_{OM} (1 - \tau_r)$$

V_{D2} = forward voltage of D2

Dissipated power in Q_1 and D1

$$Ppe = (V_{D1} + V_{CES1}) \cdot I_{OM} \cdot \tau_r$$

V_{D1} = forward voltage of D1

V_{CES1} = Saturation voltage (at $I_C = I_{OM}$) of Q1

Relation between ρ and τ_r

$$\tau_r = \frac{Vo}{Vi} \cdot \frac{1}{e} \quad \text{detail} \begin{cases} Po = \rho \cdot P\rho \\ Vo, I_{OM} = \rho \cdot I_{OM}\, Vi \cdot \tau_r \end{cases}$$

$$\rho = \frac{Vo}{Vi} = \frac{Vi - (V_{D1} + V_{CES1}) + V_{D2} + r\rho \cdot I_{OM}}{Vo + V_{D2} + r\rho \cdot I_{OM}}$$

Numeric application

$I_{OM} = 25$ mA $\quad V_o = 3.5$ V $\quad \begin{cases} V_{CES1} = 0.25 \text{ V} \\ \text{AT } I_C = 25 \text{ mA} \end{cases}$

$re = 3.2 \quad V_{D2} = 0.3$ V

$V_i = 21$ V $\quad V_{D1} = 0.4$ V

$\rightarrow \rho = 0.85$

NOTE: Currents flowing inside the circuit through pin 3 and pin 28 have not been taken in account.

It can be evaluated at:

$$I_{pin\ 3} = (V_i - V_o) \cdot \frac{1}{R1}$$

$$I_{pin\ 28} = \frac{(V_o - 1.5)}{10^5} \cdot 4$$

for $V_o = 3.5$ V $\quad I_{pin28} = 80\ \mu A$

2 — PIN FUNCTIONS

PIN 1: SWITCHING CONVERTER DRIVE OUTPUT:
Base drive output for the external PNP switching transistor in the switching converter.
This switching transistor should have the following characteristics:

$V_{CEO} > 30$ V

$I_C > 200$ mA

$G_{min} > 100$

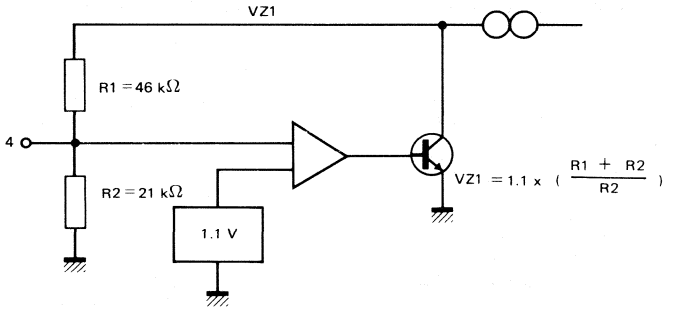
$f_T \geqslant 1$ MHz

Suitable transistors:
BC308 - BC559 - BCW93 - BC327

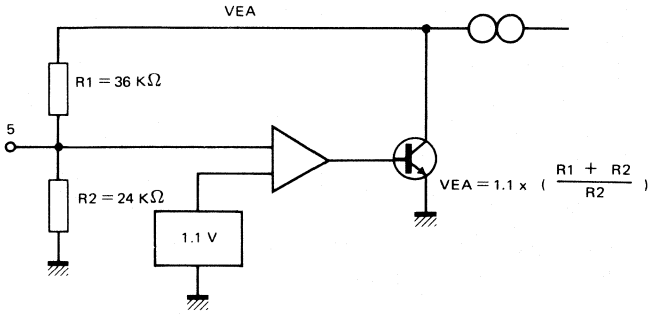
PIN 2: SWITCHMODE POWER SUPPLY REGULATION INPUT:
This input provides the voltage sensing feedback input to the switching converter.

PIN 3: VZ1: REF. VOLTAGE TO SWITCHING CONVERTER COMPARATOR:
With pin 4 open circuit, VZ1 is internally stabilized at 3.5 V.

PIN 4: ADJUST VZ1:
This pin is used to adjust the switching converter power supply reference voltage.

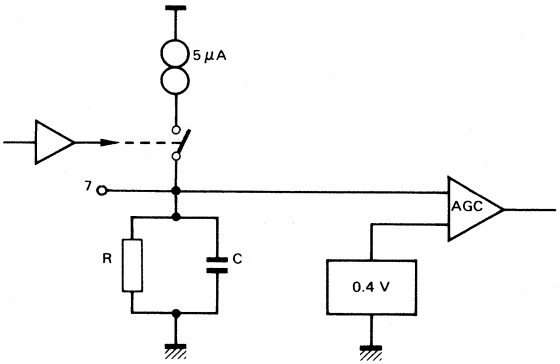


PIN 5: ADJUST VLS:
This pin is used to adjust the I.C. supply voltage.

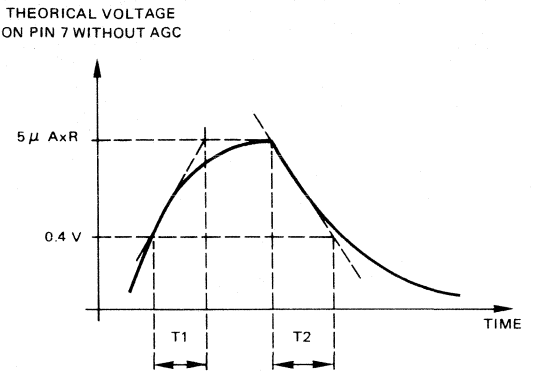


PINS 6 - 16 - 23: GROUND:
These pins have to be connected together.

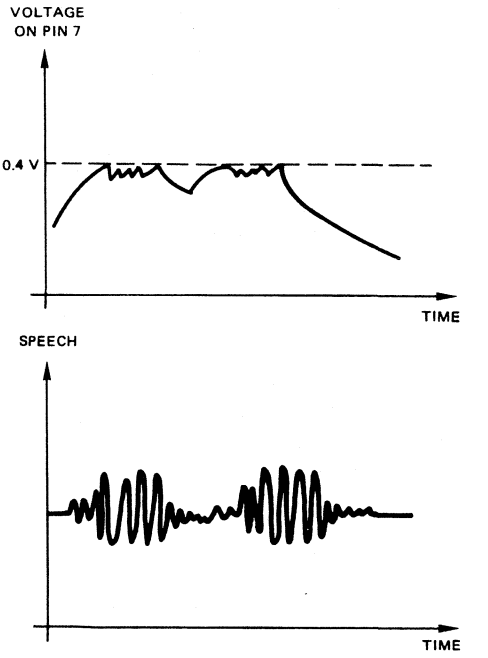
PIN 7: AUTOMATIC GAIN CONTROL FILTER:
The anti-distortion system response is adjusted by the RC network on this pin.



The AGC will be switched ON when the level on pin 7 is greater than the reference voltage (0.4 V), the RC network charges (current source ON) or discharges (current source OFF) according to the supply voltage.



- The value of R affects the system time constant and the charge/discharge duty cycle.
- The value of C only affects the system time constant.
  R should be greater or equal than 150 kΩ for correct AGC operation.

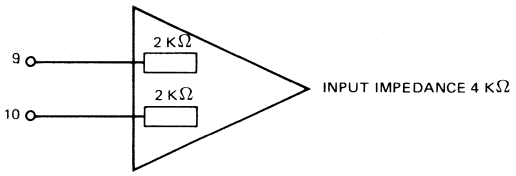


PIN 8: CIRCUIT SUPPLY VOLTAGE:

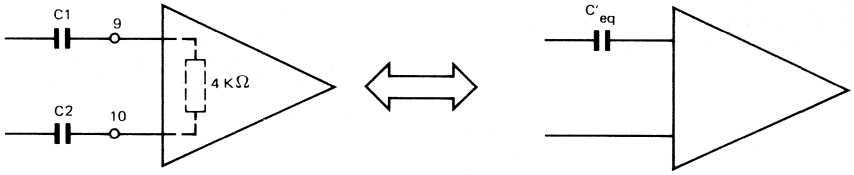
With pin 5 open circuit, VLS is internally stabilized at 2.8 V.
When the TEA7031 is under AGC control, the voltage on this pin varies slightly (due to AGC action).

PIN 9/10: MICROPHONE INPUTS:

These are used for anti-Larsen control.



The capacitors fitted to these pins constitute one of the two filters of the antilarsen system (2nd filter: pin 11).
In order to obtain a 2nd order filter for the antilarsen system, the cut off frequency set by these capacitors and that set by the filter at pin 11 should be the same.
If two capacitors are connected to pin 9 and 10 they are considered to be in serie.



$$C'eq = \frac{C1 + C2}{C1 + C2}$$

Ex:

fc = 1.5 kHz Zin = 4 kΩ

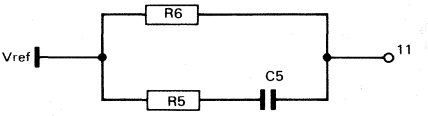
$$Fc = \frac{1}{2\pi \, Zin \, C \, eq}$$

$$Céq = \frac{1}{2\pi \, Zin \times Fc} = \frac{1}{2\pi \times 4 \, k \times 1.5 \, k} \simeq 26 \text{ nF}$$

C1 = C2 = 52 nf.

PIN 11: ANTI-LARSEN FILTER 1

The second filter of the anti-Larsen system (1st fiter: pins 9-10) is formed by the RC network R5C5. In order to obtain a second order filter for the anti-Larsen system, the cut-off frequency defined at this pin, should be the same as that chosen for the first filter.



For correct TEA7031 operation R6 and R5 should be fixed at 10 kΩ and 1 kΩ respectively.

Ex:

Fc = 1.5 kΩ

$$C_5 = \frac{1}{2\pi \, R5 \, Fc} = \frac{1}{2\pi \, 1k \times 1.5 \, k} \simeq 110 \text{ nF}$$

PIN 12: ANTI-LARSEN FILTER 2:

The gain and the response of the anti-Larsen system can be adjusted respectively by the resistor and the capacitor on this pin, according to the acoustic characteristics of the telephone set.
The value of the resistor should not exceed 390 kΩ. When the voltage on this pin exceeds the threshold voltage of 0.4 V, the AGC system is enable.

PIN 13: EARPHONE INPUT

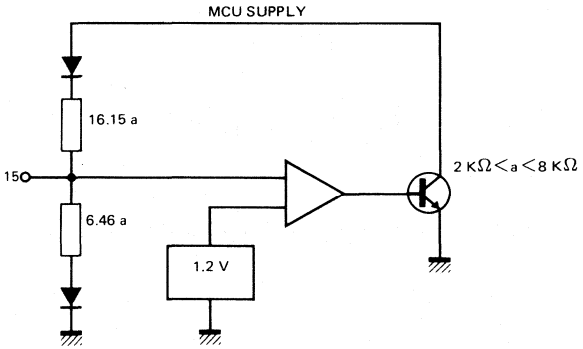
Input for loudspeaker signal. This input is only active in transmission mode, but not in ringing mode; in ringing mode, input pin 19 should be used for amplification of ringing tones. In transmission mode no signal should applied on pin 19, for a proper working of the I.C.

PIN 14: MICROPROCESSOR SUPPLY VOLTAGE

With pin 15, open circuit, MCU supply is internally stabilized at 3.3 V, and is available for microprocessor supply purposes.

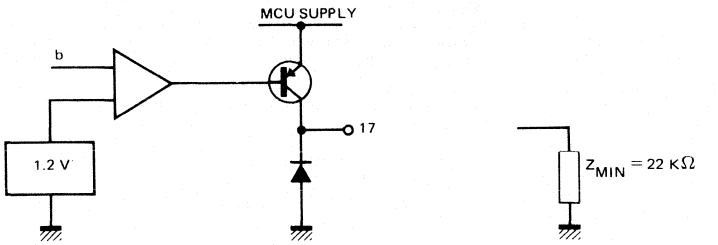
PIN 15: MCU SUPPLY ADJUST

This pin is used to adjust the microprocessor supply voltage.



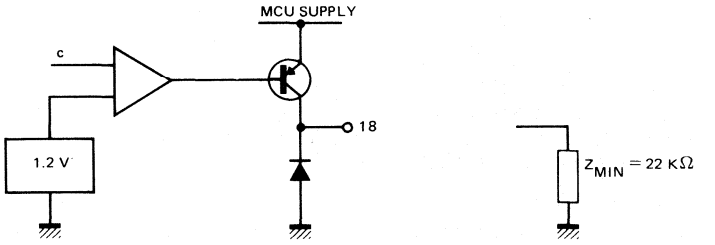
PIN 17: MICROPROCESSOR RESET OUTPUT

This output is an open collector output which delivers a reset signal for a microprocessor.



PIN 18: MICROPROCESSOR HALT OUTPUT

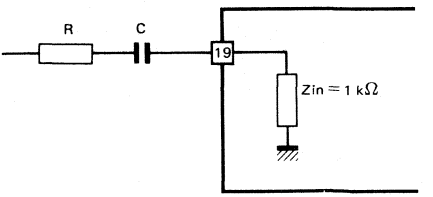
This output is an open collector output with delivers a halt signal for a microprocessor.



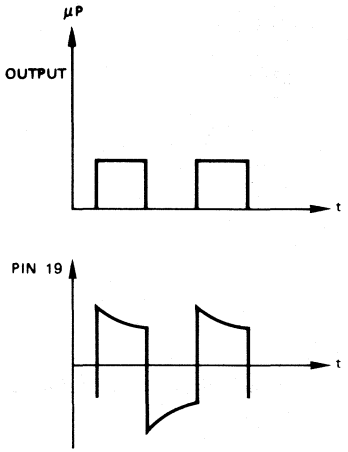
PIN 19: SQUARE WAVE RINGING MELODY SIGNAL INPUT

Input for loudspeaker signal.

This input is only active in ringing mode (when supplied by the switching supply). In transmission mode (when supplied by the shunt DC supply), input 13 should be used and no signal should be applied on pin 19. In ringing mode, it could be used, for example, to generate the microprocessor melody.



For greater efficiency, the microprocessor square wave signal is differentiated; the input signal is adjusted by the resistor R.



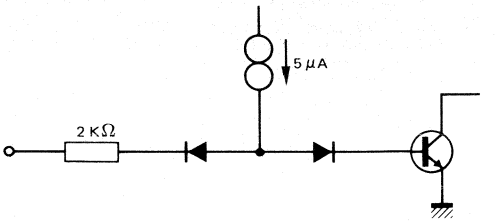
PINS 20-22: LOUDSPEAKER OUTPUTS

Outputs to be connected to a 50 Ω impedance loudspeaker.
Output voltage: Vpp = 2 VLS —2.5 volts (with a gain of 32 dB).
Maximum current: depending of the supply voltage.

PIN 21: V_{ref}: INTERNAL REFERENCE

Output which provides an internally regulated reference voltage.
V_{ref} = 1.1 V typical.
MAXIMUM AVAILABLE CURRENT: 5 μA.

PINS 24-25: GAIN ADJUSTMENT INPUTS

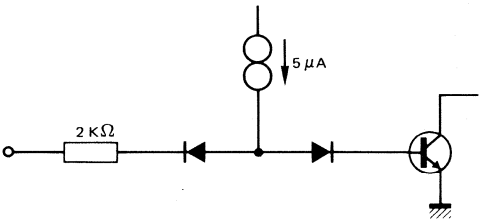


These pins are used to adjust the loudspeaker amplifier gain. Four steps of 6 dB/step are available (pin open circuit = high level).

GAIN ADJUSTMENT INPUTS

GAIN ADJ 1	GAIN ADJ 2	
1	1	G_{MAX}
1	Ø	G_{MAX} - 6 dB
Ø	1	G_{MAX} - 12 dB
Ø	Ø	G_{MAX} - 18 dB

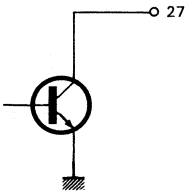
PIN 26: LOUDSPEAKER MUTING



This pin is used to mute the loudspeaker. Pin open-circuit = high level = loudspeaker muted. Pin low level = loudspeaker enabled.

PIN 27: RING SIGNAL INDICATION

This NPN open collector output provides ready status when in ringing condition.
DS is ON (low-level) when the switching converter is established in the running state and when the microprocessor supplies are stabilized. The DS signal is validated by "Halt".
It may be used to cause an associated microprocessor to generate the ringing tones.



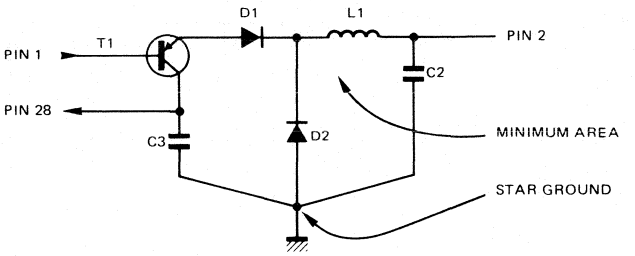
PIN 28: RECTIFIED RING SIGNAL INPUT

High voltage input for the switching converter.
Maximum voltage: 22 V.

3 — SUPPLY CONSIDERATIONS

3.1 — Switching supply lay-out

To avoid switching-noise, C2, C3, D2 should be tied together as close as possible.



3.2 — TEA7031 supply

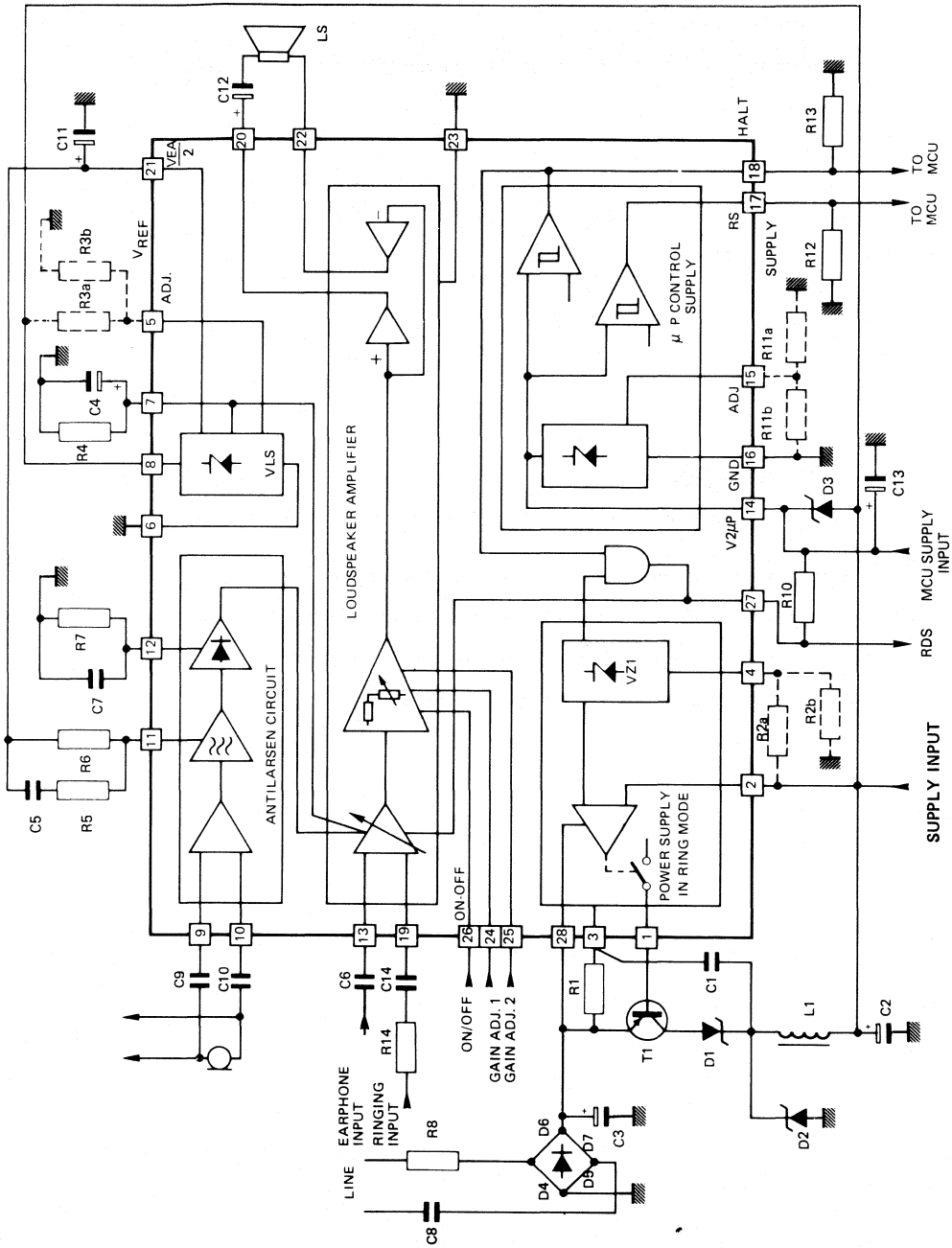
As the I.C. has a zener characteristic, it should be supplied by a current source.

Constant voltage supply:
The TEA7031 can be supplied by an external constant voltage on condition:

- To set the zener voltages at a level higher than the supply voltage.
- To tie the automatic gain control pin (pin 7) to the ground (otherwise the I.C. will always be in AGC mode).

Note: The maximum loudspeaker level is depending of the supply voltage.

4 — TYPICAL APPPLICATION



RESISTORS:

R1 : 22 kΩ
R2 :
R3 :
R4 : 470 kΩ
R5 : 1 kΩ
R6 : 10 kΩ
R7 : 330 kΩ
R8 : 1 kΩ/1W
R9 : (5 kΩ)
R10: 100 kΩ
R11:
R12: 100 kΩ
R13: 100 kΩ
R14: 47 kΩ

CAPACITORS:

C1 : 22 pF
C2 : 220 μF/10 V
C3 : 10 μF/35 V
C4 : 10 μF/10 V
C5 : 68 nF
C6 : 220 nF
C7 : 470 nF
C8 : 1 μF/250 V
C9 : 33 nF
C10: 33 nF
C11: 33 μF/10 V
C12: 22 μF
C13: 33 μF/10 V
C14: 1.5 nF

DIODES:

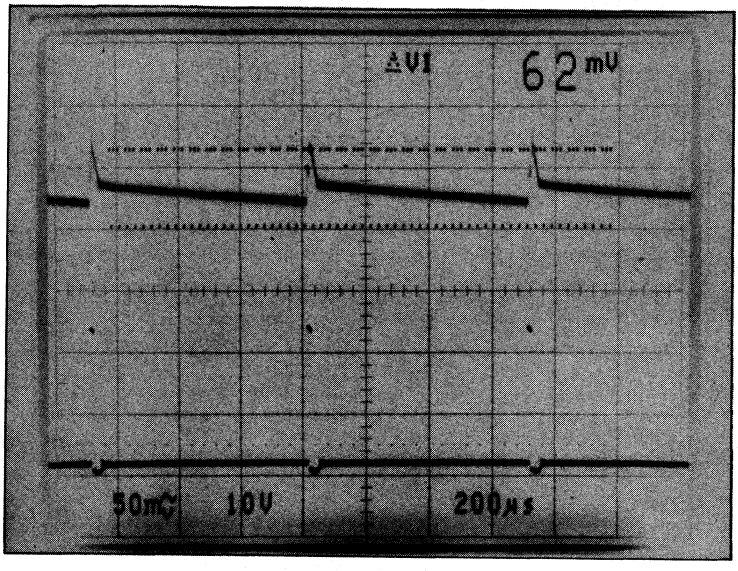
D1: BAT43
D2: BAT43
D3: BAT43
D4: 1N4004
D5: 1N4004
D6: 1N4748-BZX 85C (22 V)
D7: 1N4748-BZX 85C (22 V)

INDUCTOR:

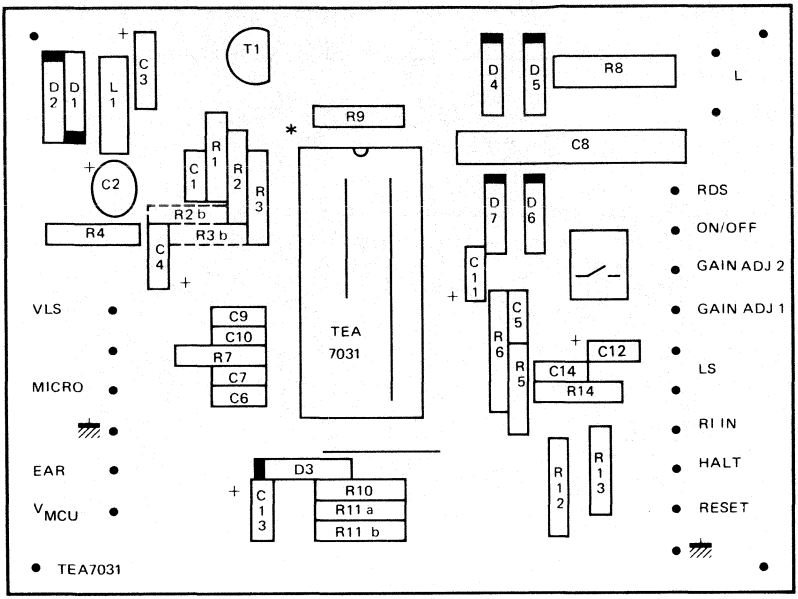
L1: 470 μH - 680 μH

TRANSISTOR:

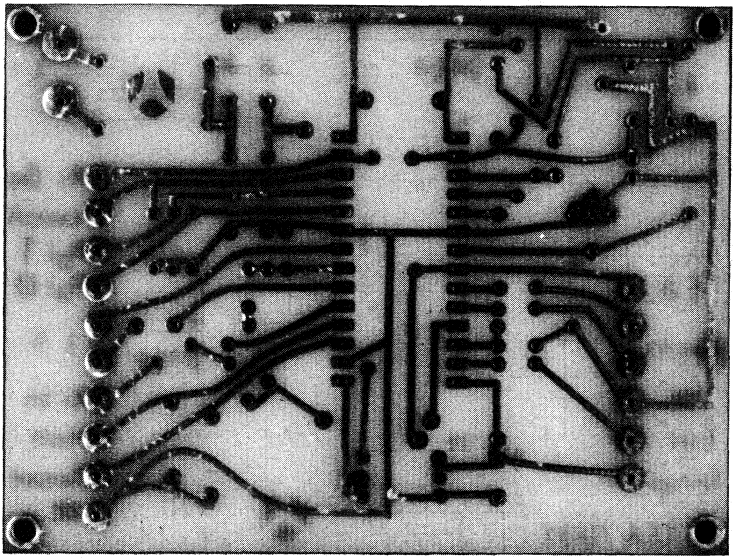
T1: BCW93 - BCW92



This figure shows the working of the switching converter.
Top: stabilized voltage (in AC): 50 mV/DIV.
Bottom: pulses driving the PNP transistor base 10 V/DIV.
Time Base: 200 μs.


T1
C3
D2
D1
L1
C2
R1
R2
R3
C1
R2 b
R3 b
R4
C4
R9
TEA
7031
C9
C10
R7
C7
C6
D3
C13
R10
R11 a
R11 b
D4
D5
R8
L
C8
D7
D6
C11
C5
R6
R5
C12
C14
R14
R12
R13
VLS
MICRO
EAR
V_{MCU}
TEA7031
RDS
ON/OFF
GAIN ADJ 2
GAIN ADJ 1
LS
RI IN
HALT
RESET

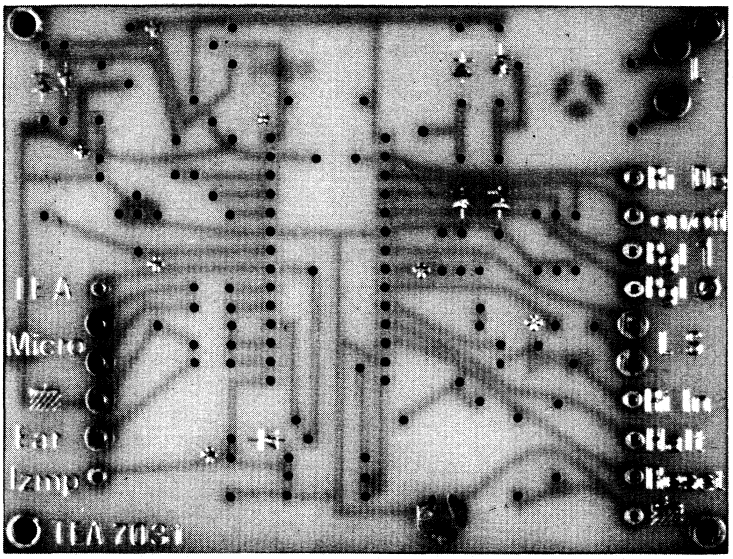
Component side



IEA VLS
Izmp V_{MCU}

Ri De=RDS
Pgl 1=G.adj 2
Pgl 0=G.adj 1

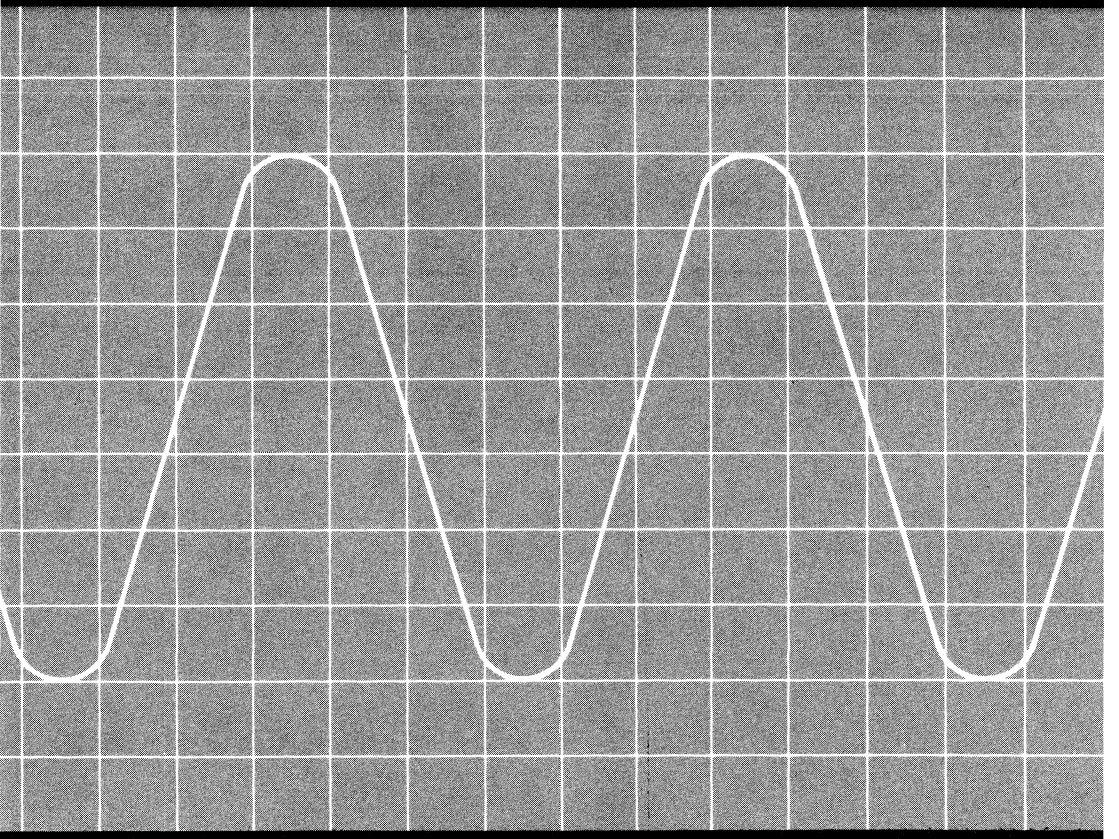
Copper side



These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

TEA 7531
MONITOR AMPLIFIER

APPLICATION NOTE AN-065

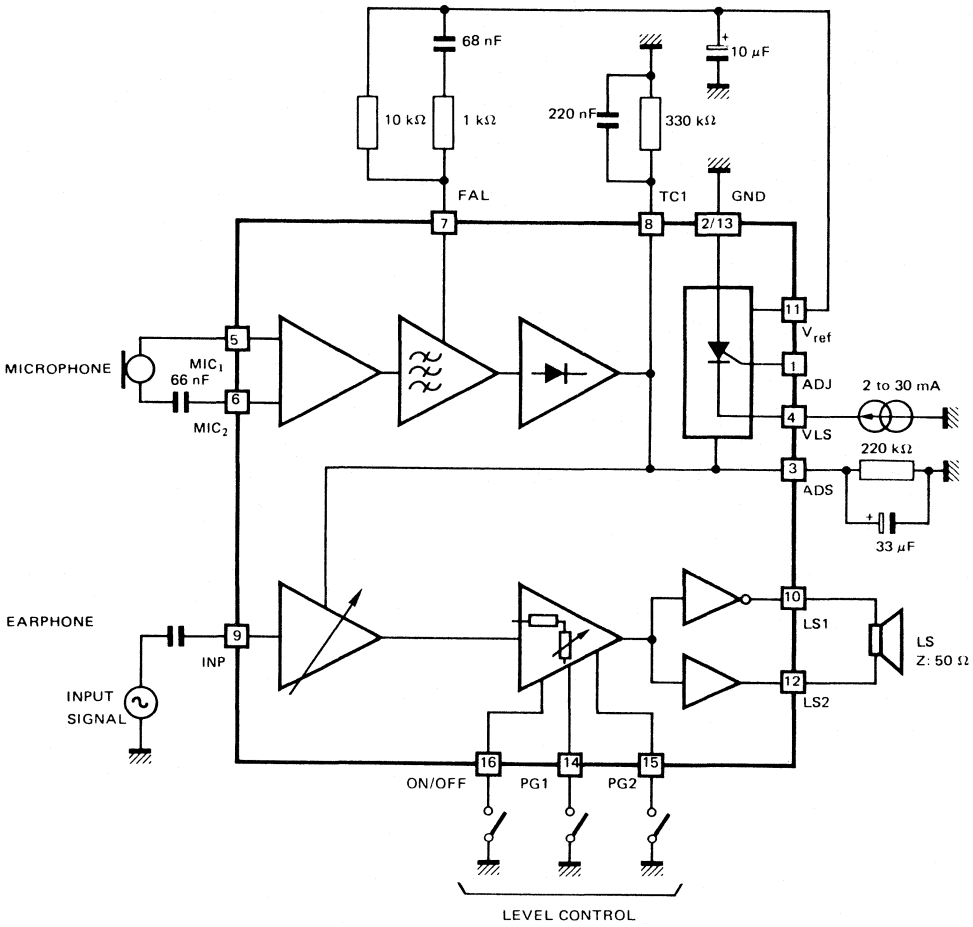


THOMSON
COMPONENTS
SEMICONDUCTEURS

TABLE OF CONTENTS

TEA 7531 circuit offers a low-cost design solution, employing a minimum of external components for loudspeaker-type telephone sets and other applications where amplified monitoring is needed.

BLOCK DIAGRAM

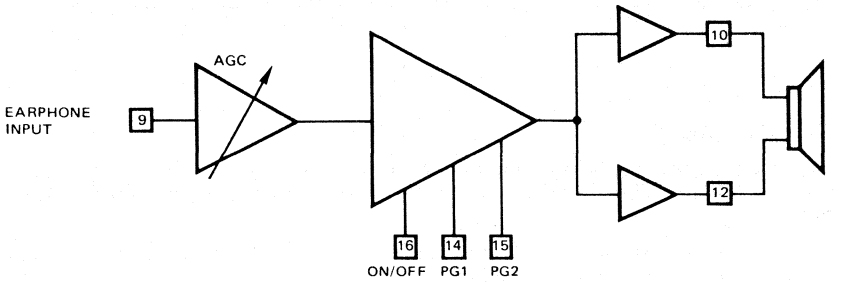


1 — DESCRIPTION

TEA 7531 I.C. is a 16 pin DIL integrated circuit providing the following facilities:

- Loudspeaker amplifier.
- Antiacoustic feed-back system (antilarsen system).

1.1 — Loudspeaker amplifier



The amplifier is divided into 3 main sections.

- Automatic Gain Control (AGC).
- Preamplifier.
- Push-pull amplifier (bridge structure).

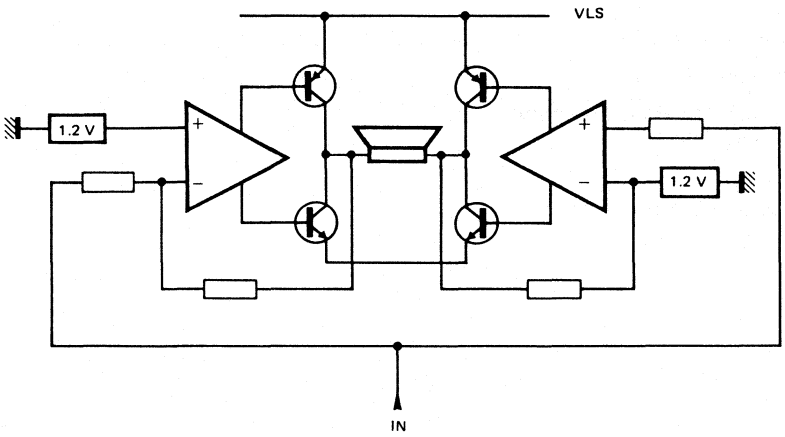
a) The AGC section is used for the antilarsen and antidistortion system.

. When used in a telephone set to avoid larsen effect the AGC automatically decreases loudspeaker amplifier gain.

. When the required output level exceeds the capabilities of the available current, the AGC decreases the loudspeaker amplifier gain to avoid distortion.

b) The preamplifier permits step control of amplifier gain in steps of 6 dB, using pins PG1 and PG2, which may be controlled using switches or by a microprocessor. The amplifier may be muted using the ON/OFF control signal (pin 16).

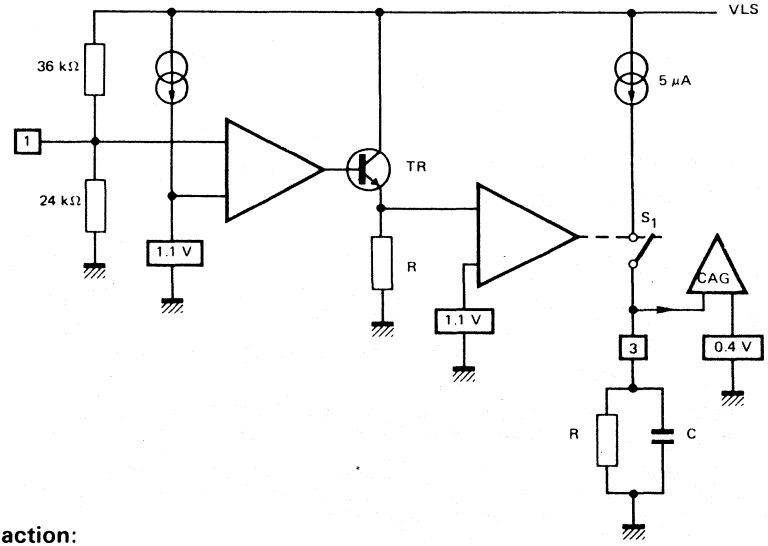
c) The output amplifier uses a double push-pull configuration (H bridge) to get maximum dynamic range under limited supply conditions.



Amplifier DC supply:

In transmission mode, the supply voltage is controlled by the internal shunt DC regulator. For this reason, the TEA 7531 should be supplied from a current source (see: supply considerations).

An antidistortion system is embodied which provides AGC control to avoid loudspeaker distortion under current-limited conditions.



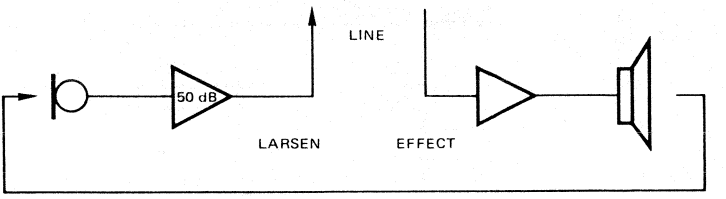
Circuit action:

When the supply voltage is insufficient, the voltage at pin 1, falls below the reference voltage 1.1 V, resulting in transistor (TR) being switched off, resulting in zero current flow in resistor R. This state enables the gain control system. Under these conditions, the shunt DC supply will switch at a rate determined by the time constant of the RC network on pin 3.

This switching action accomodates normal speech characteristics under low supply conditions.

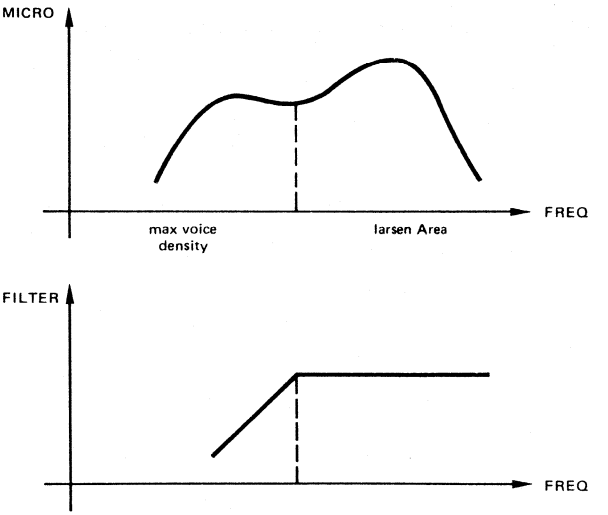
1.2 — Antiacoustic feed-back system (antilarsen system)

The purpose of this system is to control AGC action in order to avoid acoustic feed-back between the loudspeaker and the microphone, when used in a telephone set.

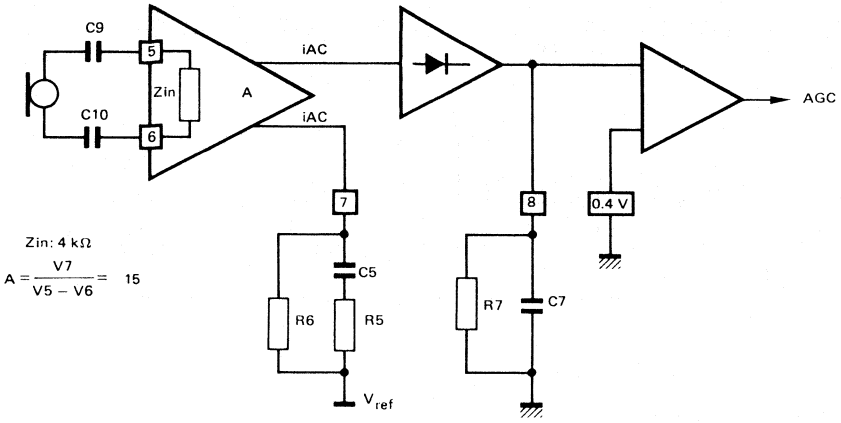


Principal of operation

When examining the spectral density of the voice area and the larsen area, it can be seen that the dominant features of each exist in different frequency bands.

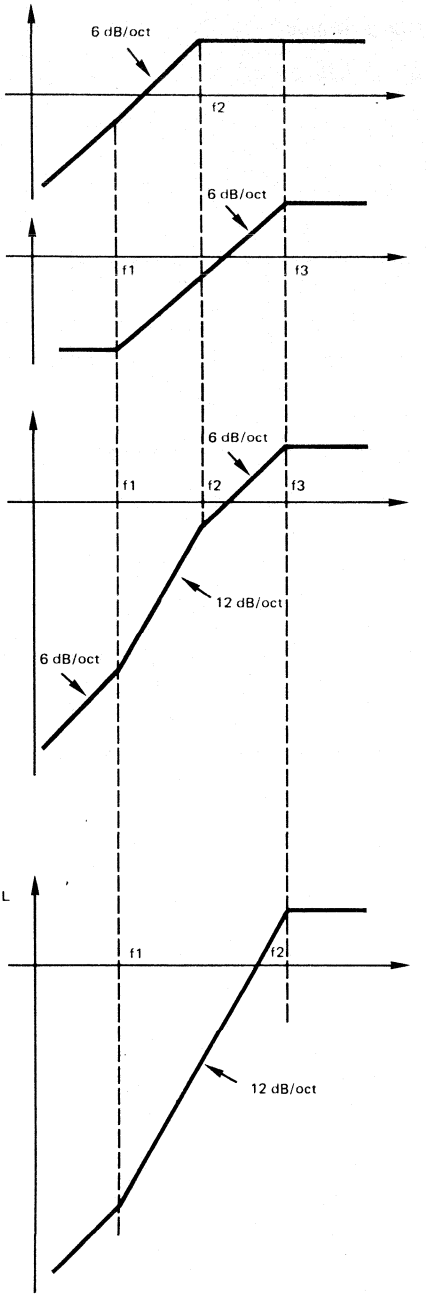


To extract the larsen component, the microphone signal is first filtered by a second order filter (formed by two first order filters), then amplified and rectified in order to produce the AGC control signal.



The first filter is generated by the capacitors on pins 5 and 6; the second filter by the R-C network on pin 7.

ANTILARSEN SYSTEM FILTER RESPONSE



Filter on pins 5 & 6

$$f2 = \frac{C9 + C10}{2\pi \, Zin \, C9 \, C10}$$

Filter on pin 7

$$f1 = \frac{1}{2\pi \, (R5 + R6) \, C5}$$

$$f3 = \frac{1}{2\pi \, R5 \, C5}$$

Antilarsen system

Filter response

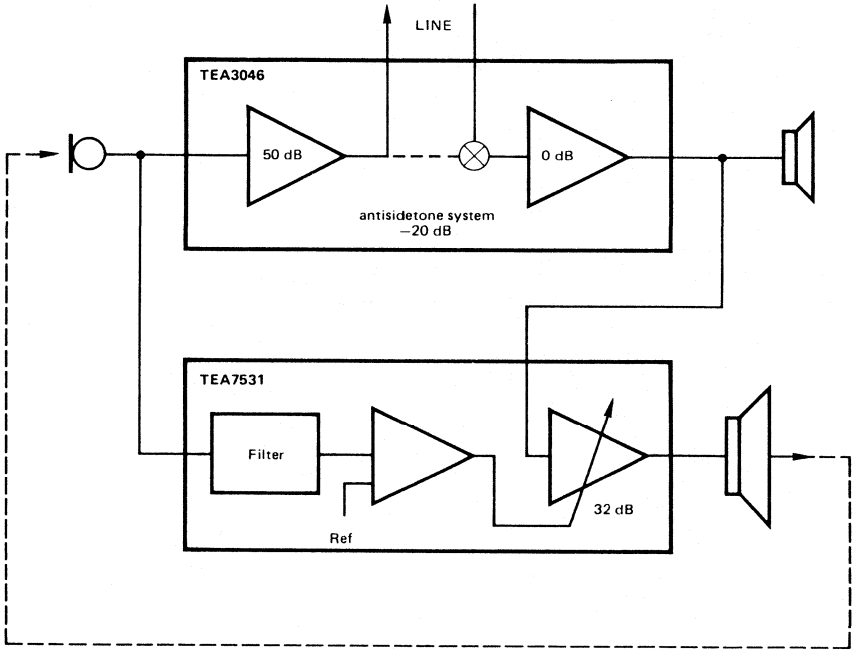
If f2 = f3 the Antilarsen system filter is equivalent to a second order filter

$$\frac{C9 + C10}{2\pi \, Zin \, C9 \, C10} = \frac{1}{2\pi \, R5 \, C5}$$

A complete telephone set has two antilarsen systems:

- one in the transmission circuit (for example: TEA 3046) antisidetone network;
- one in the loudspeaker amplifier (for example: TEA 7531).

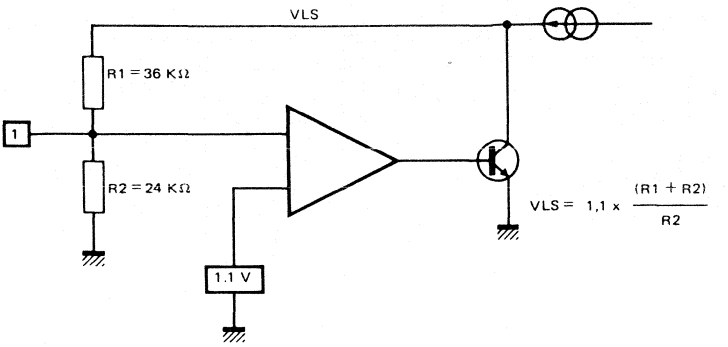
Together these form a high efficiency antilarsen system.



2 — PIN FUNCTIONS

Pin 1: adjust V_{LS}:

This pin is used to adjust the I.C. supply voltage.

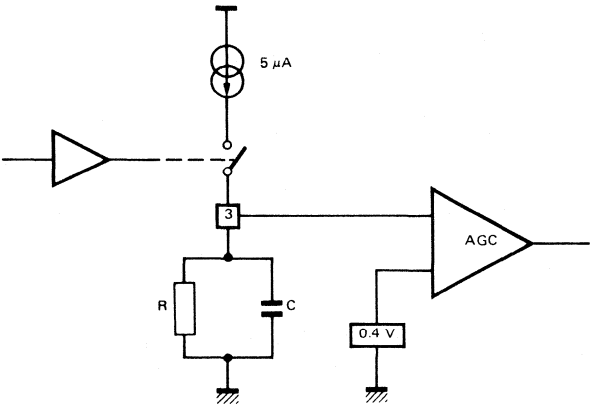


Pins 2-13 ground:

These pins have to be connected together.

Pin 3: automatic gain control filter

The antidistortion system response is adjusted by the R-C network on this pin.

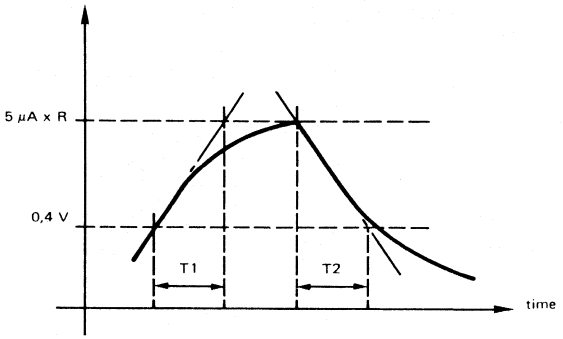


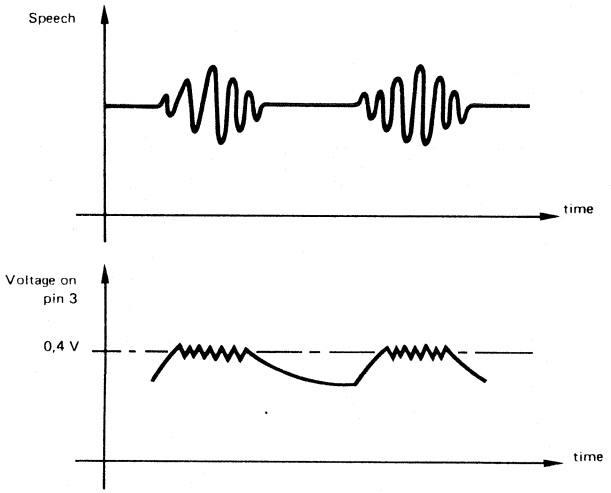
The AGC will be switched ON when the level on pin 3 is greater than the reference voltage (0.4 V), the RC-network charges (current source ON) or discharges (current source OFF) according to the supply voltage.

THEORETICAL VOLTAGE ON PIN 3

- The value of R affects the system time constant and the charge/discharge duty cycle.
- The value of C only affects the system time constant.

  R should be greater or equal than 150 kΩ for correct AGC operation.





AGC efficiency is given on chapter 3

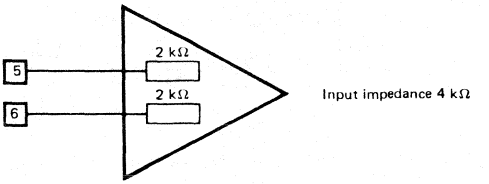
Pin 4: circuit supply voltage

With pin 1 open circuit, VLS is internally stabilized at 2.8 V.

When the TEA 7531 is under AGC control, the voltage on this pin varies slightly (due to AGC action).

Pin 5/6: microphone inputs:

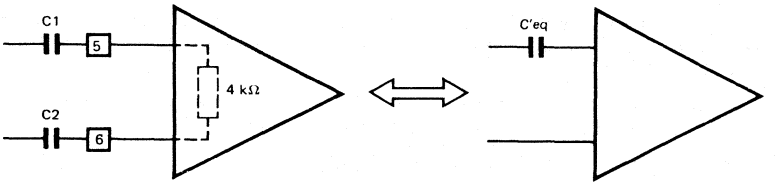
These are used for antilarsen control.



The capacitors fitted to these pins constitute one of the two filters of the antilarsen system (2nd filter: pin 7).

In order to obtain a 2nd order filter for the antilarsen system, the cut off frequency set by these capacitors and that set by the filter at pin 7 should be the same.

If two capacitors are connected to pin 5 and pin 6 they are considered to be in series.



$$C'eq = \frac{C1 \cdot C2}{C1 + C2}$$

Ex:

Fc = 1.5 kHz Zin = 4 kΩ

$$Fc = \frac{1}{2\pi \, Zin \, Ceq}$$

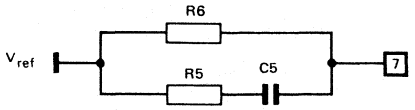
$$Ceq = \frac{1}{2\pi \, Zin \times Fc} = \frac{1}{2\pi \times 4\,k \times 1.5\,k} = 26 \text{ nF}$$

C1 = C2 = 52 nF

Pin 7: antilarsen filter 1

The second filter of the antilarsen system (1st filter: pins 5-6) is formed by the RC network R5C5.

In order to obtain a second order filter for the antilarsen system, the cut-off frequency defined at this pin, should be the same as that chosen for the first filter.



For correct TEA 7531 operation R6 and R5 should be fixed at 10 kΩ and 1 kΩ respectively.

Ex:

$$Fc = 1.5\ k\Omega$$

$$C5 = \frac{1}{2\pi\ R5\ Fc} = \frac{1}{2\pi \times 1\ k \times 1.5\ k} = 110\ nF$$

Pin 8: antilarsen filter 2

The gain and the response of the antilarsen system can be adjusted respectively by the resistor and the capacitor on this pin, according to the acoustic characteristics of the telephone set.

The value of the resistor should not exceed 390 kΩ. When the voltage on this pin exceeds the threshold voltage of 0.4 V, the AGC system is enabled.

Antilarsen system efficiency is given on chapter 3.

Pin 9: earphone input

Input for loudspeaker signal.

Pin 10-12: loudspeaker outputs:

Maximum output voltage: $V_{pp} = 2\ V_{LS}$ - 2.5 V (with a gain of 32 dB).

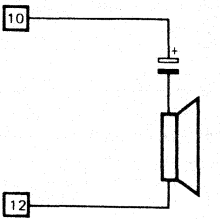
Maximum output current: depending of the supply current.

Two loudspeaker connection methods are possible, using the amplifier in either "H" mode or "B" mode.

Note: It is advisable to connect a 47 nF capacitor in paralell with the loudspeaker (Between pins 10 and 12)

- **"H" mode:**

  This is for low voltage working, but at a higher supply current. The highest output power is available in this mode, due to the 5.5 V maximum supply voltage restriction, imposed by the TEA 7531 (see curves on chapter 4).

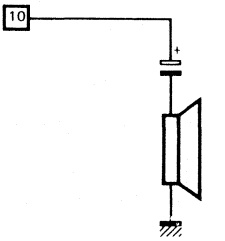


Loudspeaker impedance recommended value: 50 Ω.

Maximum gain available between earphone input and loudspeaker output: 32 dB.

- **"B" mode:**

This allows higher voltage operation, but at a lower supply current (see curves on chapter 4).



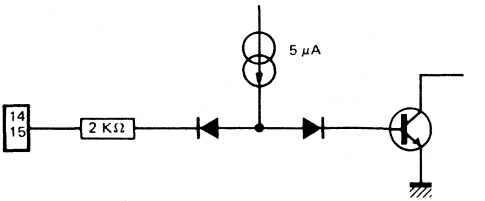
Loudspeaker impedance recommended value: 25 Ω.

Maximum gain available between earphone input and loudspeaker output: 32 - 6 = 26 dB.

Pin 11: Vref: internal reference

Output which provides an internally regulated reference voltage.
Vref = 1.1 V typical.
MAXIMUM AVAILABLE CURRENT: 5 μA.

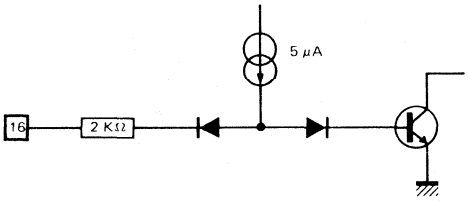
Pin 14-15: gain adjustment inputs



These pins are used to adjust the loudspeaker amplifier gain. Four steps of 6 dB/step are available (pin open circuit = high level).

PG0	PG1	
1	1	GMAX
1	0	GMAX - 6 dB
0	1	GMAX - 12 dB
0	0	GMAX - 18 dB

Pin 16: Loudspeaker muting



This pin is used to mute the loudspeaker. Pin open-circuit: high level = loudspeaker muted. Pin low level: loudspeaker enabled.

3 — SUPPLY CONSIDERATIONS

TEA 7531 supply:

As the I.C. has a Zener characteristic, it should be supplied by a current source.

Constant voltage supply:

The TEA 7531 can be supplied by an external constant voltage on condition:

- that the zener voltage is set at a level higher than the supply voltage,
- that the automatic gain control pin (pin 3) is tied to ground (otherwise the I.C. will always be in AGC mode).

Note:

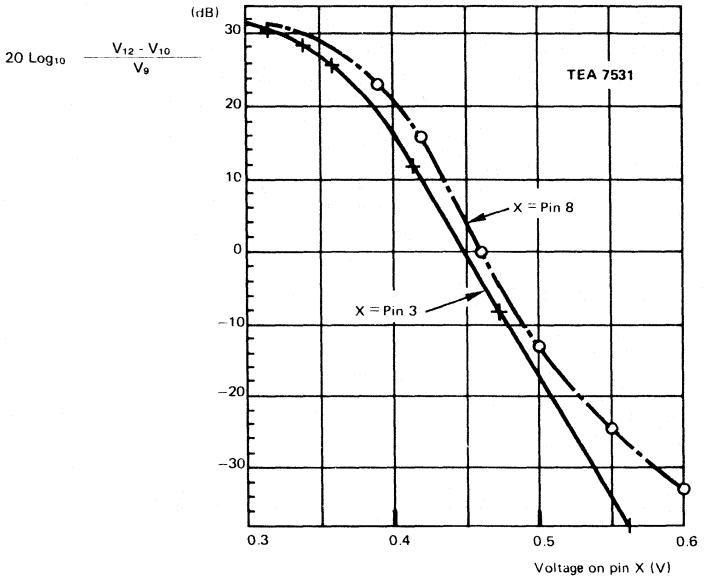
The maximum loudspeaker level is dependent on the supply voltage.

4 — CURVES

EFFICIENCY OF ANTILARSEN SYSTEM AND ANTIDISTORTION SYSTEM

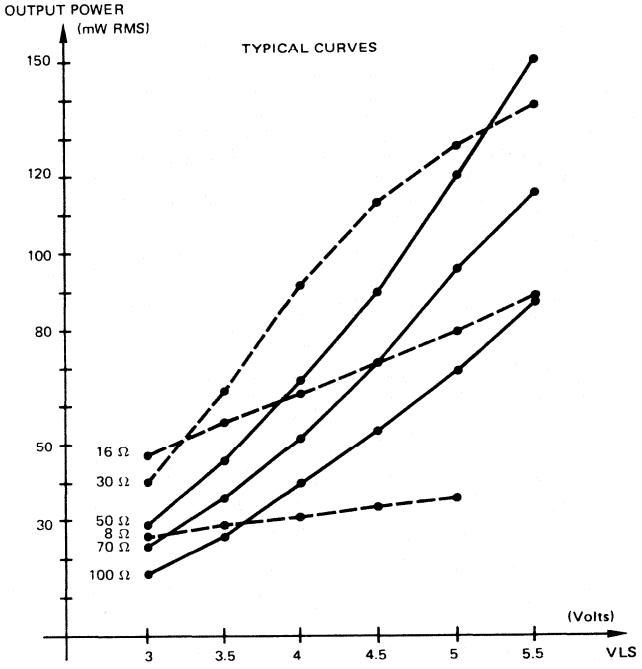
Loudspeaker gain versus voltage on pin 8, on pin 3

Typical curve

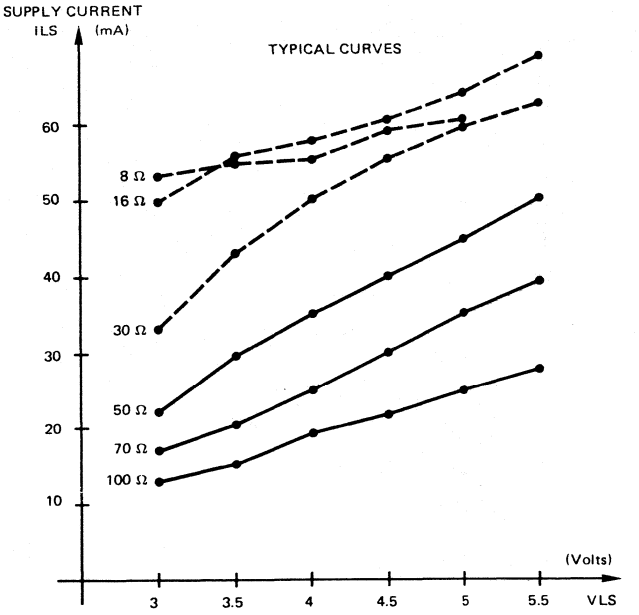


4.1 — Loudspeaker amplifier working in "H" mode

TEA 7531



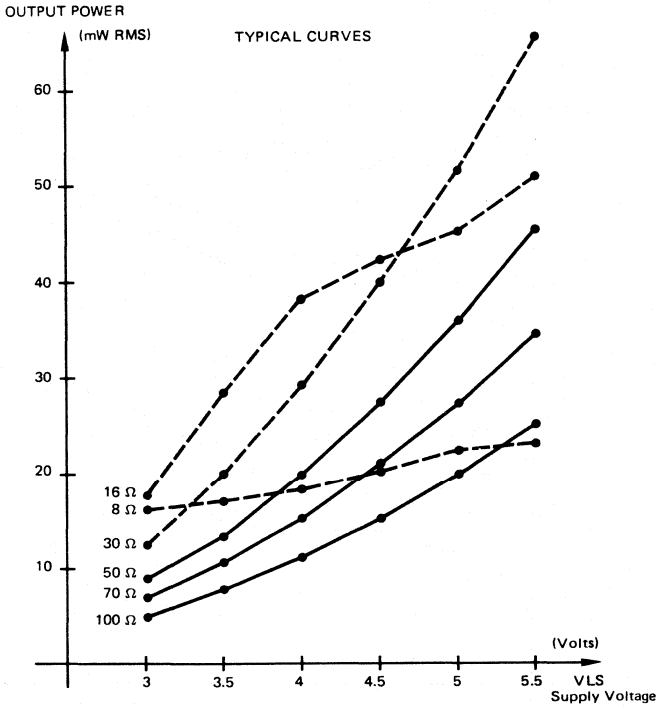
* Measurements realized with a distortion of 2%, at a frequency of 1000 Hz
* Loads: resistors
* Zener inhibited - Voltage supply
* Pins 3-8 connected to ground



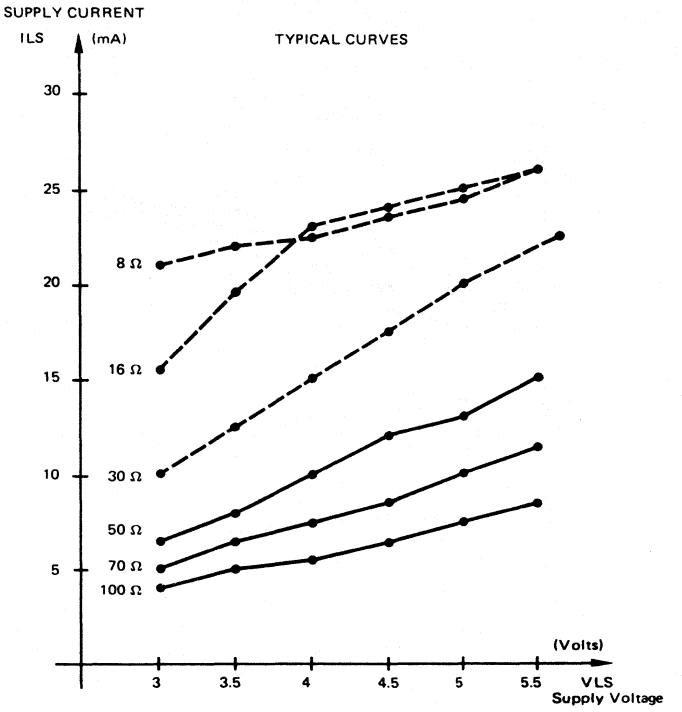
* Same measurement conditions that for output power

4.2 — Loudspeaker amplifier working in "B" mode

TEA 7531



* Measurements realized with a distortion of 2%, at a frequency of 1000 Hz
* Loads: resistors
* Zener inhibited - Voltage supply
* Pins 3-8 connected to ground

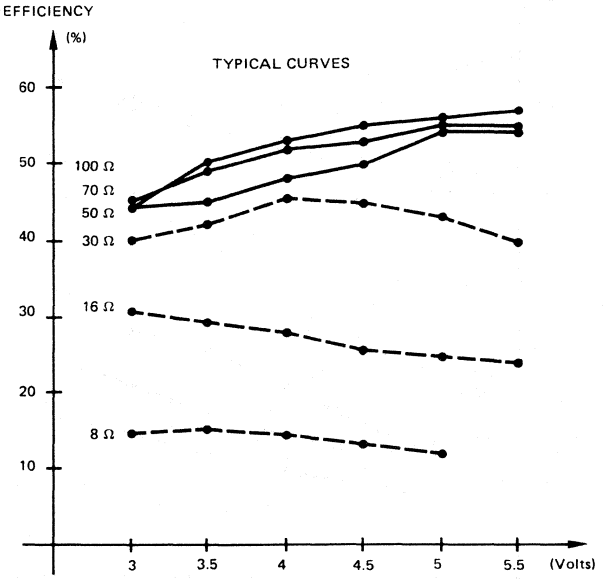


* Same measurement conditions that for output power

4.3 — Loudspeaker amplifier efficiency

"H" MODE

TEA 7531

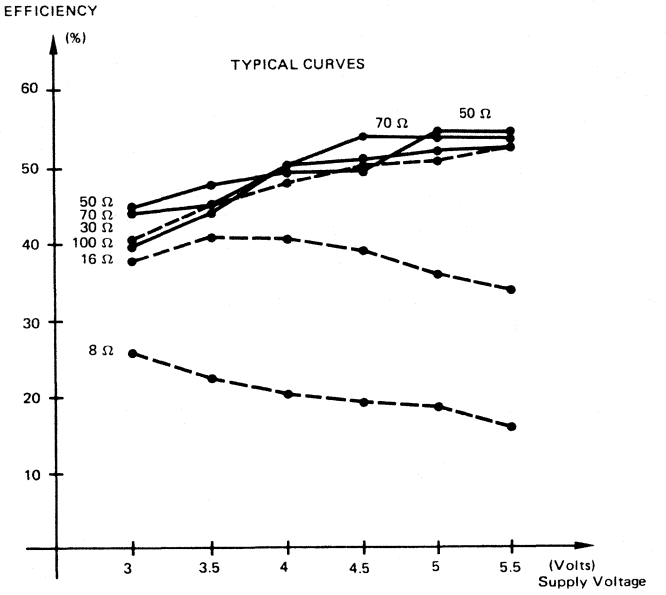


* Same measurement condition that for output power

$$\text{* Efficiency} = \frac{\text{Output power}}{\text{Supply power}} = \frac{\frac{U^2 \text{ (pins 12-10) RMS}}{\text{R out}}}{\text{VLS x ILS}}$$

"B" MODE

TEA 7531



* Same measurement condition that for output power

$$* \text{ Efficiency} = \frac{\text{Output power}}{\text{Supply power}} = \frac{\frac{U^2 \text{ (pins 10 to ground) RMS}}{\text{R out}}}{\text{VLS x ILS}}$$

5 — TEA 7531 TYPICAL APPLICATION

Resistors:

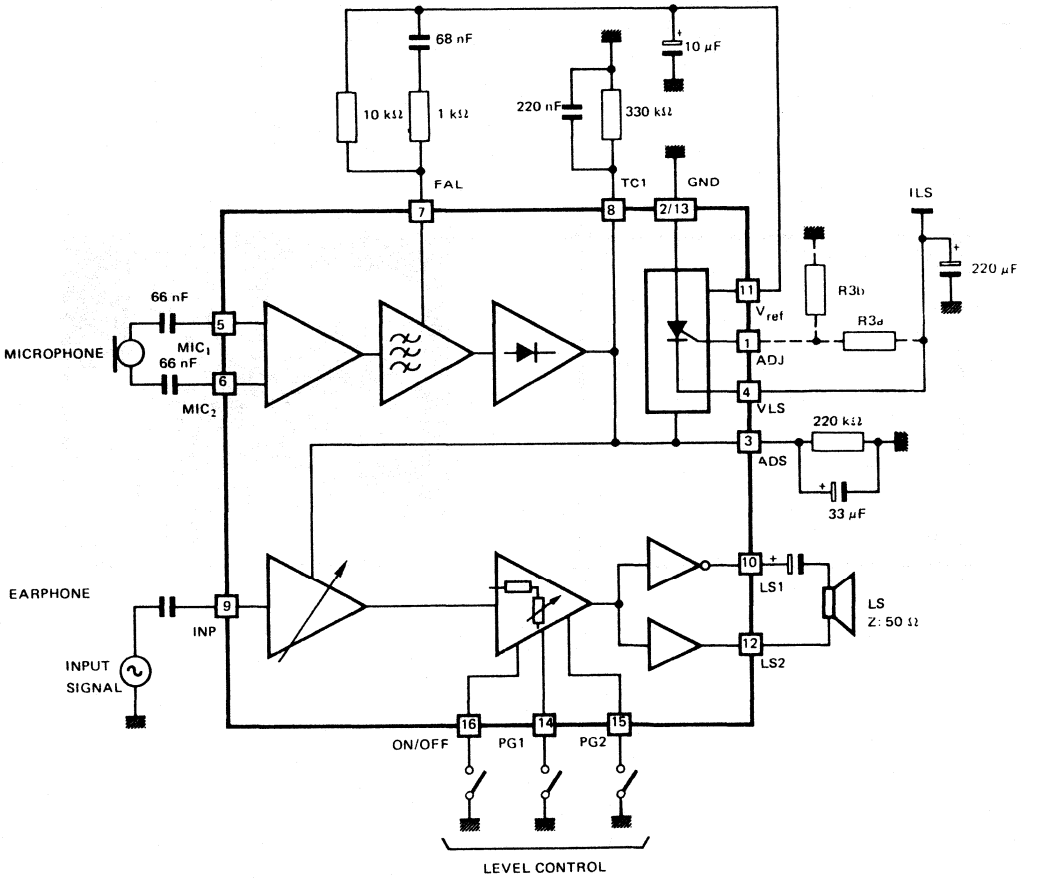
R3:
R4: 470 kΩ
R5: 1 kΩ
R6: 10 kΩ
R7: 330 kΩ

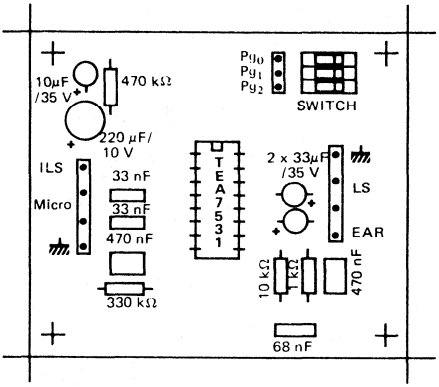
Capacitors:

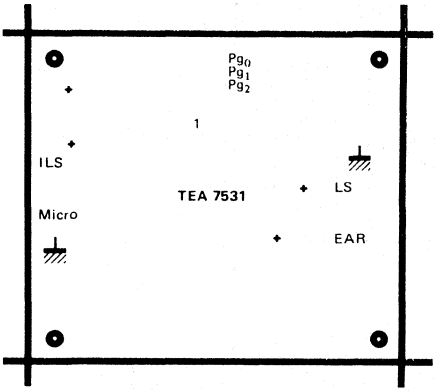
C5 = 68 nF
C7 = 470 nF
C9 = 33 nF
C11 = 33 µF/10 V

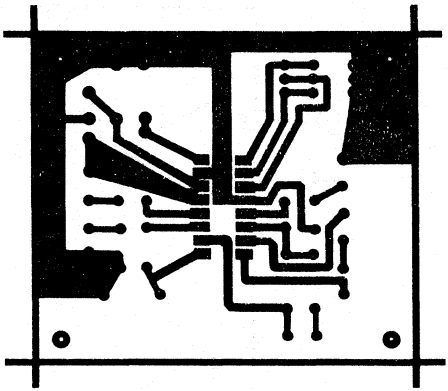
C2 : 220 µF/10 V
C4 : 10 µF/10 V
C6 : 220 nF
C10: 33 nF
C12: 33 µF/10 V

TEA 7531 APPLICATION BOARD



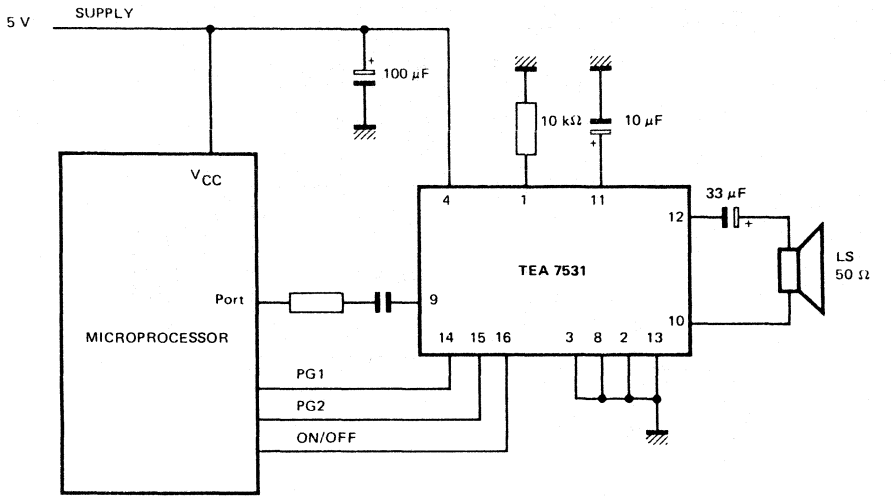

10µF
/35 V
470 kΩ
220 µF/
10 V
ILS
Micro
33 nF
33 nF
470 nF
330 kΩ
Pµ0
Pµ1
Pµ2
SWITCH
TEA7531
2 x 33µF
/35 V
LS
EAR
10 kΩ
470 nF
68 nF


Pg0
Pg1
Pg2
1
ILS
TEA 7531
LS
Micro
EAR



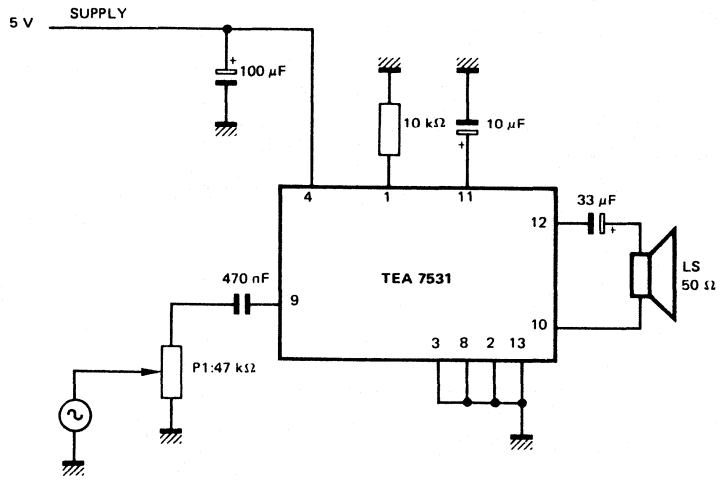
6 — VARIOUS APPLICATIONS

6.1 — Sound Generator by microprocessor



- Single 5 V voltage supply.
  The externally adjustable internal zener has been set at higher voltage by means of the 10 kΩ resistor on pin 1.
- Loudspeaker output level may be incrementally or decrementally adjustable in steps of 6 dB (4 steps + ON/OFF) by means of the microprocessor.

6.2 — Sound monitor for a LF Generator

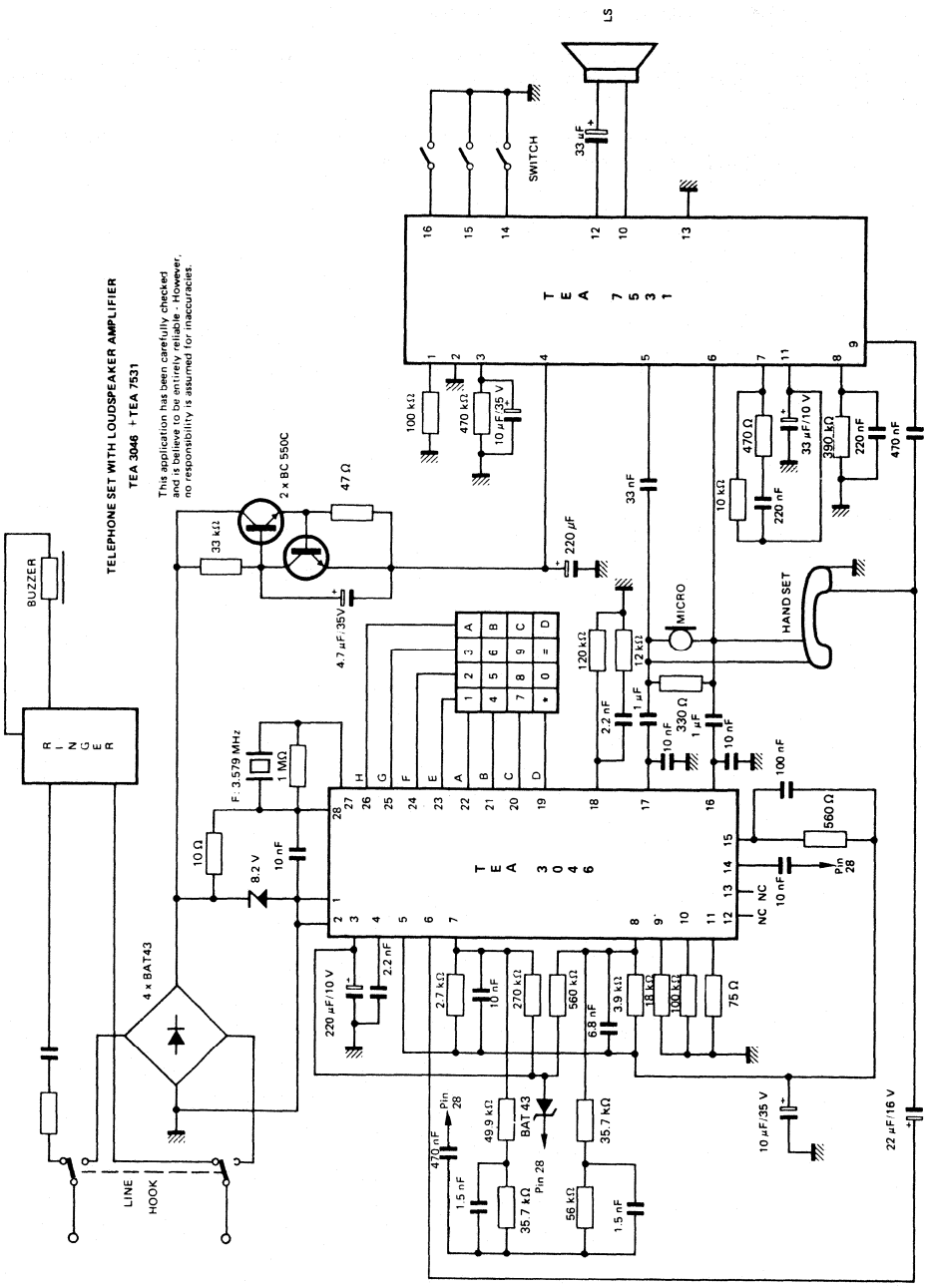


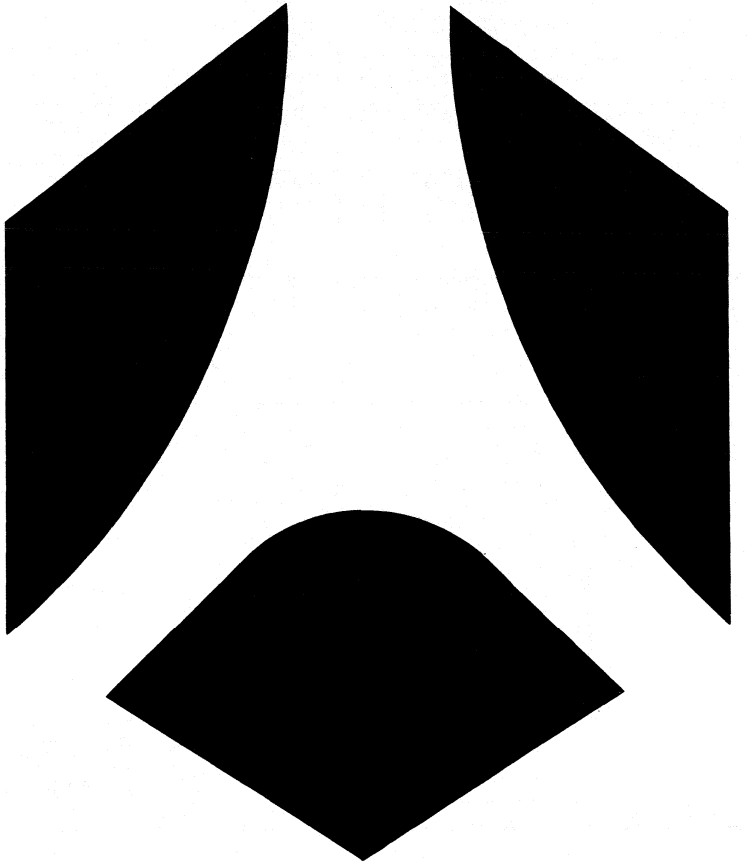
- Single 5 V voltage supply. The externally adjustable internal zener has been set at higher voltage by means of the 10 kΩ resistor on pin 1.
- Loudspeaker level may be continuously adjusted by the external potentiometer P1.
- Maximum power level available into a 50 Ω mode = 100 mW_{RMS} typically (with a 2% distortion).

6.3 — Telephone set with loudspeaker amplifier

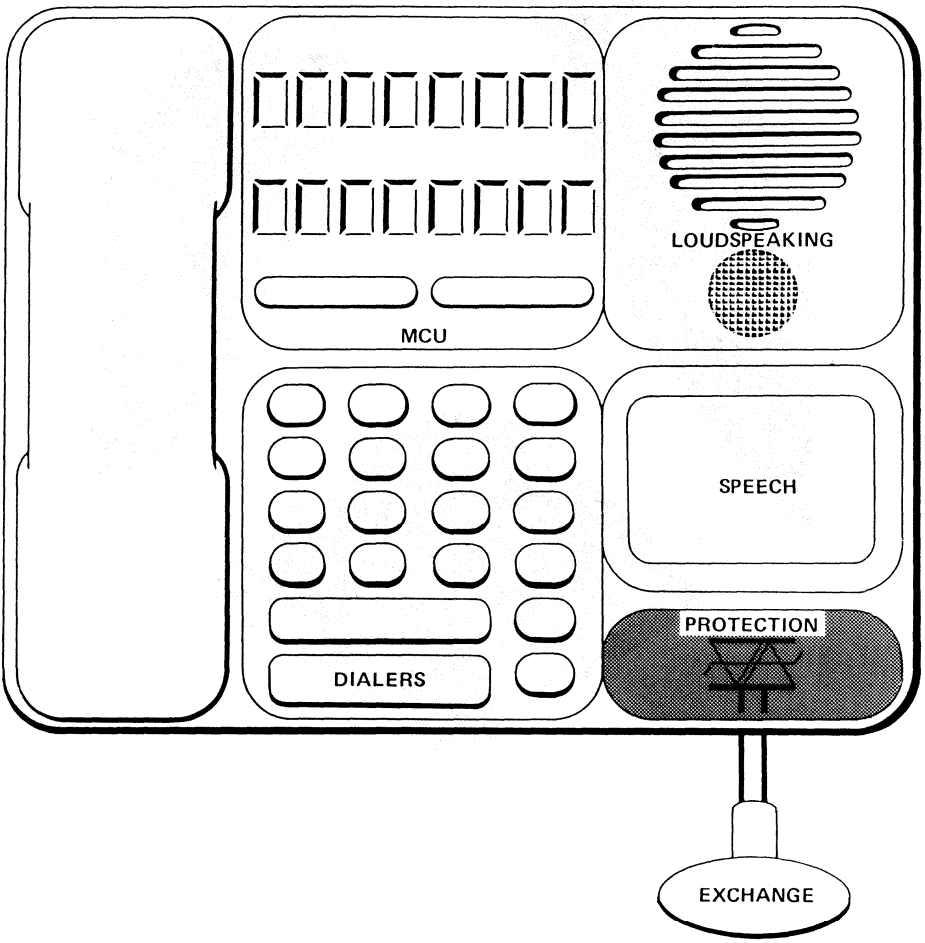
The TEA 7531 has been associated with an I.C. which provides transmission and DTMF generation, the TEA 3046. Together they constitue a low cost and a high performance telephone set.

The TEA 7531 is supplied from the line, through a current mirror, which presents a high impedance in AC loads, in order to minimize the effect on the speech.


TELEPHONE SET WITH LOUDSPEAKER AMPLIFIER
TEA 3046 + TEA 7531
This application has been carefully checked and is believe to be entirely reliable. However, no responsibility is assumed for inaccuracies.
BUZZER
RINGER
LINE
HOOK
4 x BAT43
2 x BC 550C
47 Ω
33 kΩ
4.7 µF/35V
F: 3.579 MHz
1 MΩ
10 Ω
10 nF
8.2 V
220 µF/10 V
2.2 nF
2.7 kΩ
10 nF
270 kΩ
560 kΩ
6.8 nF
3.9 kΩ
18 kΩ
100 kΩ
75 Ω
470 nF
49.9 kΩ
BAT 43
35.7 kΩ
1.5 nF
56 kΩ
Pin 28
TEA 3046
TEA 7531
100 kΩ
470 kΩ
10 µF/35 V
220 µF
33 nF
120 kΩ
12 kΩ
2.2 nF
1 µF
330 Ω
10 nF
MICRO
HAND SET
SWITCH
LS
33 µF
470 Ω
33 µF/10 V
390 kΩ
220 nF
10 kΩ
470 nF
100 nF
560 Ω
NC
10 µF/35 V
22 µF/16 V



Protection discrete components


LOUDSPEAKING
MCU
SPEECH
PROTECTION
DIALERS
EXCHANGE

HOW TO CHOOSE A TRANSIL

J.M. Peter
Laboratoires d'application

September 1986

The Transil is an avalanche diode specially designed to clamp over voltages and dissipate high transient power. A Transil has to be selected in two steps :

A). Check that the circuit operating conditions do not exceed the specified limit of the component.

- For non-repetitive «shock» operation,
- For repetitive load operation,
- For continuous operation.

B). Check that the maximum value of the clamped voltage under the most adverse conditions corresponds to the V_C specification of the circuit, i.e. there is no danger for the protected circuits.

REVIEWING THE CHARACTERISTICS OF TRANSIL

1). THE PEAK REVERSE VOLTAGE V_{RM} is the voltage which the Transil can withstand in continuous operation.

2). THE BREAKDOWN VOLTAGE OR KNEE VOLTAGE V_{BR} is the voltage value above which the current in the Transil increases very fast for a slight increase in voltage. The breakdown voltage V_{BR} is specified at 25°C and its temperature coefficient is positive. The V_{BR} tolerance is normally ± 5 %, however it is important to note that Transil technology enables obtaining much lower tolerance in mass production than the other technologies.

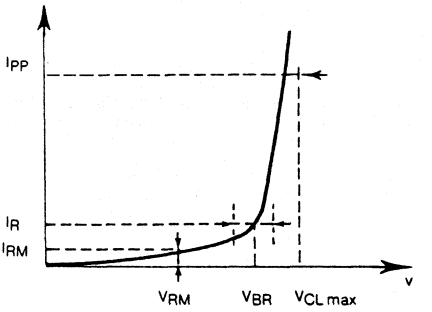


***Figure 1** · Main characteristics of a Transil.*

3). THE CLAMPING VOLTAGE V_{CL} as specified in the data-sheets in the maximum value for the «standard» pulse with a peak value of I_{PP}, specified for any type of TRANSIL. (Fig 2).

If the Transil is subjected to a different pulse, the data given in the data-sheets enables calculating the maximum value V_{CL} reached which depends, first of all, on the current level, and then, to a lesser degree, on the duration of the pulse, and finally (by means of the temperature coefficient) on the initial temperature.

The campling factor is represented by V_{CL}/V_{BR}. This ratio between the maximum value of overvoltage for a given current and the maximum voltage which the diode can withstand in continuous operation characterizes the quality of the protection.

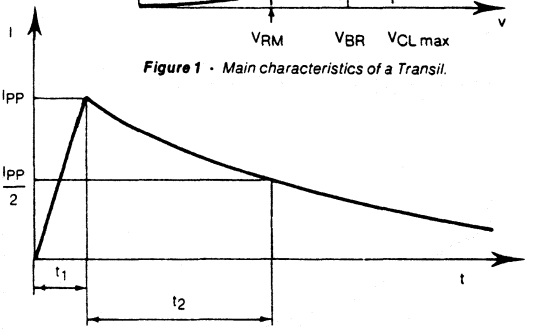


***Figure 2** · Standard exponential pulse. This type of pulse corresponds to most of the standards used for the protection of electronic equipment.*

4). TRANSIL'S POWER DISSIPATION (non-repetitive operation).
A protecting device whose operation is adiabatic can dissipate the very same energy.

	t_1 µs	t_2 µs
WAVE «8/20 µs»	8	20
WAVE «10/1000 µs»	10	1000

$$W = \int_0^{\tau} V_{CL}\, idt$$

Whatever the duration τ of the surge ; a component of this type is said to be «iso-energetic».

The first protection devices, designed to meet electrotechnical standards, often had an iso-energetic behaviour, and they were mostly used for short over voltages (of the 1/50 µs wave type) encountered on high voltage lines. The research carried out by the CNET (French Telecommunications Agency), confirmed by research abroad, tends to show that low-power electronic equipment is subjected to over voltages of a much longer duration, better represented by 10/100 µs exponential wave is Fig 2.

Transil are meant to protect electronic equipment and hence have been designed not to be iso-energetic but to perform well for over voltages up to durations of 1 ms.

The performance of Transil has thus been determined with reference to the standard exponential wave 10/1000 μs.

$P_P = V_{BR} . I_{PP}$

The maximum possibilities correspond to non-repetitve operation. If the pulse has a different duration, a curve similar to that in Fig. 3, provided in the data-sheets, enables determining the specifications of the Transil.

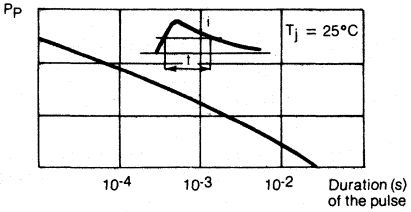


Figure 3 *- Maximum power for an exponential pulse of duration t.*

If the initial temperature exceeds 25°C, the power (PP) should be reduced in accordance with the curve of Fig. 4 which is the same for all the Transil.

If the current surge through the Transil is not exponential, the indications of the table of Fig. 5 enable calculating the equivalent exponential pulse.

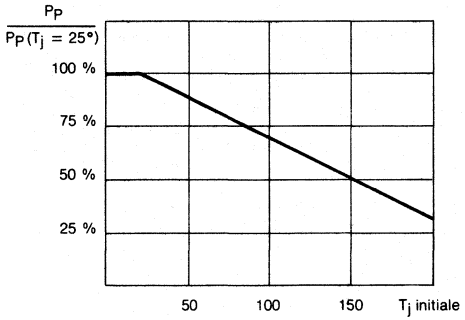


Figure 4 *- Variation of peak power as a function of the initial temperature. This curve should only be used for pulse durations of less than 0.01 s.*

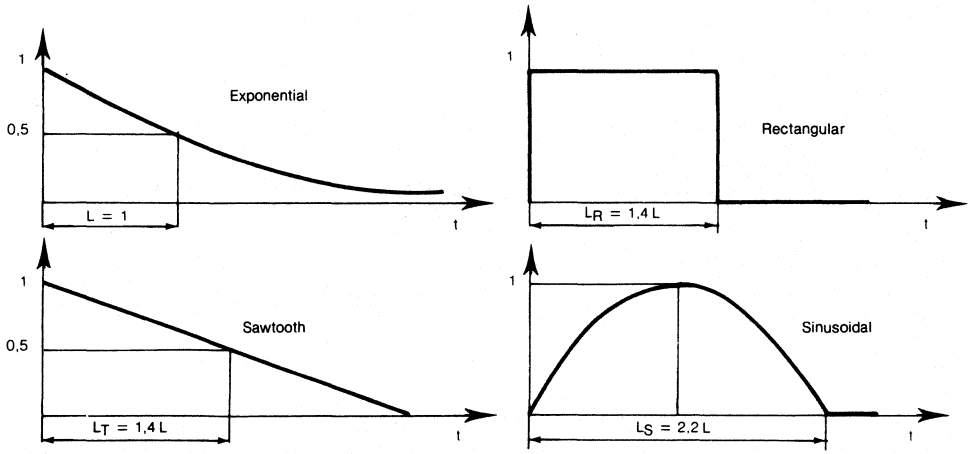


Figure 5 *- Above four pulses of same peak value lead to an identical dissipated power in a Transil.*
For example : the rectangular pulse which gives the same dissipation than the exponential pulse for a same peak value is 1.4 times longer.

5). POSSIBILITY OF POWER DISSIPATION BY TRANSIL IN MEAN POWER

In repetitive operation, the specification to be considered is mean power P_{AV}.

$$P_{AV} = f.W$$

(f : frequency, W : energy dissipated at each pulse)

The junction temperature calculated from this power should in no case exceed 175°C (note that this is the mean temperature).

This temperature is calculated from the thermal resistance, exactly like for a diode. The experience of our application laboratories leads to recommending much lower mean junction temperatures — of about 100 to 110°C — for repetitive industrial operation.

$T_j = T_{amb} + R_{th} . P_{AV}$

$R_{th} = R_{th\,(ja)}$ for axial lead Transil.

$R_{th} = R_{th}$ (Transil) + R_{th} (heatsink) for Transil in DO220, DO4, DO5 cases.

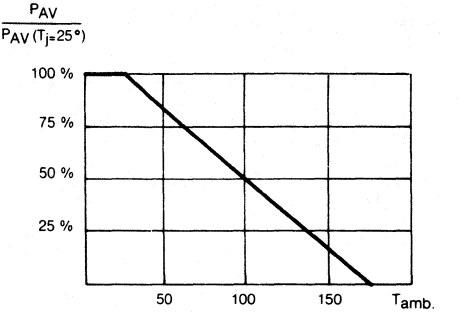


***Figure 6** · Maximum average power as a function of ambient temperature.*

6). SPEED

The first purpose of a Transil is to clamp over voltages produced by current surges.

A conventional lightning arrester system only responds with a certain delay which can reach 2 µs. A metal oxide varistor does not respond immediately either (delay of about 25 ns).

If a current with a very low rise time flows through these components, an over voltage could appear before the device reacts.

In the case of Transil, the avalanche phenomenon of a silicon diode is extremely fast (theoretical value about one picosecond).

In laboratory tests we have never succeeded in producing over-voltages across Transil, even by using special device producing very steep current gradients (dischargers, mercury relays).

In conclusion it can be said that Transil respond instantaneously in clamping, on condition that di/dt over-voltages are not introduced by connection inductances.

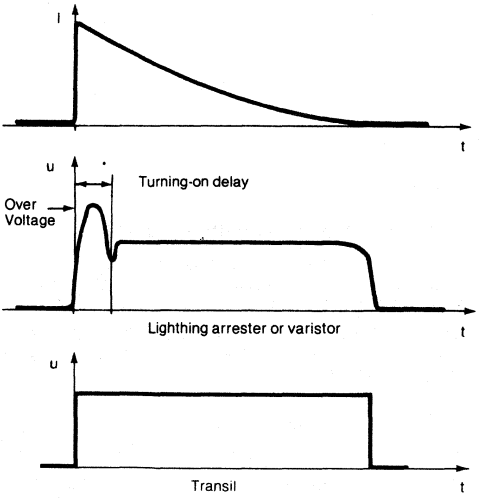


***Figure 7** · Voltage response of a classical component used for protection and of a Transil.*

The low capacitance Transil and the bidirectional models have clamping times of about 5 ns. These times remain negligible for practically all applications.

7). SPEED IN «DIODE» OPERATION

A Transil operating as a rectifier is not a fast recovery diode (it has a high recovered charge). As a result, Transil cannot be used for the rectifier function instead of fast recovery diodes.

On the other hand, a Transil operating as a diode has very low forward recovery time (and a very low forward peak voltage V_{FP}). This property can be used for particular applications since no other existing diode has a lower turn-on time for a given V_{BR} (or V_{RM}) voltage.

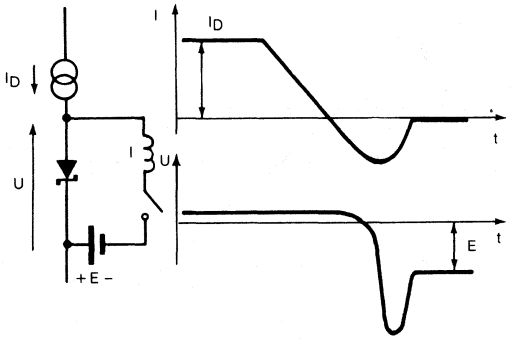


Figure 8 - *Behaviour of a Transil operating as a diode at turn-off.*

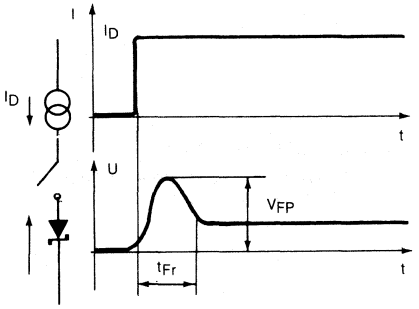


Figure 9 - *Behaviour of a Transil operating as a diode at turn-on.*

8). CALCULATION OF THE SURGE VOLTAGE

This is a very important step. A Transil is designed for protection, and the user should know the peak voltage after clamping, V_{CL}, in the presence of a current pulse.

When the Transil operates in the avalanche mode, the clamping voltage exceeds the V_{BR} value by a quantity which depends on :

- the peak current,
- the duration of the pulse,
- the initial temperature of the «simplified» Transil.

The data-sheets specify the maximum value of V_{CL} for each type of Transil associated with the maximum current I_{PP} for a standard exponential wave. The curves in the detailed data-sheets (a simplified example is given in Fig. 10) give the characteristics for other durations (10 µs and 10 ms) and enable calculating (by interpolation) the maximum clamping voltage if the current surge has a shape other than that of the standard pulse.

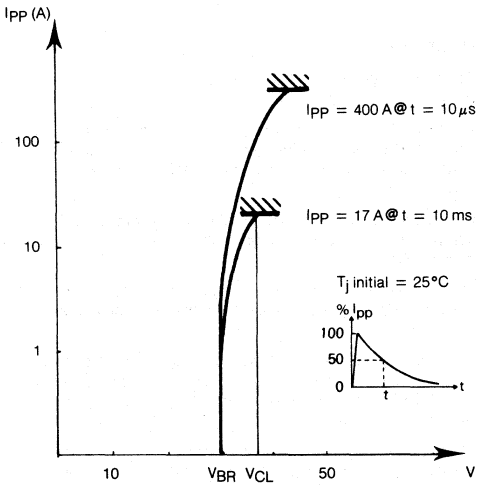


Figure 10 - *Characteristics given in the simplified data-sheets for calculating the clamping voltage V_{CL}.*

Figure 11 shows the real behaviour of the Transil. The voltage peak is not in phase with the current peak because of heating. The curves $I_{PP} = f(V_{CL})$ thus represent, in reality, the variation of the maximum voltage after clamping.

All the values are given for an initial temperature of 25°C before the surge and should be corrected as a function of the temperature coefficient as provided in the data-sheets.

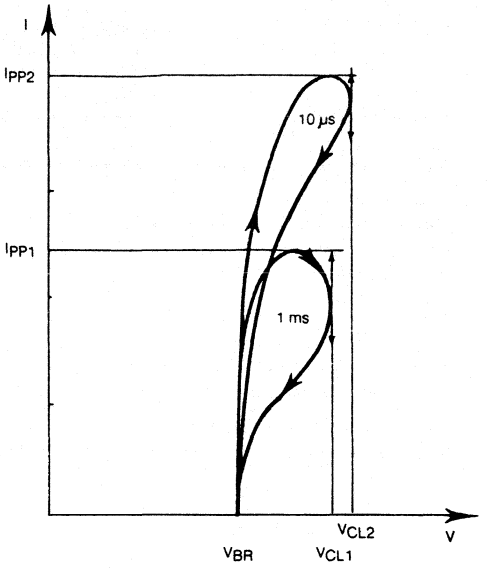


***Figure 11** - Behaviour of a Transil subjected to two pulses of different durations.*

9). CALCULATION EXAMPLE

9.1 Non-repetitive surges

A source (V_1) with a rated voltage of a 24 V supplies equipment E which is to be protected against over voltages. This source is subjected to random non-repetitive exponential over voltages with amplitudes of 200 V and a duration of 1 ms at 50 % (standard wave). The equivalent internal impedance Φ of the source with respect to 1 ms exponential waves is 13 Ω .

The maximum ambient temperature is 80°C. In no case should equipment E be subjected to a voltage higher than 50 V.

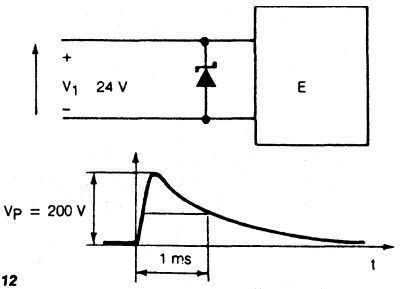


Figure 12

9.1-1 Selection of the protection voltage

In the absence of specific information, we assume that voltage V_1 varies by ± 20 %, ie between 20 V and 29 V.

The protection voltage V_{RM} of the Transil should then be equal or superior to 29 V.

9.1-2 Predetermination of the peak power P_P

The equipment E cannot withstand a voltage above 50 V $\rightarrow V_{CL} \leqslant$ 50 V.

We assume there is a Transil answering to this criterion, what allows to make a first determination of the power of the Transil we will use.

$$P_P = V_{CL} \times I_P \quad \text{where } I_P = \frac{V_P - V_{CL}}{\Phi} \qquad I_P = \frac{+200 - 50}{13} = 11{,}5\text{A and } P_p = 50 \times 11{,}5 = 577\text{W}$$

This power corresponds to an operating temperature of 80°C. The data sheets indicate power at 25°C so we have to correct the power according to the curves of admissible power versus initial temperature.

So we obtain :

$$P_{P\,(25°C)} = \frac{P_{P\,(80°C)}}{0{,}8} \qquad P_{P\,(25°C)} = \frac{577}{0{,}8} = 721\text{ W}$$

9.1-3 Selection of the Transil

We can now establish a first specification of the Transil to use.

$V_{RM} \geq 29V$

$V_{CL} \leq 50V$ for $I_p = 11,5\ A$

$P_{P\,(25°C)} = 721\ W/1ms$

The type corresponding to these characteristics is the 1.5 KE 36

$V_{RM} = 29,1V$

$V_{BR\,nom} = 36\ V$; min 32,4 V ; max 39,6 V

$V_{CL\,max} = 52\ V \quad I_{PP} = 29\ A$

$P_P = 1500\ W/1ms$

$\alpha_T = 9,9 \times 10^{-3}$

9-1.4 Determination of the clamping voltage V_{CL}.

To determine the voltage V_{CL} at 11,5 A, we can use the I_{PP} / V_{CL} curves included in the 1.5 KE data sheets.

V_{CL} at $I_P \simeq V_{BR\,max} + R_D \cdot I_P$

R_D can be determined from the indications in the data sheets.

$$R_D \leq \frac{V_{CL} - V_{BR}}{I_{PP}}$$

$$V_{CL} \text{ at } 11,5\ A \simeq 39,6 + \frac{52 - 36}{29} \times 11,5 = 45,9\ V$$

9-1.5 Temperature correction

The voltage at 80°C is :

$V_{CL\,(80°C)} = V_{CL\,(25°C)} \cdot [1 + \alpha_T (T_j - 25°)]$

$V_{CL\,(80°C)} = 45,5\ [1 + 9,9\ 10^{-4} (80 - 25)]$

$\simeq 48\ V$

This value is below the 50 V limit. The Transil insures the protection.

9.2 Repetitive surge

We have to protect the transistor shown on Fig. 13 with a Transil whose clamping voltage, V_{CL}, is not exceeding 85 V.

Calculation method

To avoid a long calculation, we assume :

$V_{CL} \simeq V_{BR}$ **only true in the case of repetitive surges.**

The experience shows this hypothesis is confirmed in most of the cases with Transil, for we have to choose the Transil considering its thermal resistance first (it is not the same with zeners which have higher dynamical resistance).

9.2-1 P_{AV}

An approximate value can be obtained by supposing that all the energy contained in the inductance is absorbed by the Transil. This hypothesis is near the reality when the ratio

$\frac{V_{BR}}{V}$ is important

$$P_{AV} = \frac{1}{2} L I^2 f = \frac{1}{2} .0,35 \left(\frac{12 + 2,2}{45} \right)^2 \quad 50 = 0.9\ W$$

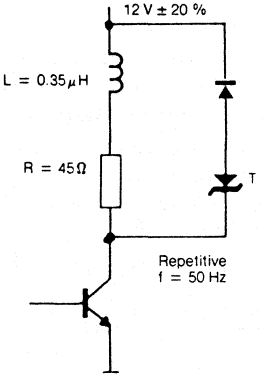


Figure 13

9.2-2 First choice

We choose the type BZW 04.61 $V_{BR\,max}$ = 82,5 V
R_{th} = 100°C/W

9.2-3 T_j calculation

This value is compatible with the Transil characteristics, but we consider that the safety coefficient is not sufficient.

9.2-4 Second choice

1.5 KE 75 $V_{BR\,max}$ = 82,5 V R_{th} = 75°C/W

9.2-5 T_j calculation

T_j = 50 + 68 = 118°C

9.2-6 Determination of V_{CL}

We see on the data sheets that for such a low current level $V_{CL} \simeq V_{BR}$

9.2-7 Temperature correction

$V_{CL}(118°C) = V_{CL}(25°C) \left[1 + \alpha_T (118 - 25)\right]$ = 90,5 volts

This value is too high.

9.2-8 Third choice

The Transil 1.5 KE 68 is suitable.

Remark : This example shows that to the component dispersion we have to add the variation due to the tempeature.

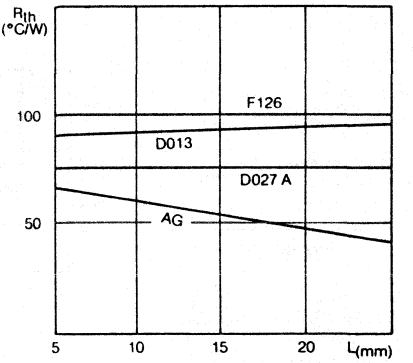


***Figure 14** · Mounted on a printed circuit.*

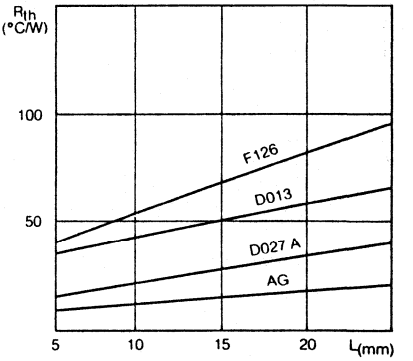
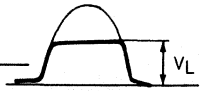


***Figure 15** · Mounted on an infinite heatsink thermal resistance j-a versus connections length.*

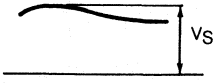
SELECTION OF A TRANSIL

For repetitive surges

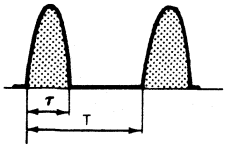
DATA



Clamping voltage

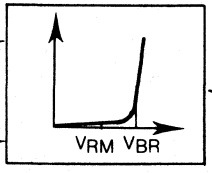


Working voltage



Current pulse

VL ou VS



SELECTION OF THE VOLTAGE

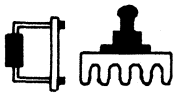
$V_{CL} \leqslant V_L$

$V_{RM} \geqslant V_S$

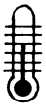
$$P_{AV} = \frac{1}{T}\int_0^{\tau} V_{CL}\, Idt$$

P_M

SELECTION OF THE TYPE



Determination of R_{th}



T_{amb}

Ambient temperature

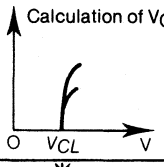
$T_j = T_{amb} + P_{AV} . R_{th}$

$T_j < T_{Lim}$?

YES | NO

Improve the cooding and/or a more powerful type

Remarks : In the case of repetitive surges, in order to simplificate the calculation we assume :
$V_{BR} \simeq V_{CL}$



Temperature correction

$V_{CLT_j} = V_{CL_{25}} (1 + \alpha_T (T-25))$

FINAL CHECK

$V_{CLT_j} < V_L$?

YES | NO

TRANSIL THE BEST CHOICE

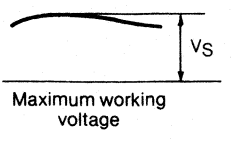
Utilize a more powerful Transil

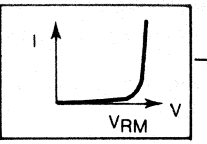
For particular cases, consult our Application Laboratory

SELECTION OF A TRANSIL

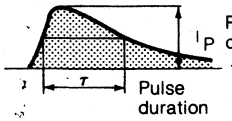
For a non-repetitive surge

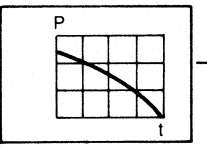
DATA



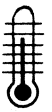


SELECTION OF V_{RM} $V_{RM} \geq V_S$

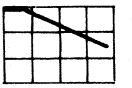




Determination of power P_P

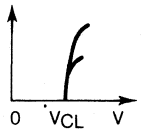


Temperature correction



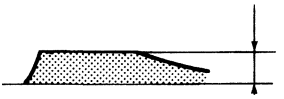
SELECTION OF THE TYPE

Calculation of V_{CL}



Temperature correction

$V_{CL_T} = V_{CL_{25}} (I + \alpha_T (T-25))$



FINAL CHECK

$V_{CL} < V_L$?

YES | NO

TRANSIL THE BEST CHOICE

Use a more powerful Transil

For particular cases, please consult our Application Laboratory

Remarks :

1. If the surge pulse is not exponential, calculate the equivalent exponential pulse.

2. To increase the power of the Transil it could be useful to connect two Transil of lower voltage in series (never in parallel).

APPLICATIONS OF TRANSIL

Reviewing, Transil are silicon components and hence utilize a technology close to that of diodes. They have been specially designed to protect professional and industrial equipment.

Transil are the only protection components which simultaneously have the following characteristics :

- High operating temperature (175°C maximum),
- Perfect stability of the characteristics in time, i.e. contrary to most other technologies, Transil do not age,
- Extremely short response time,
- Very narrow tolerances on the characteristics,
- Very low dynamic power impedance this leads to a very good clamping factor.

Transil have high power absorbing characteristics for over voltages with short durations, i.e. over voltages which are encountered mostly in electronic equipment.

Correctly cooled or mounted on a heatsink they can withstand either long duration overloads or non negligible mean powers in repetitive operation.

The purpose of this publication is to complete the previous information by showing some common applications.

UTILIZATION OF TRANSIL FOR RECTIFICATION

1). UTILIZATION OF TRANSIL AS RECTIFIER DIODES

Transil are diodes specially designed to dissipate considerable power in avalanche operation. In direct conduction they have the properties of very good conventional diodes (with the possibility of handling very high surge currents) and operate as well as rectifiers.

The characteristics given in the data-sheets (I_{FSM}, forward voltage drop characteristic) enable calculating their values for these functions.

Each time this is possible, it is more attractive to use Transil directly as rectifiers instead of protecting the rectifiers with Transil, since the number of components is reduced.

2). UTILIZATION OF TRANSIL FOR PROTECTION

2.1 With bridge rectifiers

Considering the most general case, the voltage surge could be due either to the power supply or to the load. A study of the operation of the bridge rectifier shows that it is sufficient to limit the voltage on the «dc» side to protect the bridge whatever the origin of the over voltage is. In all cases, a single Transil is sufficient to protect a single phase or a 3-phase bridge rectifier.

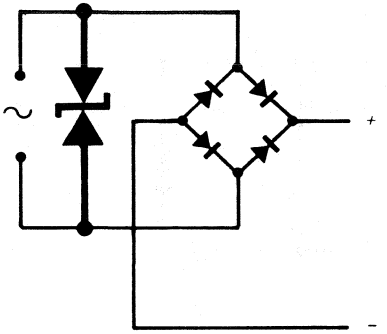


Figure 1 - *The diodes are not protected from over voltages due to the load.*

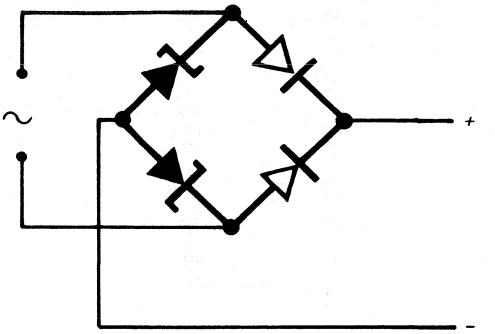
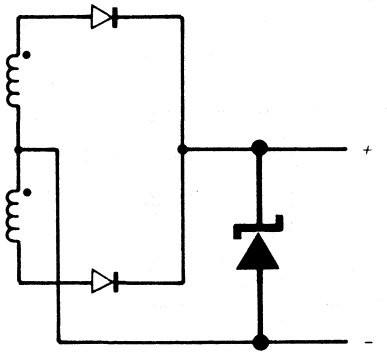


Figure 2 - *Mixed solution which insures protection of the load and of the rectifier diodes. The 2 Transil work as rectifiers.*



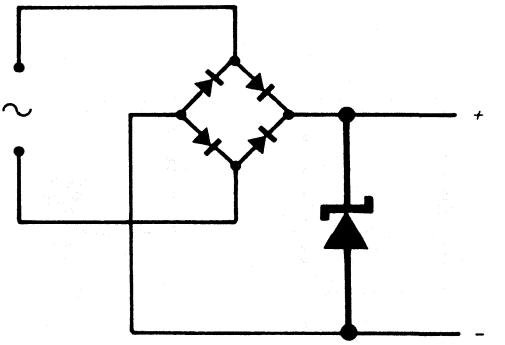


Figure 3 - *Optimal solution. A single Transil protects the rectifying components whatever the origin (power supply or load) of the over voltages.*

UTILIZATION OF TRANSIL WITH THYRISTORS AND TRIACS

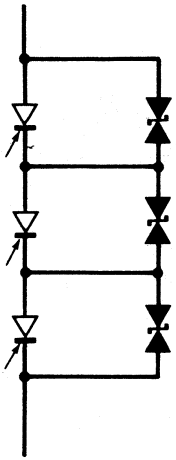


Figure 4 - *Protection for series circuits.*

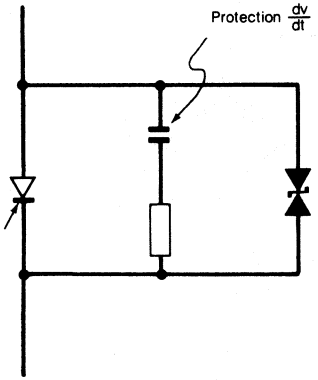


Figure 5 - *Protection from false triggerings.*

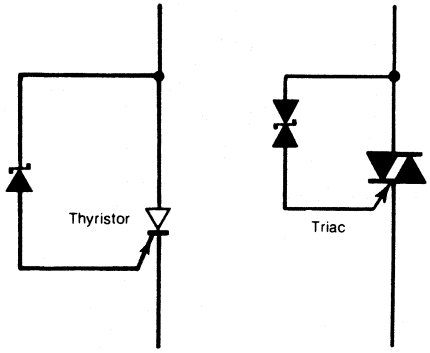


Figure 6 - *The Transil as shown in this circuit does not prevent the thyristor from turning on by gate triggering, however it does prevent the thyristor from being triggered by over voltages. (See technical information note 83-15 «Protégez vos triacs»).*

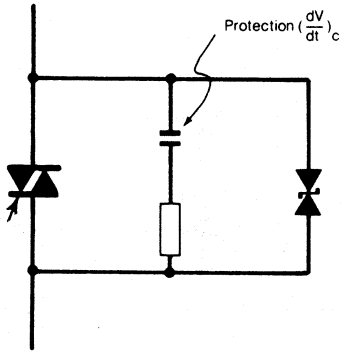


Figure 7 - *Protection of triacs.*
a) from false triggering,
b) from over voltages due to an incorrect damping of the RC network.

TRANSIL FOR PROTECTING MICROELECTRONIC CIRCUITS

DECENTRALIZED PROTECTION

Protection from accidental surges (consequences of lightning, incorrect actuation on a mains network, short circuit or breaking of a cable etc.) cannot generally be carried out in a single place, for example a high-power protection device connected directly accross the power supply input. In reality, the surges are transmitted to the electronic circuits by various paths : unwanted capacitance, inductive coupling, etc. insufficiently known by the designer of the circuit. Experience shows that for adequate protection it is necessary to decentralize the protection, i.e. install the Transil at the exact point which needs to be protected.

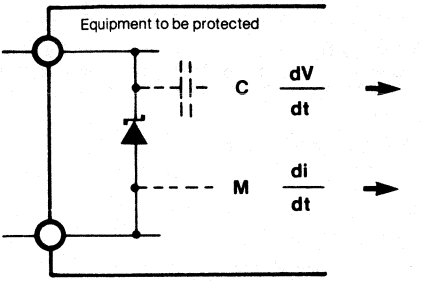


Figure 8 · *A local protection on the power supply is insufficient.*

DECENTRALIZED PROTECTION

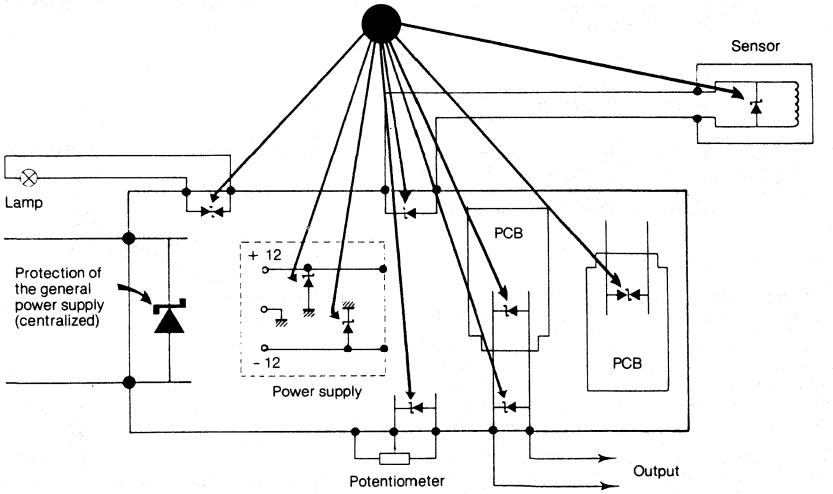


Figure 9 · *Decentralized protection is carried out locally at each spot where the circuit can «communicate» with the exterior.*

PROTECTION FROM TRANSIENTS GENERATED BY TRANSFORMERS

When a transformer is off-load the magnetizing current flowing through it is equal to :

$$i_O = \frac{V_1}{L_1 \omega} \sin\left(\omega t - \frac{\pi}{2}\right)$$

Where L_1 is the inductance throught to winding n_1.

If the switch is turned off (at the most unfavorable moment $\omega t = \pi / 2$), the Transil placed as a protection for the secondary, has to dissipate a power of.

$$W = \frac{1}{2} L (i_O \sqrt{2})^2 = L i_O^2$$

It corresponds to a peak power of :

$$P_P = i_O \sqrt{2}. V_{CL}$$

and this current will decrease as :

$$\frac{di}{dt} = \frac{V_{CL}}{L_2} \simeq \frac{V_{BR}}{L_2}$$

If the magnetizing current (off-load current) is unknown, it can be evaluated according to the following table :

Apparent power (KVA) of the 50 Hz transformer	0,1	1	5
Magnetizing current/nominal current	10%	7%	4%

Knowledge of the magnetizing current enables determining L_1 and the power to be dissipated. The selection of V_{BR} will fix the duration of the pulse.

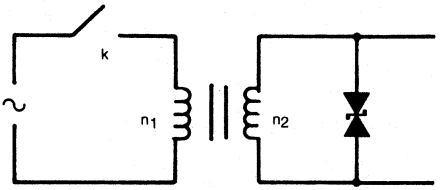


Figure 10

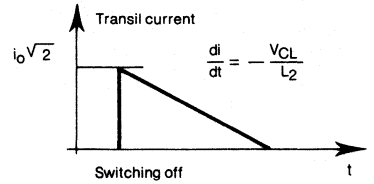


Figure 11 · Decrease of the current in the Transil of Fig. 10.

SHORT-CIRCUITS

When a short-circuit takes place, the current grows rapidly and the fuse blows, i.e. breaks the circuit only when the value of I_{CC} is sufficiently high (generally the value of I_{CC} is very high compared with the nominal current).

Two phenomena should be considered :

a). «Magnetic» disturbances
Unwanted magnetically induced voltages, follow the formula M. dI_{CC}/dt. Where M is the coupling coefficient. Engineers know how to protect equipment from electrostatic disturbances but as yet cannot offer efficient protection from disturbances caused by magnetic fields. Transil placed at sensitive spots help protect electronic circuits.

b). Electric disturbance caused by arcing of the fuse
Transil placed across fuses (or if not possible, at the input of the equipment) absorb part of these over voltages.

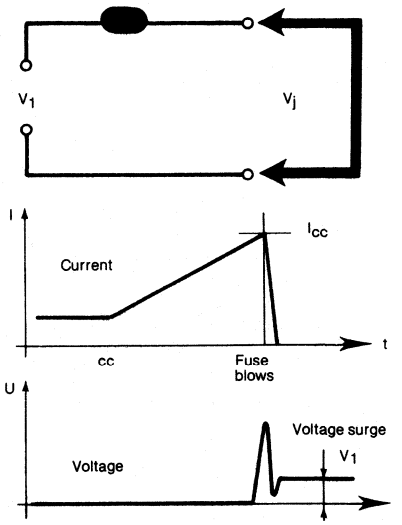


Figure 12 · Current and voltage across a fuse after a short-circuit.

RELAYS AND CONTACTS

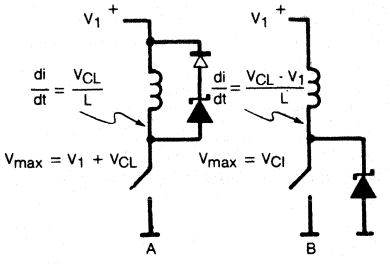
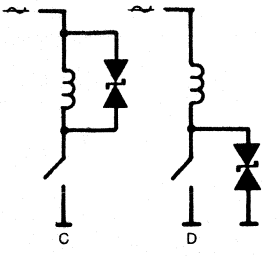


Figure 13 *- In cases whole the contacts are to be protected, configurations A and C enable higher operating safety.*



In the case of a relay, the Transil, while limiting the voltage surge enables cutting off the current in the coil faster than if there was only one free-wheeling diode.

IMPROVEMENT OF A CLAMPING CIRCUITS

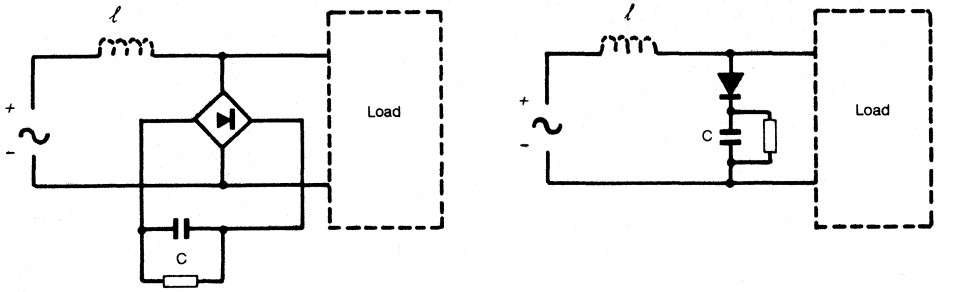
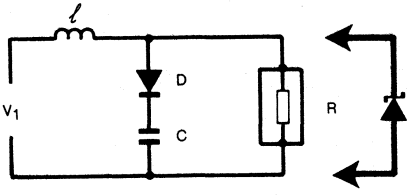


Figure 14 *- Clamping circuit with capacitor. ℓ represents the unwanted inductance of the power supply network.*



The circuits shown in Fig. 4 are commonly used in power electronics. Capacitor C can absorb considerable power.

Unfortunately the circuit whose equivalent diagram is represented in Fig 15 has a great disadvantage. The unwanted inductance of a power supply network can never be neglected and it often depends on the installation conditions. If the «load», equipment such as a converter, motor, etc., is itself not loaded the system may not be damped, and the off-load equipment could be damaged by an over voltages. **By inserting a Transil the equipment is guaranteed protection under all conditions encountered in practice.**

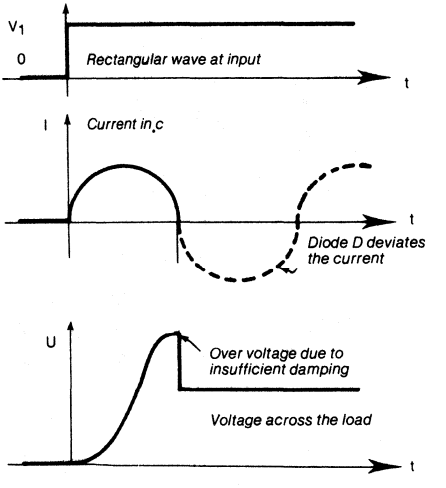


Figure 15 *- Equivalent diagram of the clamping circuit and waveform.*

UTILIZATION OF TRANSIL IN TRANSISTORIZED CONVERTERS

Because of their mode of operation, transistorized converters sometimes produce repetitive over voltages which should be limited of absorbed by passive components. A Transil is perfectly suited for this function.

Over voltages are mainly produced by unwanted inductances.

A chopper works very high curents. At the moment transitor T is turned off, the current is deverted by diode D, but an over voltages appears across the transitor, produced by thge unwanted inductance of the circuit.

The utilization of a Transil across the transitor limits the over voltages and protects it ; overstressing of the transitor can thus be avoided.

In power equipment Transil can be used to discharge circuit generated inductances there by helping switching.

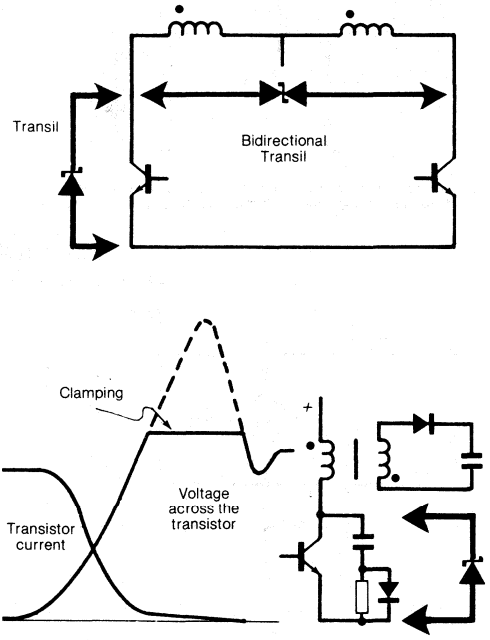


Figure 16 *- Utilization of Transil to limit the over voltages produced by the leakage inductances of transformers.*

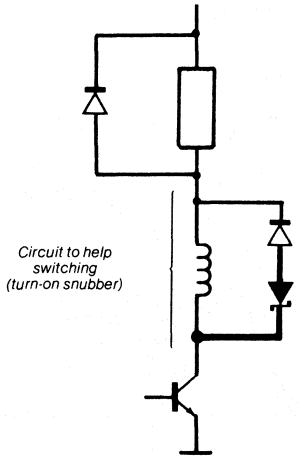


Figure 18 *- Utilization of a Transil with a circuit to help switching.*

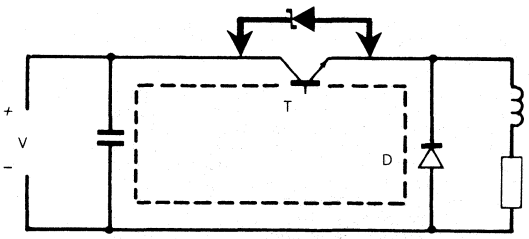


Figure 17 *- The Transil clamps the over voltages ldi/dt due to the unwanted inductance 1 of the dotted circuit.*

PROTECTION OF FAST RECTIFIER DIODES

Transil are very quick in avalanche operation, but they are not fast recovery diodes. When a fast rectifier is to be protected, two Transil in series should be used in order to be sure that all the forward current passes effectively through the fast rectifier diode.

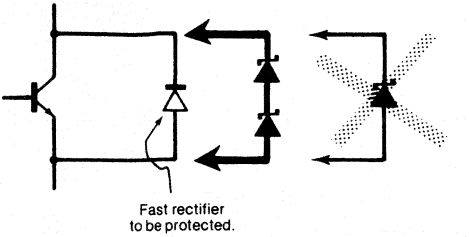


Figure 19 *- Protection of a fast rectifier by Transil.*

EXTENSION OF THE APPLICATION AREA

1). HIGH VOLTAGE

Transil can be connected in series without difficulty. It is unnecesary to balance them by RC networks however it is advisable to connect in series only Transil of the same type in order to distribute the power correctly between the components.

2). HIGH CURRENT

The connection of Transil in parallel is generally not possible. Other methods can be utilized.

Figure 20 gives the peak power P_P of the Transil as a function of the pulse duration. The utilization of other components with Transil enables extending their area of application.

2.1 The current ratings of a Transil are multiplied by the current gain of the transitors. The transistors ratings, which then operates linearly, should be determined as a function of its «second breakdown» characteristics (determined by the safety area in linear and pulsatory operation). For this type of operation it is advisable to utilize (as soon as the voltage exceeds twenty volts) transitors with a technology suited to linear operation.

2.2 A capacitor previously charged to a voltage V, sees this voltage increasing by a quantity $\Delta V = 1/C\ \Delta Q$, where ΔQ is the quantity of electricity which comes from the surge. The connection of capacitors across Transil enables a considerable increase in their area of utilization, particularly for pulses of short duration and high amplitude.

2.3 The association with other components like lightning arresters also enables extending the application area of Transil.

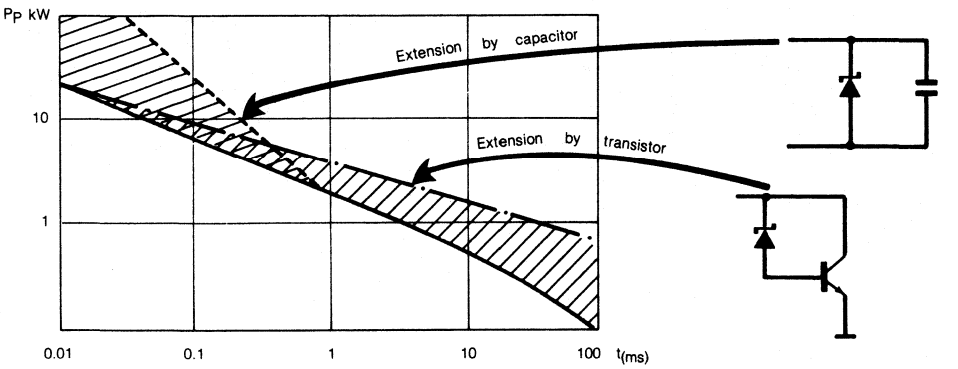


Figure 20 *- Extension of the application area.*

PRACTICAL CONSIDERATION

1). CONNECTION OF TRANSIL

A considerable proportion of the over voltages against which equipment is protected, by Transil have short rise times. The wiring of the Transil should thus be considered as «high frequency» wiring if effective protection is to be obtained.

a). Parasitic inductances can introduce considerable over voltages (Fig. 21).

b). Coupling by unwanted capacitances and especially by mutual inductance can produce disturbances in the neighbouring circuit.

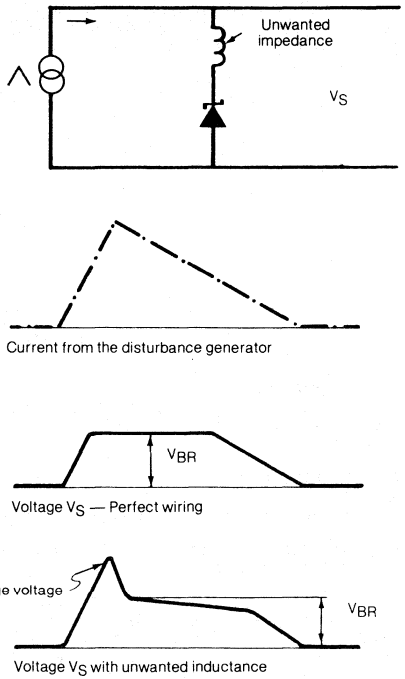
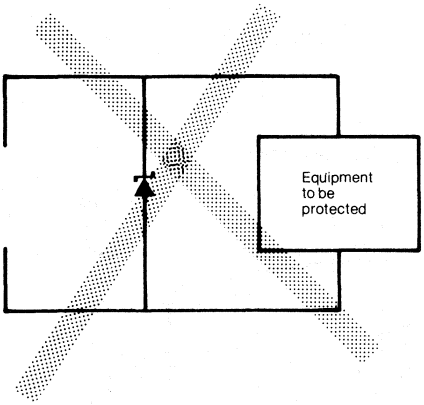


Figure 21 · *Clamping by Transil.*



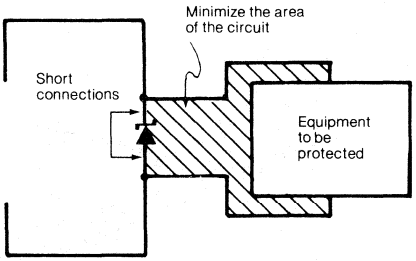


Figure 22 · *Connection of a Transil.*

2). ESTIMATION OF SURGE CURRENTS

The «energy» aspect is fundamental in the protection against over voltages. The component should :

1 — First be capable of dissipating the energy of the surge.

2 — Then have a sufficiently low dynamic resistance to limit the clamping voltage.

If Transil are compared to other devices offering protection against over voltages, one can observe that Transil are characterized by an excellent clamping factor (i.e. by a low dynamic resistance r_D).

Suppose that V_1 is the maximum value of the over voltages, ρ is the internal impedance of the over voltages source, and r_D the dynamic resistance of the Transil.

$$I_P = \frac{V_S - V_{CL}}{\rho + r_D}$$

$$V_S = V_{CL} + \frac{r_D}{r_D + \rho} V_1$$

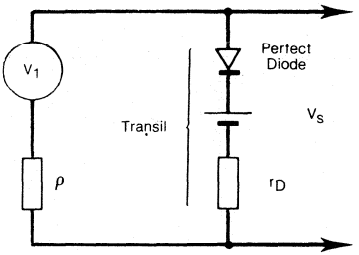


Figure 23

The first parameter to establish in order to determine the right Transil is the peak current I_P (and its duration). Although we begin to know the level of the over voltages encountered in various equipment (an abundant bibliograph exists on this subject), the internal impedance of the various networks is still to a large extent unknown. Nevertheless this is a quantity whose knowlege is fundamental, since it determines the level of power which will have to be dissipated by the Transil.

The determination of the protection level is part of the responsability of the designer : in the absence of accurate data, the following elements discovered from experience, could help to clarify the choices.

The over voltages can be divided into two major categories.

2.1 Over voltages from atmospheric origin

By far the majority of these over voltages are generated by a coupling, generally capacitive, between the source (atmospheric discharge) and the equipment to be protected.

The over voltages are characterized by :

- an amplitude which can be very high,
- dV/dt gradients which are also often high,
- a relatively high internal impedance of the source of the voltage surge.

On power lines, over voltages are generally short and can be simulated by the conventional 1/50 μs exponential wave used in the testing of electrotechnic equipment. In the case of electronic equipment whose power is approximately several kW (or less) it was considered necessary to standardize slightly longer exponential waves (10/1000 us) since operating conditions differ from those of the power lines.

With respect to this type of over voltages, the following average values can be given to ρ :

	Signaling or communication network	220 V mains	280 V mains (P < 10 kW)
ρ (Ω)	200	50	30

2.2 Over voltages from electrotechnical origin

Sometimes called «switching over voltages» these over voltages are produced by transients on the mains (coupling of lines or transformers, freeing of energy contained in transformers, inductances, etc.).

Their amplitude is much lower than that of atmospheric over voltages. They are generally somewhat longer and often more dangerous since the equivalent internal impedance of the mains can be low. They produce less disturbance on the level of electronic circuits (lower dV/dt gradient) but lead more easily to the destruction of the power components.

In order to get an idea of the order of magnitude, the following values can be given for the internal impedances of industrial networks.

- For the 220 V single phase mains : R = 0.2 + j 0.06 f
- For 380 V 3-phase mains, P 10 kW : R = 0.05 + j 0.02 f (where f is the frequency of the disturbance in Hz).

For on-board mains aeronautics, there now are standards fixing values approaching those above.

In general, the rules should be applied prudently and the presence of large transformers on the power mains, liable to be switched when off-load, could produce much more powerful surges.

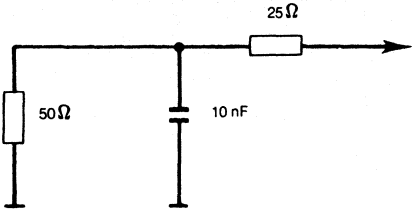


***Figure 24** - Internal impedance of the exponential shock wave generator in accordance with specification CNET ST/DAS/PRL/011.*

2.3 Long duration over voltages of electrotechnical origin

The amplitude of these over voltages could reach 10 to 25 % that on the main lines and could increase to 40 % or even more for the on-board mains. In all these case it must be considered that the internal impedance of the source is not modified and that the protecting component should withstand the over voltages in continuous operation.

3. BEHAVIOUR OF TRANSIL IN CASE OF ABNORMAL OVERLOADING

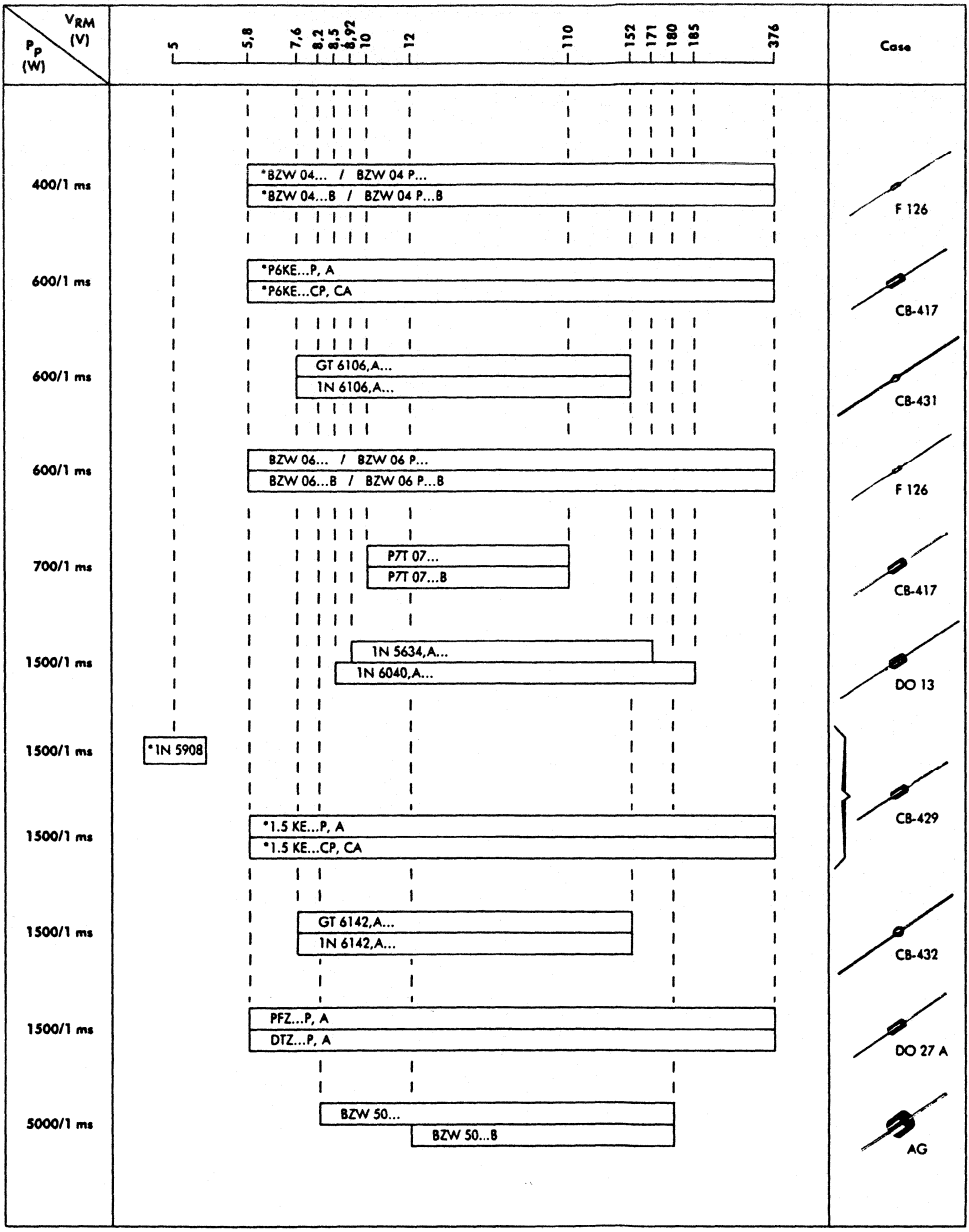
If a Transil is subjected to an overload which far exceeds the «absolute utilization limits», the temperatures arising locally in the form of hot spots could be sufficiently high to cause lasting damage (localized fusion). This generally destroys the diode which then behaves like a short-circuit. (In certain rare cases, the Transil could be damaged so that it has a high leakage current without a clear short-circuit).

See technical information note 83-14

Long-term reliability

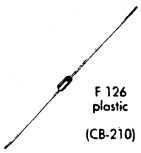
Most of the protecting components, lightning arresters, and metal oxide varistors, have their characteristics altered quickly after a certain number of surges. With a Transil, a silicon component, this phenomenon of «ageing» does not exist. The characteristics of Transil, like those of transistors and Zener diodes, etc. remain particularly stable.

TRANSIENT VOLTAGE SUPPRESSOR "TRANSIL" SELECTOR GUIDE



TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V)			@ I_R	$V_{(CL)}$ @ I_{pp} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
400 W / 1 ms expo.											**I_{FSM} = 50 A - 10 ms for unidirectional**
P BZW04P5V8	P BZW04P5V8B	1000	5,8	6,45	6,8	7,48	10	10,5	38	5,7	
BZW04-5V8	BZW04-5V8B	1000	5,8	6,45	6,8	7,14	10	10,5	38	5,7	
P BZW04P6V4	P BZW04P6V4B	500	6,4	7,13	7,5	8,25	10	11,3	35,4	6,1	
BZW04-6V4	BZW04-6V4B	500	6,4	7,13	7,5	7,88	10	11,3	35,4	6,1	
BZW04P7V0	BZW04P7V0B	200	7,02	7,79	8,2	9,02	10	12,1	33	6,5	
BZW04-7V0	BZW04-7V0B	200	7,02	7,79	8,2	8,61	10	12,1	33	6,5	
BZW04P7V8	BZW04P7V8B	50	7,78	8,65	9,1	10,0	1	13,4	30	6,8	
BZW04-7V8	BZW04-7V8B	50	7,78	8,65	9,1	9,55	1	13,4	30	6,8	
BZW04P8V5	BZW04P8V5B	10	8,55	9,50	10	11,0	1	14,5	27,6	7,3	
BZW04-8V5	BZW04-8V5B	10	8,55	9,50	10	10,50	1	14,5	27,6	7,3	
BZW04P9V4	BZW04P9V4B	5	9,4	10,5	11	12,1	1	15,6	25,7	7,5	
BZW04-9V4	BZW04-9V4B	5	9,4	10,5	11	11,6	1	15,6	25,7	7,5	
P BZW04P10	P BZW04P10B	5	10,2	11,4	12	13,2	1	16,7	24	7,8	
BZW04-10	BZW04-10B	5	10,2	11,4	12	12,6	1	16,7	24	7,8	
BZW04P11	BZW04P11B	5	11,1	12,4	13	14,3	1	18,2	22	8,1	
BZW04-11	BZW04-11B	5	11,1	12,4	13	13,7	1	18,2	22	8,1	
P BZW04P13	P BZW04P13B	5	12,8	14,3	15	16,5	1	21,2	19	8,4	
BZW04-13	BZW04-13B	5	12,8	14,3	15	15,8	1	21,2	19	8,4	
BZW04P14	BZW04P14B	5	13,6	15,2	16	17,6	1	22,5	17,8	8,6	
BZW04-14	BZW04-14B	5	13,6	15,2	16	16,8	1	22,5	17,8	8,6	
BZW04P15	BZW04P15B	5	15,3	17,1	18	19,8	1	25,2	16	8,8	
BZW04-15	BZW04-15B	5	15,3	17,1	18	18,9	1	25,2	16	8,8	
BZW04P17	BZW04P17B	5	17,1	19	20	22	1	27,7	14,5	9,0	
BZW04-17	BZW04-17B	5	17,1	19	20	21	1	27,7	14,5	9,0	
BZW04P19	BZW04P19B	5	18,8	20,9	22	24,2	1	30,6	13	9,2	
BZW04-19	BZW04-19B	5	18,8	20,9	22	23,1	1	30,6	13	9,2	
P BZW04P20	P BZW04P20B	5	20,5	22,8	24	26,4	1	33,2	12	9,4	
BZW04-20	BZW04-20B	5	20,5	22,8	24	25,2	1	33,2	12	9,4	
P BZW04P23	BZW04P23B	5	23,1	25,7	27	29,7	1	37,5	10,7	9,6	
BZW04-23	BZW04-23B	5	23,1	25,7	27	28,4	1	37,5	10,7	9,6	
P BZW04P26	BZW04P26B	5	25,6	28,5	30	33	1	41,5	9,6	9,7	
BZW04-26	BZW04-26B	5	25,6	28,5	30	31,5	1	41,5	9,6	9,7	
P BZW04P28	P BZW04P28B	5	28,2	31,4	33	36,3	1	45,7	8,8	9,8	
BZW04-28	BZW04-28B	5	28,2	31,4	33	34,7	1	45,7	8,8	9,8	
P BZW04P31	P BZW04P31B	5	30,8	34,2	36	39,6	1	49,9	8	9,9	
BZW04-31	BZW04-31B	5	30,8	34,2	36	37,8	1	49,9	8	9,9	
P BZW04P33	P BZW04P33B	5	33,3	37,1	39	42,9	1	53,9	7,4	10,0	
BZW04-33	BZW04-33B	5	33,3	37,1	39	41	1	53,9	7,4	10,0	
BZW04P37	BZW04P37B	5	36,8	40,9	43	47,3	1	59,3	6,7	10,1	
BZW04-37	BZW04-37B	5	36,8	40,9	43	45,2	1	59,3	6,7	10,1	
BZW04P40	BZW04P40B	5	40,2	44,7	47	51,7	1	64,8	6,2	10,1	
BZW04-40	BZW04-40B	5	40,2	44,7	47	49,4	1	64,8	6,2	10,1	
BZW04P44	BZW04P44B	5	43,6	48,5	51	56,1	1	70,1	5,7	10,2	
BZW04-44	BZW04-44B	5	43,6	48,5	51	53,6	1	70,1	5,7	10,2	
BZW04P48	BZW04P48B	5	47,8	53,2	56	61,6	1	77	5,2	10,3	
BZW04-48	BZW04-48B	5	47,8	53,2	56	58,8	1	77	5,2	10,3	
BZW04P53	BZW04P53B	5	53	58,9	62	68,2	1	85	4,7	10,4	
BZW04-53	BZW04-53B	5	53	58,9	62	65,1	1	85	4,7	10,4	
P BZW04P58	P BZW04P58B	5	58,1	64,6	68	74,8	1	92	4,3	10,4	
BZW04-58	BZW04-58B	5	58,1	64,6	68	71,4	1	92	4,3	10,4	
BZW04P64	BZW04P64B	5	64,1	71,3	75	82,5	1	103	3,9	10,5	
BZW04-64	BZW04-64B	5	64,1	71,3	75	78,8	1	103	3,9	10,5	
P BZW04P70	P BZW04P70B	5	70,1	77,9	82	90,2	1	113	3,5	10,5	
BZW04-70	BZW04-70B	5	70,1	77,9	82	86,1	1	113	3,5	10,5	
BZW04P78	BZW04P78B	5	77,8	86,5	91	100	1	125	3,2	10,6	
BZW04-78	BZW04-78B	5	77,8	86,5	91	95,5	1	125	3,2	10,6	
P BZW04P85	P BZW04P85B	5	85,5	95	100	110	1	137	2,9	10,6	
BZW04-85	BZW04-85B	5	85,5	95	100	105	1	137	2,9	10,6	
BZW04P94	BZW04P94B	5	94	105	110	121	1	152	2,6	10,7	
BZW04-94	BZW04-94B	5	94	105	110	116	1	152	2,6	10,7	



F 126
plastic
(CB-210)

* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.
P : Preferred device.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{pp} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
400 W / 1 ms expo.										**I_{FSM} = 50 A - 10 ms for unidirectional**	
BZW04P102	BZW04P102B	5	102	114	120	132	1	165	2,4	10,7	F 126 plastic (CB-210)
BZW04-102	BZW04-102B	5	102	114	120	126	1	165	2,4	10,7	
BZW04P111	BZW04P111B	5	111	124	130	143	1	179	2,2	10,7	
BZW04-111	BZW04-111B	5	111	124	130	137	1	179	2,2	10,7	
P BZW04P128	P BZW04P128B	5	128	143	150	165	1	207	2,0	10,8	
BZW04-128	BZW04-128B	5	128	143	150	158	1	207	2,0	10,8	
BZW04P136	P BZW04P136B	5	136	152	160	176	1	219	1,8	10,8	
BZW04-136	BZW04-136B	5	136	152	160	168	1	219	1,8	10,8	
BZW04P145	BZW04P145B	5	145	161	170	187	1	234	1,7	10,8	
BZW04-145	BZW04-145B	5	145	161	170	179	1	234	1,7	10,8	
BZW04P154	BZW04P154B	5	154	171	180	198	1	246	1,6	10,8	
BZW04-154	BZW04-154B	5	154	171	180	189	1	246	1,6	10,8	
BZW04P171	P BZW04P171B	5	171	190	200	220	1	274	1,5	10,8	
BZW04-171	BZW04-171B	5	171	190	200	210	1	274	1,5	10,8	
BZW04P188	BZW04P188B	5	188	209	220	242	1	301	1,4	10,8	
BZW04-188	BZW04-188B	5	188	209	220	231	1	301	1,4	10,8	
BZW04P213	BZW04P213B	5	213	237	250	275	1	344	1,5	11	
BZW04-213	BZW04-213B	5	213	237	250	263	1	344	1,5	11	
BZW04P239	BZW04P239B	5	239	266	280	308	1	384	1,5	11	
BZW04-239	BZW04-239B	5	239	266	280	294	1	384	1,5	11	
BZW04P256	BZW04P256B	5	256	285	300	330	1	414	1,2	11	
BZW04-256	BZW04-256B	5	256	285	300	315	1	414	1,2	11	
BZW04P273	BZW04P273B	5	273	304	320	352	1	438	1,2	11	
BZW04-273	BZW04-273B	5	273	304	320	336	1	438	1,2	11	
BZW04P299	BZW04P299B	5	299	332	350	385	1	482	0,9	11	
BZW04-299	BZW04-299B	5	299	332	350	368	1	482	0,9	11	
BZW04P342	P BZW04P342B	5	342	380	400	440	1	548	0,9	11	
BZW04-342	BZW04-342B	5	342	380	400	420	1	548	0,9	11	
BZW04P376	P BZW04P376B	5	376	418	440	484	1	603	0,8	11	
BZW04-376	BZW04-376B	5	376	418	440	462	1	603	0,8	11	
600 W / 1 ms expo.										**I_{FSM} = 100 A - 10 ms for unidirectional**	
BZW06P5V8	BZW06P5V8B	1000	5,8	6,45	6,8	7,48	10	10,5	57	5,7	F 126 plastic (CB-210)
BZW06-5V8	BZW06-5V8B	1000	5,8	6,45	6,8	7,14	10	10,5	57	5,7	
BZW06P6V4	BZW06P6V4B	500	6,4	7,13	7,5	8,25	10	11,3	53	6,1	
BZW06-6V4	BZW06-6V4B	500	6,4	7,13	7,5	7,88	10	11,3	53	6,1	
BZW06P7V0	BZW06P7V0B	200	7,02	7,79	8,2	9,02	10	12,1	50	6,5	
BZW06-7V0	BZW06-7V0B	200	7,02	7,79	8,2	8,61	10	12,1	50	6,5	
BZW06P7V8	BZW06P7V8B	50	7,78	8,65	9,1	10	1	13,4	45	6,8	
BZW06-7V8	BZW06-7V8B	50	7,78	8,65	9,1	9,55	1	13,4	45	6,8	
BZW06P8V5	BZW06P8V5B	10	8,55	9,5	10	11	1	14,5	41	7,3	
BZW06-8V5	BZW06-8V5B	10	8,55	9,5	10	10,5	1	14,5	41	7,3	
BZW06P9V4	BZW06P9V4B	5	9,4	10,5	11	12,1	1	15,6	38	7,5	
BZW06-9V4	BZW06-9V4B	5	9,4	10,5	11	11,6	1	15,6	38	7,5	
BZW06P10	BZW06P10B	5	10,2	11,4	12	13,2	1	16,7	36	7,8	
BZW06-10	BZW06-10B	5	10,2	11,4	12	12,6	1	16,7	36	7,8	
BZW06P11	BZW06P11B	5	11,1	12,4	13	14,3	1	18,2	33	8,1	
BZW06-11	BZW06-11B	5	11,1	12,4	13	13,7	1	18,2	33	8,1	
BZW06P13	BZW06P13B	5	12,8	14,3	15	16,5	1	21,2	28	8,4	
BZW06-13	BZW06-13B	5	12,8	14,3	15	15,8	1	21,2	28	8,4	
BZW06P14	BZW06P14B	5	13,6	15,2	16	17,6	1	22,5	27	8,6	
BZW06-14	BZW06-14B	5	13,6	15,2	16	16,8	1	22,5	27	8,6	
BZW06P15	BZW06P15B	5	15,3	17,1	18	19,8	1	25,2	24	8,8	
BZW06-15	BZW06-15B	5	15,3	17,1	18	18,9	1	25,2	24	8,8	
BZW06P17	BZW06P17B	5	17,1	19	20	22	1	27,7	22	9,0	
BZW06-17	BZW06-17B	5	17,1	19	20	21	1	27,7	22	9,0	
BZW06P19	BZW06P19B	5	18,8	20,9	22	24,2	1	30,6	20	9,2	
BZW06-19	BZW06-19B	5	18,8	20,9	22	23,1	1	30,6	20	9,2	
BZW06P20	BZW06P20B	5	20,5	22,8	24	26,4	1	33,2	18	9,4	
BZW06-20	BZW06-20B	5	20,5	22,8	24	25,2	1	33,2	18	9,4	
BZW06P23	BZW06P23B	5	23,1	25,7	27	29,7	1	37,5	16	9,6	
BZW06-23	BZW06-23B	5	23,1	25,7	27	28,4	1	37,5	16	9,6	

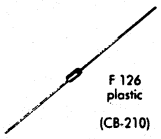
* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

P : Preferred device.

note : For new designing (BZW06 series), refer to P6KE series.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{PP} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
600 W / 1 ms expo.										**I_{FSM} = 100 A - 10 ms for unidirectional**	
BZW06P26	BZW06P26B	5	25,6	28,5	30	33	1	41,4	14,5	9,7	
BZW06-26	BZW06-26B	5	25,6	28,5	30	31,5	1	41,4	14,5	9,7	
BZW06P28	BZW06P28B	5	28,2	31,4	33	36,3	1	45,7	13,1	9,8	
BZW06-28	BZW06-28B	5	28,2	31,4	33	34,7	1	45,7	13,1	9,8	
BZW06P31	BZW06P31B	5	30,8	34,2	36	39,6	1	49,9	12	9,9	
BZW06-31	BZW06-31B	5	30,8	34,2	36	37,8	1	49,9	12	9,9	
BZW06P33	BZW06P33B	5	33,3	37,1	39	42,9	1	53,9	11,1	10,0	
BZW06-33	BZW06-33B	5	33,3	37,1	39	41	1	53,9	11,1	10,0	
BZW06P37	BZW06P37B	5	36,8	40,9	43	47,3	1	59,3	10,1	10,1	
BZW06-37	BZW06-37B	5	36,8	40,9	43	45,2	1	59,3	10,1	10,1	
BZW06P40	BZW06P40B	5	40,2	44,7	47	51,7	1	64,8	9,3	10,1	
BZW06-40	BZW06-40B	5	40,2	44,7	47	49,4	1	64,8	9,3	10,1	
BZW06P44	BZW06P44B	5	43,6	48,5	51	56,1	1	70,1	8,6	10,2	
BZW06-44	BZW06-44B	5	43,6	48,5	51	53,6	1	70,1	8,6	10,2	
BZW06P48	BZW06P48B	5	47,8	53,2	56	61,6	1	77	7,8	10,3	
BZW06-48	BZW06-48B	5	47,8	53,2	56	58,8	1	77	7,8	10,3	
BZW06P53	BZW06P53B	5	53	58,9	62	68,2	1	85	7,1	10,4	
BZW06-53	BZW06-53B	5	53	58,9	62	65,1	1	85	7,1	10,4	
BZW06P58	BZW06P58B	5	58,1	64,6	68	74,8	1	92	6,5	10,4	
BZW06-58	BZW06-58B	5	58,1	64,6	68	71,4	1	92	6,5	10,4	
BZW06P64	BZW06P64B	5	64,1	71,3	75	82,5	1	103	5,8	10,5	
BZW06-64	BZW06-64B	5	64,1	71,3	75	78,8	1	103	5,8	10,5	
BZW06P70	BZW06P70B	5	70,1	77,9	82	90,2	1	113	5,3	10,5	
BZW06-70	BZW06-70B	5	70,1	77,9	82	86,1	1	113	5,3	10,5	
BZW06P78	BZW06P78B	5	77,8	86,5	91	100	1	125	4,8	10,6	
BZW06-78	BZW06-78B	5	77,8	86,5	91	95,5	1	125	4,8	10,6	
BZW06P85	BZW06P85B	5	85,5	95	100	110	1	137	4,4	10,6	
BZW06-85	BZW06-85B	5	85,5	95	100	105	1	137	4,4	10,6	
BZW06P94	BZW06P94B	5	94	105	110	121	1	152	3,9	10,7	
BZW06-94	BZW06-94B	5	94	105	110	116	1	152	3,9	10,7	
BZW06P102	BZW06P102B	5	102	114	120	132	1	165	3,6	10,7	
BZW06-102	BZW06-102B	5	102	114	120	126	1	165	3,6	10,7	
BZW06P111	BZW06P111B	5	111	124	130	143	1	179	3,4	10,7	
BZW06-111	BZW06-111B	5	111	124	130	137	1	179	3,4	10,7	
BZW06P128	BZW06P128B	5	128	143	150	165	1	207	2,9	10,8	
BZW06-128	BZW06-128B	5	128	143	150	158	1	207	2,9	10,8	
BZW06P136	BZW06P136B	5	136	152	160	176	1	219	2,7	10,8	
BZW06-136	BZW06-136B	5	136	152	160	168	1	219	2,7	10,8	
BZW06P145	BZW06P145B	5	145	161	170	187	1	234	2,6	10,8	
BZW06-145	BZW06-145B	5	145	161	170	179	1	234	2,6	10,8	
BZW06P154	BZW06P154B	5	154	171	180	198	1	246	2,4	10,8	
BZW06-154	BZW06-154B	5	154	171	180	189	1	246	2,4	10,8	
BZW06P171	BZW06P171B	5	171	190	200	220	1	274	2,2	10,8	
BZW06-171	BZW06-171B	5	171	190	200	210	1	274	2,2	10,8	
BZW06P188	BZW06P188B	5	188	209	220	242	1	301	2	10,8	
BZW06-188	BZW06-188B	5	188	209	220	231	1	301	2	10,8	
BZW06P213	BZW06P213B	5	213	237	250	275	1	344	2	11	
BZW06-213	BZW06-213B	5	213	237	250	263	1	344	2	11	
BZW06P239	BZW06P239B	5	239	266	280	308	1	384	2	11	
BZW06-239	BZW06-239B	5	239	266	280	294	1	384	2	11	
BZW06P256	BZW06P256B	5	256	285	300	330	1	414	1,6	11	
BZW06-256	BZW06-256B	5	256	285	300	315	1	414	1,6	11	
BZW06P273	BZW06P273B	5	273	304	320	352	1	438	1,6	11	
BZW06-273	BZW06-273B	5	273	304	320	336	1	438	1,6	11	
BZW06P299	BZW06P299B	5	299	332	350	385	1	482	1,6	11	
BZW06-299	BZW06-299B	5	299	332	350	368	1	482	1,6	11	
BZW06P342	BZW06P342B	5	342	380	400	440	1	548	1,3	11	
BZW06-342	BZW06-342B	5	342	380	400	420	1	548	1,3	11	
BZW06P376	BZW06P376B	5	376	418	440	484	1	603	1,3	11	
BZW06-376	BZW06-376B	5	376	418	440	462	1	603	1,3	11	



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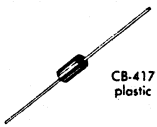
(CB-210)

* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

note : For new designing, refer to P6KE series.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{pp} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
600 W / 1 ms expo.										**I_{FSM} = 100A - 10 ms for unidirectional**	
P6KE 6V8P	P6KE 6V8CP	1000 §	5,8	6,45	6,8	7,48	10	10,5	57	5,7	
P6KE 6V8A	P6KE 6V8CA	1000 §	5,8	6,45	6,8	7,14	10	10,5	57	5,7	
P6KE 7V5P	P6KE 7V5CP	500 §	6,4	7,13	7,5	8,25	10	11,3	53	6,1	
P6KE 7V5A	P6KE 7V5CA	500 §	6,4	7,13	7,5	7,88	10	11,3	53	6,1	
P6KE 8V2P	P6KE 8V2CP	200 §	7,02	7,79	8,2	9,02	10	12,1	50	6,5	
P6KE 8V2A	P6KE 8V2CA	200 §	7,02	7,79	8,2	8,61	10	12,1	50	6,5	
P6KE 9V1P	P6KE 9V1CP	50 §	7,78	8,65	9,1	10	1	13,4	45	6,8	
P6KE 9V1A	P6KE 9V1CA	50 §	7,78	8,65	9,1	9,55	1	13,4	45	6,8	
P6KE 10P	P6KE 10CP	10 §	8,55	9,5	10	11	1	14,5	41	7,3	
P6KE 10A	P6KE 10CA	10 §	8,55	9,5	10	10,5	1	14,5	41	7,3	
P6KE 11P	P6KE 11CP	5 §	9,4	10,5	11	12,1	1	15,6	38	7,5	
P6KE 11A	P6KE 11CA	5 §	9,4	10,5	11	11,6	1	15,6	38	7,5	
P P6KE 12P	P P6KE 12CP	5	10,2	11,4	12	13,2	1	16,7	36	7,8	
P6KE 12A	P6KE 12CA	5	10,2	11,4	12	12,6	1	16,7	36	7,8	
P6KE 13P	P6KE 13CP	5	11,1	12,4	13	14,3	1	18,2	33	8,1	
P6KE 13A	P6KE 13CA	5	11,1	12,4	13	13,7	1	18,2	33	8,1	
P P6KE 15P	P P6KE 15CP	5	12,8	14,3	15	16,5	1	21,2	28	8,4	
P6KE 15A	P6KE 15CA	5	12,8	14,3	15	15,8	1	21,2	28	8,4	
P6KE 16P	P6KE 16CP	5	13,6	15,2	16	17,6	1	22,5	27	8,6	
P6KE 16A	P6KE 16CA	5	13,6	15,2	16	16,8	1	22,5	27	8,6	
P P6KE 18P	P P6KE 18CP	5	15,3	17,1	18	19,8	1	25,2	24	8,8	
P6KE 18A	P6KE 18CA	5	15,3	17,1	18	18,9	1	25,2	24	8,8	
P6KE 20P	P6KE 20CP	5	17,1	19	20	22	1	27,7	22	9,0	
P6KE 20A	P6KE 20CA	5	17,1	19	20	21	1	27,7	22	9,0	
P P6KE 22P	P P6KE 22CP	5	18,8	20,9	22	24,2	1	30,6	20	9,2	
P6KE 22A	P6KE 22CA	5	18,8	20,9	22	23,1	1	30,6	20	9,2	
P P6KE 24P	P P6KE 24CP	5	20,5	22,8	24	26,4	1	33,2	18	9,4	
P6KE 24A	P6KE 24CA	5	20,5	22,8	24	25,2	1	33,2	18	9,4	
P P6KE 27P	P6KE 27CP	5	23,1	25,7	27	29,7	1	37,5	16	9,6	
P6KE 27A	P6KE 27CA	5	23,1	25,7	27	28,4	1	37,5	16	9,6	
P P6KE 30P	P6KE 30CP	5	25,6	28,5	30	33	1	41,4	14,5	9,7	
P6KE 30A	P6KE 30CA	5	25,6	28,5	30	31,5	1	41,4	14,5	9,7	
P P6KE 33P	P P6KE 33CP	5	28,2	31,4	33	36,3	1	45,7	13,1	9,8	
P6KE 33A	P6KE 33CA	5	28,2	31,4	33	34,7	1	45,7	13,1	9,8	
P P6KE 36P	P P6KE 36CP	5	30,8	34,2	36	39,6	1	49,9	12	9,9	
P6KE 36A	P6KE 36CA	5	30,8	34,2	36	37,8	1	49,9	12	9,9	
P P6KE 39P	P P6KE 39CP	5	33,3	37,1	39	42,9	1	53,9	11,1	10,0	
P6KE 39A	P6KE 39CA	5	33,3	37,1	39	41	1	53,9	11,1	10,0	
P6KE 43P	P6KE 43CP	5	36,8	40,9	43	47,3	1	59,3	10,1	10,1	
P6KE 43A	P6KE 43CA	5	36,8	40,9	43	45,2	1	59,3	10,1	10,1	
P6KE 47P	P6KE 47CP	5	40,2	44,7	47	51,7	1	64,8	9,3	10,1	
P6KE 47A	P6KE 47CA	5	40,2	44,7	47	49,4	1	64,8	9,3	10,1	
P6KE 51P	P6KE 51CP	5	43,6	48,5	51	56,1	1	70,1	8,6	10,2	
P6KE 51A	P6KE 51CA	5	43,6	48,5	51	53,6	1	70,1	8,6	10,2	
P6KE 56P	P6KE 56CP	5	47,8	53,2	56	61,6	1	77	7,8	10,3	
P6KE 56A	P6KE 56CA	5	47,8	53,2	56	58,8	1	77	7,8	10,3	
P6KE 62P	P6KE 62CP	5	53	58,9	62	68,2	1	85	7,1	10,4	
P6KE 62A	P6KE 62CA	5	53	58,9	62	65,1	1	85	7,1	10,4	
P P6KE 68P	P P6KE 68CP	5	58,1	64,6	68	74,8	1	92	6,5	10,4	
P6KE 68A	P6KE 68CA	5	58,1	64,6	68	71,4	1	92	6,5	10,4	
P6KE 75P	P6KE 75CP	5	64,1	71,3	75	82,5	1	103	5,8	10,5	
P6KE 75A	P6KE 75CA	5	64,1	71,3	75	78,8	1	103	5,8	10,5	
P P6KE 82P	P P6KE 82CP	5	70,1	77,9	82	90,2	1	113	5,3	10,5	
P6KE 82A	P6KE 82CA	5	70,1	77,9	82	86,1	1	113	5,3	10,5	
P6KE 91P	P6KE 91CP	5	77,8	86,5	91	100	1	125	4,8	10,6	
P6KE 91A	P6KE 91CA	5	77,8	86,5	91	95,5	1	125	4,8	10,6	
P P6KE 100P	P P6KE 100CP	5	85,5	95	100	110	1	137	4,4	10,6	
P6KE 100A	P6KE 100CA	5	85,5	95	100	105	1	137	4,4	10,6	
P6KE 110P	P6KE 110CP	5	94	105	110	121	1	152	3,9	10,7	
P6KE 110A	P6KE 110CA	5	94	105	110	116	1	152	3,9	10,7	
P6KE 120P	P6KE 120CP	5	102	114	120	132	1	165	3,6	10,7	
P6KE 120A	P6KE 120CA	5	102	114	120	126	1	165	3,6	10,7	
P6KE 130P	P6KE 130CP	5	111	124	130	143	1	179	3,4	10,7	
P6KE 130A	P6KE 130CA	5	111	124	130	137	1	179	3,4	10,7	
P P6KE 150P	P P6KE 150CP	5	128	143	150	165	1	207	2,9	10,8	
P6KE 150A	P6KE 150CA	5	128	143	150	158	1	207	2,9	10,8	



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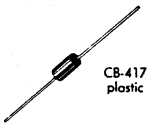
* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

§ For bidirectional types P6KE 6V8CP → P6KE 11 CA, I_{RM} must be double that specified for unidirectional types.

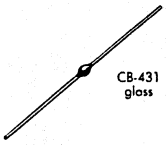
P : Preferred device.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{pp} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(µA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
600 W / 1 ms expo.											**I_{FSM} = 100 A - 10 ms for unidirectional**
P6KE 160P	P P6KE 160CP	5	136	152	160	176	1	219	2,7	10,8	
P6KE 160A	P6KE 160CA	5	136	152	160	168	1	219	2,7	10,8	
P6KE 170P	P6KE 170CP	5	145	161	170	187	1	234	2,6	10,8	
P6KE 170A	P6KE 170CA	5	145	161	170	179	1	234	2,6	10,8	
P6KE 180P	P6KE 180CP	5	154	171	180	198	1	246	2,4	10,8	
P6KE 180A	P6KE 180CA	5	154	171	180	189	1	246	2,4	10,8	
P6KE 200P	P P6KE 200CP	5	171	190	200	220	1	274	2,2	10,8	
P6KE 200A	P6KE 200CA	5	171	190	200	210	1	274	2,2	10,8	
P6KE 220P	P6KE 220CP	5	188	209	220	242	1	301	2	10,8	
P6KE 220A	P6KE 220CA	5	188	209	220	231	1	301	2	10,8	
P6KE 250P	P6KE 250CP	5	213	237	250	275	1	344	2	11	
P6KE 250A	P6KE 250CA	5	213	237	250	263	1	344	2	11	
P6KE 280P	P6KE 280CP	5	239	266	280	308	1	384	2	11	
P6KE 280A	P6KE 280CA	5	239	266	280	294	1	384	2	11	
P P6KE 300P	P P6KE 300CP	5	256	285	300	330	1	414	1,6	11	
P6KE 300A	P6KE 300CA	5	256	285	300	315	1	414	1,6	11	
P6KE 320P	P6KE 320CP	5	273	304	320	352	1	438	1,6	11	
P6KE 320A	P6KE 320CA	5	273	304	320	336	1	438	1,6	11	
P6KE 350P	P6KE 350CP	5	299	332	350	385	1	482	1,6	11	
P6KE 350A	P6KE 350CA	5	299	332	350	368	1	482	1,6	11	
P6KE 400P	P P6KE 400CP	5	342	380	400	440	1	548	1,3	11	
P6KE 400A	P6KE 400CA	5	342	380	400	420	1	548	1,3	11	
P6KE 440P	P P6KE 440CP	5	376	418	440	484	1	603	1,3	11	
P6KE 440A	P6KE 440CA	5	376	418	440	462	1	603	1,3	11	



600 W / 1 ms expo.											**I_{FSM} = 100 A - 10 ms for unidirectional**
GT 6106	1N 6106	20	7,6	9,00	10	11,00	125	15	40	7	
GT 6106 A	1N 6106 A	20	7,6	9,50	10	10,50	125	14,5	41	7	
GT 6107	1N 6107	20	8,4	9,90	11	12,10	125	16,2	37	7	
GT 6107 A	1N 6107 A	20	8,4	10,45	11	11,55	125	15,6	38	7	
GT 6108	1N 6108	20	9,1	10,80	12	13,20	100	17,3	35	7	
GT 6108 A	1N 6108 A	20	9,1	11,40	12	12,60	100	16,7	36	7	
GT 6109	1N 6109	20	9,9	11,70	13	14,30	100	19	32	8	
GT 6109 A	1N 6109 A	20	9,9	12,35	13	13,65	100	18,2	33	8	
GT 6110	1N 6110	20	11,4	13,50	15	16,50	75	22	27,5	8	
GT 6110 A	1N 6110 A	20	11,4	14,25	15	15,75	75	21,2	28	8	
GT 6111	1N 6111	20	12,2	14,40	16	17,60	75	23,5	26	8	
GT 6111 A	1N 6111 A	20	12,2	15,20	16	16,80	75	22,5	27	8	
GT 6112	1N 6112	1	13,7	16,20	18	19,80	65	26,5	22,5	8,5	
GT 6112 A	1N 6112 A	1	13,7	17,10	18	18,90	65	25,2	24	8,5	
GT 6113	1N 6113	1	15,2	18,0	20	22,0	65	29,1	20,5	8,5	
GT 6113 A	1N 6113 A	1	15,2	19,0	20	21,0	65	27,7	22	8,5	
GT 6114	1N 6114	1	16,7	19,8	22	24,2	50	31,9	18,5	8,5	
GT 6114 A	1N 6114 A	1	16,7	20,9	22	23,1	50	30,6	20	8,5	
GT 6115	1N 6115	1	18,2	21,6	24	26,4	50	34,7	17,5	9	
GT 6115 A	1N 6115 A	1	18,2	22,8	24	25,2	50	33,2	18	9	
GT 6116	1N 6116	1	20,6	24,3	27	29,7	50	39,1	15,5	9	
GT 6116 A	1N 6116 A	1	20,6	25,7	27	28,3	50	37,5	16	9	

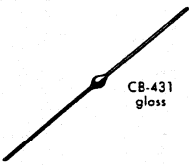


* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

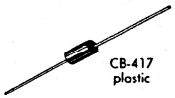
P : Preferred device.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{PP} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(µA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
600 W / 1 ms expo.											**I_{FSM} = 100 A - 10 ms for unidirectional**
GT 6117	1N 6117	1	22,8	27,0	30	33,0	40	43,5	13,5	9	
GT 6117 A	1N 6117 A	1	22,8	28,5	30	31,5	40	41,4	14,5	9	
GT 6118	1N 6118	1	25,1	29,7	33	36,3	40	47,7	12,5	9,5	
GT 6118 A	1N 6118 A	1	25,1	31,4	33	34,6	40	45,7	13,1	9,5	
GT 6119	1N 6119	1	27,4	32,4	36	39,6	30	52	11,5	9,5	
GT 6119 A	1N 6119 A	1	27,4	34,2	36	37,8	30	49,9	12	9,5	
GT 6120	1N 6120	1	29,7	35,1	39	42,9	30	56,4	10,6	9,5	
GT 6120 A	1N 6120 A	1	29,7	37,1	39	40,9	30	53,9	11,1	9,5	
GT 6121	1N 6121	1	32,7	38,7	43	47,3	30	61,9	9,7	9,5	
GT 6121 A	1N 6121 A	1	32,7	40,9	43	45,1	30	59,3	10,1	9,5	
GT 6122	1N 6122	1	35,8	42,3	47	51,7	25	67,8	8,8	9,5	
GT 6122 A	1N 6122 A	1	35,8	44,7	47	49,3	25	64,8	9,3	9,5	
GT 6123	1N 6123	1	38,8	45,9	51	56,1	25	73,5	8,2	9,5	
GT 6123 A	1N 6123 A	1	38,8	48,5	51	53,5	25	70,1	8,6	9,5	
GT 6124	1N 6124	1	42,6	50,4	56	61,6	20	80,5	7,5	9,5	
GT 6124 A	1N 6124 A	1	42,6	53,2	56	58,8	20	77	7,8	9,5	
GT 6125	1N 6125	1	47,1	55,8	62	68,2	20	89	6,7	10	
GT 6125 A	1N 6125 A	1	47,1	58,9	62	65,1	20	85	7,1	10	
GT 6126	1N 6126	1	51,7	61,2	68	74,8	20	98	6,1	10	
GT 6126 A	1N 6126 A	1	51,7	64,6	68	71,4	20	92	6,5	10	
GT 6127	1N 6127	1	56,0	67,5	75	82,5	20	108	5,6	10	
GT 6127 A	1N 6127 A	1	56,0	71,3	75	78,7	20	103	5,8	10	
GT 6128	1N 6128	1	62,2	73,8	82	90,2	15	118	5,1	10	
GT 6128 A	1N 6128 A	1	62,2	77,9	82	86,1	15	113	5,3	10	
GT 6129	1N 6129	1	69,2	81,9	91	100,1	15	131	4,6	10	
GT 6129 A	1N 6129 A	1	69,2	86,5	91	95,5	15	125	4,8	10	
GT 6130	1N 6130	1	76,0	90,0	100	110,0	12	144	4,2	10	
GT 6130 A	1N 6130 A	1	76,0	95,0	100	105,0	12	137	4,4	10	
GT 6131	1N 6131	1	83,6	99,0	110	121,0	12	158	3,8	10	
GT 6131 A	1N 6131 A	1	83,6	104,5	110	115,5	12	152	3,9	10	
GT 6132	1N 6132	1	91,2	108,0	120	132,0	10	173	3,5	10	
GT 6132 A	1N 6132 A	1	91,2	114,0	120	126,0	10	165	3,6	10	
GT 6133	1N 6133	1	98,8	117,0	130	143,0	10	187	3,2	10,5	
GT 6133 A	1N 6133 A	1	98,8	123,5	130	136,5	10	179	3,4	10,5	
GT 6134	1N 6134	1	114,0	135,0	150	165,0	8	215	2,8	10,5	
GT 6134 A	1N 6134 A	1	114,0	142,5	150	157,5	8	207	2,9	10,5	
GT 6135	1N 6135	1	121,6	144	160	176	8	230	2,6	10,5	
GT 6135 A	1N 6135 A	1	121,6	152	160	168	8	219	2,7	10,5	
GT 6136	1N 6136	1	136,8	162	180	198	5	258	2,3	11	
GT 6136 A	1N 6136 A	1	136,8	171	180	189	5	246	2,4	11	
GT 6137	1N 6137	1	152,0	180	200	220	5	287	2,1	11	
GT 6137 A	1N 6137 A	1	152,0	190	200	210	5	274	2,2	11	



700 W / 1 ms expo.												**I_{FSM} = 120 A - 10 ms for unidirectional**
N P7T-10	P7T-10B	5	10	13	16	20	5	25	30	8,4		
N P7T-27	P7T-27B	5	27	29,6	36	43,5	5	53	13	9,8		
N P7T-43	P7T-43B	5	43	50	62	75	5	90	8	10,3		
N P7T-110	P7T-110B	5	110	130	160	200	5	235	3	10,8		



* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

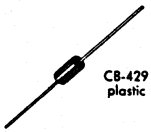
N : New product.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{pp} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(µA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	

1,5 KW / 1 ms expo. **I_{FSM} = 250 A - 10 ms for unidirectional**

P 1.5 KE 6V8 P	P 1.5 KE 6V8 CP	1000	5,8	6,45	6,8	7,48	10	10,5	143	5,7	
1.5 KE 6V8 A	1.5 KE 6V8 CA	1000	5,8	6,45	6,8	7,14	10	10,5	143	5,7	
P 1.5 KE 7V5 P	P 1.5 KE 7V5 CP	500	6,4	7,13	7,5	8,25	10	11,3	132	6,1	
1.5 KE 7V5 A	1.5 KE 7V5 CA	500	6,4	7,13	7,5	7,88	10	11,3	132	6,1	
1.5 KE 8V2 P	1.5 KE 8V2 CP	200	7,02	7,79	8,2	9,02	10	12,1	124	6,5	
1.5 KE 8V2 A	1.5 KE 8V2 CA	200	7,02	7,79	8,2	8,61	10	12,1	124	6,5	
1.5 KE 9V1 P	1.5 KE 9V1 CP	50	7,78	8,65	9,1	10	1	13,4	112	6,8	
1.5 KE 9V1 A	1.5 KE 9V1 CA	50	7,78	8,65	9,1	9,55	1	13,4	112	6,8	
1.5 KE 10 P	1.5 KE 10 CP	10	8,55	9,5	10	11	1	14,5	103	7,3	
1.5 KE 10 A	1.5 KE 10 CA	10	8,55	9,5	10	10,5	1	14,5	103	7,3	
1.5 KE 11 P	1.5 KE 11 CP	5	9,4	10,5	11	12,1	1	15,6	96	7,5	
1.5 KE 11 A	1.5 KE 11 CA	5	9,4	10,5	11	11,6	1	15,6	96	7,5	
1.5 KE 12 P	1.5 KE 12 CP	5	10,2	11,4	12	13,2	1	16,7	90	7,8	
1.5 KE 12 A	1.5 KE 12 CA	5	10,2	11,4	12	12,6	1	16,7	90	7,8	
1.5 KE 13 P	1.5 KE 13 CP	5	11,1	12,4	13	14,3	1	18,2	82	8,1	
1.5 KE 13 A	1.5 KE 13 CA	5	11,1	12,4	13	13,7	1	18,2	82	8,1	
P 1.5 KE 15 P	P 1.5 KE 15 CP	5	12,8	14,3	15	16,5	1	21,2	71	8,4	
1.5 KE 15 A	1.5 KE 15 CA	5	12,8	14,3	15	15,8	1	21,2	71	8,4	
1.5 KE 16 P	1.5 KE 16 CP	5	13,6	15,2	16	17,6	1	22,5	67	8,6	
1.5 KE 16 A	1.5 KE 16 CA	5	13,6	15,2	16	16,8	1	22,5	67	8,6	
P 1.5 KE 18 P	P 1.5 KE 18 CP	5	15,3	17,1	18	19,8	1	25,2	59,5	8,8	
1.5 KE 18 A	1.5 KE 18 CA	5	15,3	17,1	18	18,9	1	25,2	59,5	8,8	
1.5 KE 20 P	1.5 KE 20 CP	5	17,1	19	20	22	1	27,7	54	9	
1.5 KE 20 A	1.5 KE 20 CA	5	17,1	19	20	21	1	27,7	54	9	
P 1.5 KE 22 P	P 1.5 KE 22 CP	5	18,8	20,9	22	24,2	1	30,6	49	9,2	
1.5 KE 22 A	1.5 KE 22 CA	5	18,8	20,9	22	23,1	1	30,6	49	9,2	
P 1.5 KE 24 P	P 1.5 KE 24 CP	5	20,5	22,8	24	26,4	1	33,2	45	9,4	
1.5 KE 24 A	1.5 KE 24 CA	5	20,5	22,8	24	25,2	1	33,2	45	9,4	
P 1.5 KE 27 P	1.5 KE 27 CP	5	23,1	25,7	27	29,7	1	37,5	40	9,6	
1.5 KE 27 A	1.5 KE 27 CA	5	23,1	25,7	27	28,4	1	37,5	40	9,6	
P 1.5 KE 30 P	1.5 KE 30 CP	5	25,6	28,5	30	33	1	41,4	36	9,7	
1.5 KE 30 A	1.5 KE 30 CA	5	25,6	28,5	30	31,5	1	41,4	36	9,7	
P 1.5 KE 33 P	P 1.5 KE 33 CP	5	28,2	31,4	33	36,3	1	45,7	33	9,8	
1.5 KE 33 A	1.5 KE 33 CA	5	28,2	31,4	33	34,7	1	45,7	33	9,8	
P 1.5 KE 36 P	P 1.5 KE 36 CP	5	30,8	34,2	36	39,6	1	49,9	30	9,9	
1.5 KE 36 A	1.5 KE 36 CA	5	30,8	34,2	36	37,8	1	49,9	30	9,9	
P 1.5 KE 39 P	P 1.5 KE 39 CP	5	33,3	37,1	39	42,9	1	53,9	28	10	
1.5 KE 39 A	1.5 KE 39 CA	5	33,3	37,1	39	41	1	53,9	28	10	
1.5 KE 43 P	1.5 KE 43 CP	5	36,8	40,9	43	47,3	1	59,3	25,3	10,1	
1.5 KE 43 A	1.5 KE 43 CA	5	36,8	40,9	43	45,2	1	59,3	25,3	10,1	
1.5 KE 47 P	1.5 KE 47 CP	5	40,2	44,7	47	51,7	1	64,8	23,2	10,1	
1.5 KE 47 A	1.5 KE 47 CA	5	40,2	44,7	47	49,4	1	64,8	23,2	10,1	
1.5 KE 51 P	1.5 KE 51 CP	5	43,6	48,5	51	56,1	1	70,1	21,4	10,2	
1.5 KE 51 A	1.5 KE 51 CA	5	43,6	48,5	51	53,6	1	70,1	21,4	10,2	
1.5 KE 56 P	1.5 KE 56 CP	5	47,8	53,2	56	61,6	1	77	19,5	10,3	
1.5 KE 56 A	1.5 KE 56 CA	5	47,8	53,2	56	58,8	1	77	19,5	10,3	
1.5 KE 62 P	1.5 KE 62 CP	5	53	58,9	62	68,2	1	85	17,7	10,4	
1.5 KE 62 A	1.5 KE 62 CA	5	53	58,9	62	65,1	1	85	17,7	10,4	
P 1.5 KE 68 P	P 1.5 KE 68 CP	5	58,1	64,6	68	74,8	1	92	16,3	10,4	
1.5 KE 68 A	1.5 KE 68 CA	5	58,1	64,6	68	71,4	1	92	16,3	10,4	
1.5 KE 75 P	1.5 KE 75 CP	5	64,1	71,3	75	82,5	1	103	14,6	10,5	
1.5 KE 75 A	1.5 KE 75 CA	5	64,1	71,3	75	78,8	1	103	14,6	10,5	
P 1.5 KE 82 P	P 1.5 KE 82 CP	5	70,1	77,9	82	90,2	1	113	13,3	10,5	
1.5 KE 82 A	1.5 KE 82 CA	5	70,1	77,9	82	86,1	1	113	13,3	10,5	
1.5 KE 91 P	1.5 KE 91 CP	5	77,8	86,5	91	100	1	125	12	10,6	
1.5 KE 91 A	1.5 KE 91 CA	5	77,8	86,5	91	95,5	1	125	12	10,6	
P 1.5 KE 100 P	P 1.5 KE 100 CP	5	85,5	95	100	110	1	137	11	10,6	
1.5 KE 100 A	1.5 KE 100 CA	5	85,5	95	100	105	1	137	11	10,6	
1.5 KE 110 P	1.5 KE 110 CP	5	94	105	110	121	1	152	9,9	10,7	
1.5 KE 110 A	1.5 KE 110 CA	5	94	105	110	116	1	152	9,9	10,7	
1.5 KE 120 P	1.5 KE 120 CP	5	102	114	120	132	1	165	9,1	10,7	
1.5 KE 120 A	1.5 KE 120 CA	5	102	114	120	126	1	165	9,1	10,7	



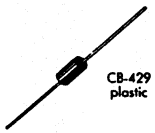
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.

§ For bidirectional types 1.5 KE 6V8 CP → 1.5 KE 11 CA, I_{RM} must be double that specified for unidirectional types.

P : Preferred device.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{pp} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
1,5 KW / 1 ms expo.											**I_{FSM} = 250A - 10 ms for unidirectional**
1.5 KE 130 P	1.5 KE 130 CP	5	111	124	130	143	1	179	8,4	10,7	
1.5 KE 130 A	1.5 KE 130 CA	5	111	124	130	137	1	179	8,4	10,7	
P 1.5 KE 150 P	P 1.5 KE 150 CP	5	128	143	150	165	1	207	7,2	10,8	
1.5 KE 150 A	1.5 KE 150 CA	5	128	143	150	158	1	207	7,2	10,8	
1.5 KE 160 P	P 1.5 KE 160 CP	5	136	152	160	176	1	219	6,8	10,8	
1.5 KE 160 A	1.5 KE 160 CA	5	136	152	160	168	1	219	6,8	10,8	
1.5 KE 170 P	1.5 KE 170 CP	5	145	161	170	187	1	234	6,4	10,8	
1.5 KE 170 A	1.5 KE 170 CA	5	145	161	170	179	1	234	6,4	10,8	
1.5 KE 180 P	1.5 KE 180 CP	5	154	171	180	198	1	246	6,1	10,8	
1.5 KE 180 A	1.5 KE 180 CA	5	154	171	180	189	1	246	6,1	10,8	
P 1.5 KE 200 P	P 1.5 KE 200 CP	5	171	190	200	220	1	274	5,5	10,8	
1.5 KE 200 A	1.5 KE 200 CA	5	171	190	200	210	1	274	5,5	10,8	
P 1.5 KE 220 P	P 1.5 KE 220 CP	5	185	209	220	242	1	328	4,6	10,8	
1.5 KE 220 A	1.5 KE 220 CA	5	185	209	220	231	1	328	4,6	10,8	
1.5 KE 250 P	1.5 KE 250 CP	5	213	237	250	275	1	344	5,0	11	
1.5 KE 250 A	1.5 KE 250 CA	5	213	237	250	263	1	344	5,0	11	
1.5 KE 280 P	1.5 KE 280 CP	5	239	266	280	308	1	384	5,0	11	
1.5 KE 280 A	1.5 KE 280 CA	5	239	266	280	294	1	384	5,0	11	
P 1.5 KE 300 P	P 1.5 KE 300 CP	5	256	285	300	330	1	414	5,0	11	
1.5 KE 300 A	1.5 KE 300 CA	5	256	285	300	315	1	414	5,0	11	
1.5 KE 320 P	1.5 KE 320 CP	5	273	304	320	352	1	438	4,5	11	
1.5 KE 320 A	1.5 KE 320 CA	5	273	304	320	336	1	438	4,5	11	
1.5 KE 350 P	1.5 KE 350 CP	5	299	332	350	385	1	482	4,0	11	
1.5 KE 350 A	1.5 KE 350 CA	5	299	332	350	368	1	482	4,0	11	
P 1.5 KE 400 P	P 1.5 KE 400 CP	5	342	380	400	440	1	548	4,0	11	
1.5 KE 400 A	1.5 KE 400 CA	5	342	380	400	420	1	548	4,0	11	
P 1.5 KE 440 P	1.5 KE 440 CP	5	376	418	440	484	1	603	3,5	11	
1.5 KE 440 A	1.5 KE 440 CA	5	376	418	440	462	1	603	3,5	11	
1,5 KW / 1 ms expo.											**I_{FSM} = 250A - 10 ms for unidirectional**
PFZ 6V8 P	DTZ 6V8 P	1000	5,8	6,45	6,8	7,48	10	10,5	143	5,7	
PFZ 6V8 A	DTZ 6V8 A	1000	5,8	6,45	6,8	7,14	10	10,5	143	5,7	
PFZ 7V5 P	DTZ 7V5 P	500	6,4	7,13	7,5	8,25	10	11,3	132	6,1	
PFZ 7V5 A	DTZ 7V5 A	500	6,4	7,13	7,5	7,88	10	11,3	132	6,1	
PFZ 8V2 P	DTZ 8V2 P	200	7,02	7,79	8,2	9,02	10	12,1	124	6,5	
PFZ 8V2 A	DTZ 8V2 A	200	7,02	7,79	8,2	8,61	10	12,1	124	6,5	
PFZ 9V1 P	DTZ 9V1 P	50	7,78	8,65	9,1	10	1	13,4	112	6,8	
PFZ 9V1 A	DTZ 9V1 A	50	7,78	8,65	9,1	9,55	1	13,4	112	6,8	
PFZ 10 P	DTZ 10 P	10	8,55	9,5	10	11	1	14,5	103	7,3	
PFZ 10 A	DTZ 10 A	10	8,55	9,5	10	10,5	1	14,5	103	7,3	
PFZ 11 P	DTZ 11 P	5	9,4	10,5	11	12,1	1	15,6	96	7,5	
PFZ 11 A	DTZ 11 A	5	9,4	10,5	11	11,6	1	15,6	96	7,5	
PFZ 12 P	DTZ 12 P	5	10,2	11,4	12	13,2	1	16,7	90	7,8	
PFZ 12 A	DTZ 12 A	5	10,2	11,4	12	12,6	1	16,7	90	7,8	
PFZ 13 P	DTZ 13 P	5	11,1	12,4	13	14,3	1	18,2	82	8,1	
PFZ 13 A	DTZ 13 A	5	11,1	12,4	13	13,7	1	18,2	82	8,1	
PFZ 15 P	DTZ 15 P	5	12,8	14,3	15	16,5	1	21,2	71	8,4	
PFZ 15 A	DTZ 15 A	5	12,8	14,3	15	15,8	1	21,2	71	8,4	
PFZ 16 P	DTZ 16 P	5	13,6	15,2	16	17,6	1	22,5	67	8,6	
PFZ 16 A	DTZ 16 A	5	13,6	15,2	16	16,8	1	22,5	67	8,6	
PFZ 18 P	DTZ 18 P	5	15,3	17,1	18	19,8	1	25,2	59,5	8,8	
PFZ 18 A	DTZ 18 A	5	15,3	17,1	18	18,9	1	25,2	59,5	8,8	
PFZ 20 P	DTZ 20 P	5	17,1	19	20	22	1	27,7	54	9	
PFZ 20 A	DTZ 20 A	5	17,1	19	20	21	1	27,7	54	9	
PFZ 22 P	DTZ 22 P	5	18,8	20,9	22	24,2	1	30,6	49	9,2	
PFZ 22 A	DTZ 22 A	5	18,8	20,9	22	23,1	1	30,6	49	9,2	



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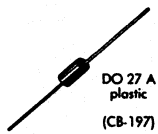

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* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

P : Preferred device.

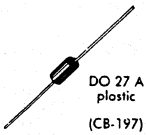
note : For new designing (PFZ/DTZ series), refer to 1.5 KE series.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{PP} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	

1,5 KW / 1 ms expo. **I_{FSM} = 250A - 10 ms for unidirectional**

PFZ 24 P	DTZ 24 P	5	20,5	22,8	24	26,4	1	33,2	45	9,4	
PFZ 24 A	DTZ 24 A	5	20,5	22,8	24	25,2	1	33,2	45	9,4	
PFZ 27 P	DTZ 27 P	5	23,1	25,7	27	29,7	1	37,5	40	9,6	
PFZ 27 A	DTZ 27 A	5	23,1	25,7	27	28,4	1	37,5	40	9,6	
PFZ 30 P	DTZ 30 P	5	25,6	28,5	30	33	1	41,4	36	9,7	
PFZ 30 A	DTZ 30 A	5	25,6	28,5	30	31,5	1	41,4	36	9,7	
PFZ 33 P	DTZ 33 P	5	28,2	31,4	33	36,3	1	45,7	33	9,8	
PFZ 33 A	DTZ 33 A	5	28,2	31,4	33	34,7	1	45,7	33	9,8	
PFZ 36 P	DTZ 36 P	5	30,8	34,2	36	39,6	1	49,9	30	9,9	
PFZ 36 A	DTZ 36 A	5	30,8	34,2	36	37,8	1	49,9	30	9,9	
PFZ 39 P	DTZ 39 P	5	33,3	37,1	39	42,9	1	53,9	28	10	
PFZ 39 A	DTZ 39 A	5	33,3	37,1	39	41	1	53,9	28	10	
PFZ 43 P	DTZ 43 P	5	36,8	40,9	43	47,3	1	59,3	25,3	10,1	
PFZ 43 A	DTZ 43 A	5	36,8	40,9	43	45,2	1	59,3	25,3	10,1	
PFZ 47 P	DTZ 47 P	5	40,2	44,7	47	51,7	1	64,8	23,2	10,1	
PFZ 47 A	DTZ 47 A	5	40,2	44,7	47	49,4	1	64,8	23,2	10,1	
PFZ 51 P	DTZ 51 P	5	43,6	48,5	51	56,1	1	70,1	21,4	10,2	
PFZ 51 A	DTZ 51 A	5	43,6	48,5	51	53,6	1	70,1	21,4	10,2	
PFZ 56 P	DTZ 56 P	5	47,8	53,2	56	61,6	1	77	19,5	10,3	
PFZ 56 A	DTZ 56 A	5	47,8	53,2	56	58,8	1	77	19,5	10,3	
PFZ 62 P	DTZ 62 P	5	53	58,9	62	68,2	1	85	17,7	10,4	
PFZ 62 A	DTZ 62 A	5	53	58,9	62	65,1	1	85	17,7	10,4	
PFZ 68 P	DTZ 68 P	5	58,1	64,6	68	74,8	1	92	16,3	10,4	
PFZ 68 A	DTZ 68 A	5	58,1	64,6	68	71,4	1	92	16,3	10,4	
PFZ 75 P	DTZ 75 P	5	64,1	71,3	75	82,5	1	103	14,6	10,5	
PFZ 75 A	DTZ 75 A	5	64,1	71,3	75	78,8	1	103	14,6	10,5	
PFZ 82 P	DTZ 82 P	5	70,1	77,9	82	90,2	1	113	13,3	10,5	
PFZ 82 A	DTZ 82 A	5	70,1	77,9	82	86,1	1	113	13,3	10,5	
PFZ 91 P	DTZ 91 P	5	77,8	86,5	91	100	1	125	12	10,6	
PFZ 91 A	DTZ 91 A	5	77,8	86,5	91	95,5	1	125	12	10,6	
PFZ 100 P	DTZ 100 P	5	85,5	95	100	110	1	137	11	10,6	
PFZ 100 A	DTZ 100 A	5	85,5	95	100	105	1	137	11	10,6	
PFZ 110 P	DTZ 110 P	5	94	105	110	121	1	152	9,9	10,7	
PFZ 110 A	DTZ 110 A	5	94	105	110	116	1	152	9,9	10,7	
PFZ 120 P	DTZ 120 P	5	102	114	120	132	1	165	9,1	10,7	
PFZ 120 A	DTZ 120 A	5	102	114	120	126	1	165	9,1	10,7	
PFZ 130 P	DTZ 130 P	5	111	124	130	143	1	179	8,4	10,7	
PFZ 130 A	DTZ 130 A	5	111	124	130	137	1	179	8,4	10,7	
PFZ 150 P	DTZ 150 P	5	128	143	150	165	1	207	7,2	10,8	
PFZ 150 A	DTZ 150 A	5	128	143	150	158	1	207	7,2	10,8	
PFZ 160 P	DTZ 160 P	5	136	152	160	176	1	219	6,8	10,8	
PFZ 160 A	DTZ 160 A	5	136	152	160	168	1	219	6,8	10,8	
PFZ 170 P	DTZ 170 P	5	145	161	170	187	1	234	6,4	10,8	
PFZ 170 A	DTZ 170 A	5	145	161	170	179	1	234	6,4	10,8	
PFZ 180 P	DTZ 180 P	5	154	171	180	198	1	246	6,1	10,8	
PFZ 180 A	DTZ 180 A	5	154	171	180	189	1	246	6,1	10,8	
PFZ 200 P	DTZ 200 P	5	171	190	200	220	1	274	5,5	10,8	
PFZ 200 A	DTZ 200 A	5	171	190	200	210	1	274	5,5	10,8	
PFZ 220 P	DTZ 220 P	5	185	209	220	242	1	328	4,6	10,8	
PFZ 220 A	DTZ 220 A	5	185	209	220	231	1	328	4,6	10,8	
PFZ 250 P	DTZ 250 P	5	213	237	250	275	1	344	5,0	10,8	
PFZ 250 A	DTZ 250 A	5	213	237	250	263	1	344	5,0	10,8	
PFZ 280 P	DTZ 280 P	5	239	266	280	308	1	384	5,0	10,8	
PFZ 280 A	DTZ 280 A	5	239	266	280	294	1	384	5,0	10,8	
PFZ 300 P	DTZ 300 P	5	256	285	300	330	1	414	5,0	10,8	
PFZ 300 A	DTZ 300 A	5	256	285	300	315	1	414	5,0	10,8	
PFZ 320 P	DTZ 320 P	5	273	304	320	352	1	438	4,5	10,8	
PFZ 320 A	DTZ 320 A	5	273	304	320	336	1	438	4,5	10,8	
PFZ 350 P	DTZ 350 P	5	299	332	350	385	1	482	4,0	10,8	
PFZ 350 A	DTZ 350 A	5	299	332	350	368	1	482	4,0	10,8	
PFZ 400 P	DTZ 400 P	5	342	380	400	440	1	548	4,0	10,8	
PFZ 400 A	DTZ 400 A	5	342	380	400	420	1	548	4,0	10,8	
PFZ 440 P	DTZ 440 P	5	376	418	440	484	1	603	3,5	10,8	
PFZ 440 A	DTZ 440 A	5	376	418	440	462	1	603	3,5	10,8	



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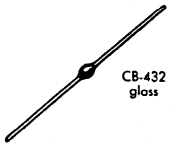
* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.
note : For new designing, refer to 1.5 KE series.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

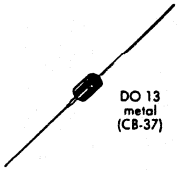
Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{PP} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
1,5 KW / 1 ms expo.											**I_{FSM} = 250 A - 10 ms for unidirectional**
GT 6142	1N 6142	100	7,6	9,00	10	11,00	125	15,2	98,7	7	
GT 6142 A	1N 6142 A	100	7,6	9,50	10	10,50	125	14,5	103,4	7	
GT 6143	1N 6143	20	8,4	9,90	11	12,10	125	16,3	92,0	7	
GT 6143 A	1N 6143 A	20	8,4	10,45	11	11,55	125	15,6	96,2	7	
GT 6144	1N 6144	20	9,1	10,80	12	13,20	100	17,7	84,7	7	
GT 6144 A	1N 6144 A	20	9,1	11,40	12	12,60	100	16,9	88,8	7	
GT 6145	1N 6145	20	9,9	11,70	13	14,30	100	19,0	78,9	8	
GT 6145 A	1N 6145 A	20	9,9	12,35	13	13,65	100	18,2	82,4	8	
GT 6146	1N 6146	20	11,4	13,50	15	16,50	75	21,9	68,5	8	
GT 6146 A	1N 6146 A	20	11,4	14,25	15	15,75	75	21,0	71,4	8	
GT 6147	1N 6147	20	12,2	14,40	16	17,60	75	23,4	64,1	8	
GT 6147 A	1N 6147 A	20	12,2	15,20	16	16,80	75	22,3	67,3	8	
GT 6148	1N 6148	10	13,7	16,20	18	19,80	65	26,3	57,0	8,5	
GT 6148 A	1N 6148 A	10	13,7	17,10	18	18,90	65	25,1	59,8	8,5	
GT 6149	1N 6149	5	15,2	18,0	20	22,0	65	29,0	51,7	8,5	
GT 6149 A	1N 6149 A	5	15,2	19,0	20	21,0	65	27,7	54,2	8,5	
GT 6150	1N 6150	5	16,7	19,8	22	24,2	50	31,9	47,0	8,5	
GT 6150 A	1N 6150 A	5	16,7	20,9	22	23,1	50	30,5	49,2	8,5	
GT 6151	1N 6151	5	18,2	21,6	24	26,4	50	34,8	43,1	9	
GT 6151 A	1N 6151 A	5	18,2	22,8	24	25,2	50	33,3	45,0	9	
GT 6152	1N 6152	5	20,6	24,3	27	29,7	50	39,2	38,3	9	
GT 6152 A	1N 6152 A	5	20,6	25,7	27	28,3	50	37,4	40,1	9	
GT 6153	1N 6153	5	22,8	27,0	30	33,0	40	43,6	34,4	9	
GT 6153 A	1N 6153 A	5	22,8	28,5	30	31,5	40	41,6	36,0	9	
GT 6154	1N 6154	5	25,1	29,7	33	36,3	40	47,9	31,3	9,5	
GT 6154 A	1N 6154 A	5	25,1	31,4	33	34,6	40	45,7	32,8	9,5	
GT 6155	1N 6155	5	27,4	32,4	36	39,6	30	52,3	28,7	9,5	
GT 6155 A	1N 6155 A	5	27,4	34,2	36	37,8	30	49,9	30,1	9,5	
GT 6156	1N 6156	5	29,7	35,1	39	42,9	30	56,2	26,7	9,5	
GT 6156 A	1N 6156 A	5	29,7	37,1	39	40,9	30	53,6	28,0	9,5	
GT 6157	1N 6157	5	32,7	38,7	43	47,3	30	62,0	24,2	9,5	
GT 6157 A	1N 6157 A	5	32,7	40,9	43	45,1	30	59,1	25,4	9,5	
GT 6158	1N 6158	5	35,8	42,3	47	51,7	25	67,7	22,2	9,5	
GT 6158 A	1N 6158 A	5	35,8	44,7	47	49,3	25	64,6	23,2	9,5	
GT 6159	1N 6159	5	38,8	45,9	51	56,1	25	73,5	20,4	9,5	
GT 6159 A	1N 6159 A	5	38,8	48,5	51	53,5	25	70,1	21,4	9,5	
GT 6160	1N 6160	5	42,6	50,4	56	61,6	20	80,7	18,6	9,5	
GT 6160 A	1N 6160 A	5	42,6	53,2	56	58,8	20	77,0	19,5	9,5	
GT 6161	1N 6161	5	47,1	55,8	62	68,2	20	89,3	16,8	10	
GT 6161 A	1N 6161 A	5	47,1	58,9	62	65,1	20	85,3	17,6	10	
GT 6162	1N 6162	5	51,7	61,2	68	74,8	20	98,0	15,3	10	
GT 6162 A	1N 6162 A	5	51,7	64,6	68	71,4	20	97,1	15,4	10	
GT 6163	1N 6163	5	56,0	67,5	75	82,5	20	108,1	13,9	10	
GT 6163 A	1N 6163 A	5	56,0	71,3	75	78,7	20	103,1	14,5	10	
GT 6164	1N 6164	5	62,2	73,8	82	90,2	15	118,2	12,7	10	
GT 6164 A	1N 6164 A	5	62,2	77,9	82	86,1	15	112,8	13,3	10	
GT 6165	1N 6165	5	69,2	81,9	91	100,1	15	131,1	11,4	10	
GT 6165 A	1N 6165 A	5	69,2	86,5	91	95,5	15	125,1	12,0	10	
GT 6166	1N 6166	5	76,0	90,0	100	110,0	12	144,1	10,4	10	
GT 6166 A	1N 6166 A	5	76,0	95,0	100	105,0	12	137,6	10,9	10	
GT 6167	1N 6167	5	83,6	99,0	110	121,0	12	158,5	9,5	10	
GT 6167 A	1N 6167 A	5	83,6	104,5	110	115,5	12	151,3	9,9	10	
GT 6168	1N 6168	5	91,2	108,0	120	132,0	10	172,9	8,7	10	
GT 6168 A	1N 6168 A	5	91,2	114,0	120	126,0	10	165,1	9,1	10	
GT 6169	1N 6169	5	98,8	117,0	130	143,0	10	187,3	8,0	10,5	
GT 6169 A	1N 6169 A	5	98,8	123,5	130	136,5	10	178,8	8,4	10,5	
GT 6170	1N 6170	5	114,0	135,0	150	165,0	8	216,2	6,9	10,5	
GT 6170 A	1N 6170 A	5	114,0	142,5	150	157,5	8	206,3	7,3	10,5	
GT 6171	1N 6171	5	121,6	144	160	176	8	228,8	6,6	10,5	
GT 6171 A	1N 6171 A	5	121,6	152	160	168	8	218,4	6,9	10,5	
GT 6172	1N 6172	5	136,8	162	180	198	5	257,4	5,8	11	
GT 6172 A	1N 6172 A	5	136,8	171	180	189	5	245,7	6,1	11	
GT 6173	1N 6173	5	152,0	180	200	220	5	286,0	5,2	11	
GT 6173 A	1N 6173 A	5	152,0	190	200	210	5	273,0	5,5	11	



* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{PP} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
1,5 KW / 1 ms expo.										**I_{FSM} = 250A - 10 ms**	
1N 5634		5	8,92	9,9	11	12,1	1	16,2	93	7,5	
1N 5634 A		5	9,4	10,5	11	11,6	1	15,6	96	7,5	
1N 5635		5	9,72	10,8	12	13,2	1	17,3	87	7,8	
1N 5635 A		5	10,2	11,4	12	12,6	1	16,7	90	7,8	
1N 5636		5	10,5	11,7	13	14,3	1	19	79	8,1	
1N 5636 A		5	11,1	12,4	13	13,7	1	18,2	82	8,1	
1N 5637		5	12,1	13,5	15	16,5	1	22	68	8,4	
1N 5637 A		5	12,8	14,3	15	15,8	1	21,2	71	8,4	
1N 5638		5	12,9	14,4	16	17,6	1	23,5	64	8,6	
1N 5638 A		5	13,6	15,2	16	16,8	1	22,5	67	8,6	
1N 5639		5	14,5	16,2	18	19,8	1	26,5	56,5	8,8	
1N 5639 A		5	15,3	17,1	18	18,9	1	25,2	59,5	8,8	
1N 5640		5	16,2	18	20	22	1	29,1	51,5	9	
1N 5640 A		5	17,1	19	20	21	1	27,7	54	9	
1N 5641		5	17,8	19,8	22	24,2	1	31,9	47	9,2	
1N 5641 A		5	18,8	20,9	22	23,1	1	30,6	49	9,2	
1N 5642		5	19,4	21,6	24	26,4	1	34,7	43	9,4	
1N 5642 A		5	20,5	22,8	24	25,2	1	33,2	45	9,4	
1N 5643		5	21,8	24,3	27	29,7	1	39,1	38,5	9,6	
1N 5643 A		5	23,1	25,7	27	28,4	1	37,5	40	9,6	
1N 5644		5	24,3	27	30	33	1	43,5	34,5	9,7	
1N 5644 A		5	25,6	28,5	30	31,5	1	41,4	36	9,7	
1N 5645		5	26,8	29,7	33	36,3	1	47,7	31,5	9,8	
1N 5645 A		5	28,2	31,4	33	34,7	1	45,7	33	9,8	
1N 5646		5	29,1	32,4	36	39,6	1	52	29	9,9	
1N 5646 A		5	30,8	34,2	36	37,8	1	49,9	30	9,9	
1N 5647		5	31,6	35,1	39	42,9	1	56,4	26,5	10	
1N 5647 A		5	33,3	37,1	39	41	1	53,9	28	10	
1N 5648		5	34,8	38,7	43	47,3	1	61,9	24	10,1	
1N 5648 A		5	36,8	40,9	43	45,2	1	59,3	25,3	10,1	
1N 5649		5	38,1	42,3	47	51,7	1	67,8	22,2	10,1	
1N 5649 A		5	40,2	44,7	47	49,4	1	64,8	23,2	10,1	
1N 5650		5	41,3	45,9	51	56,1	1	73,5	20,4	10,2	
1N 5650 A		5	43,6	48,5	51	53,6	1	70,1	21,4	10,2	
1N 5651		5	45,4	50,4	56	61,6	1	80,5	18,6	10,3	
1N 5651 A		5	47,8	53,2	56	58,8	1	77	19,5	10,3	
1N 5652		5	50,2	55,8	62	68,2	1	89	16,9	10,4	
1N 5652 A		5	53	58,9	62	65,1	1	85	17,7	10,4	
1N 5653		5	55,1	61,2	68	74,8	1	98	15,3	10,4	
1N 5653 A		5	58,1	64,6	68	71,4	1	92	16,3	10,4	
1N 5654		5	60,7	67,5	75	82,5	1	108	13,9	10,5	
1N 5654 A		5	64,1	71,3	75	78,8	1	103	14,6	10,5	
1N 5655		5	66,4	73,8	82	90,2	1	118	12,7	10,5	
1N 5655 A		5	70,1	77,9	82	86,1	1	113	13,3	10,5	
1N 5656		5	73,7	81,9	91	100	1	131	11,4	10,6	
1N 5656 A		5	77,8	86,5	91	95,5	1	125	12	10,6	
1N 5657		5	81	90	100	110	1	144	10,4	10,6	
1N 5657 A		5	85,5	95	100	105	1	137	11	10,6	
1N 5658		5	89,2	99	110	121	1	158	9,5	10,7	
1N 5658 A		5	94	105	110	116	1	152	9,9	10,7	
1N 5659		5	97,2	108	120	132	1	173	8,7	10,7	
1N 5659 A		5	102	114	120	126	1	165	9,1	10,7	
1N 5660		5	105	117	130	143	1	187	8	10,7	
1N 5660 A		5	111	124	130	137	1	179	8,4	10,7	
1N 5661		5	121	135	150	165	1	215	7	10,8	
1N 5661 A		5	128	143	150	158	1	207	7,2	10,8	



DO 13
metal
(CB-37)

* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

note : 1N 5629,A → 1N 5933,A, on request.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{pp} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
1,5 KW / 1 ms expo. I_{FSM} = 250A - 10 ms for 1N 56.. series											
1N 5662		5	130	144	160	176	1	230	6,5	10,8	
1N 5662 A		5	136	152	160	168	1	219	6,8	10,8	
1N 5663		5	138	153	170	187	1	244	6,2	10,8	
1N 5663 A		5	145	161	170	179	1	234	6,4	10,8	
1N 5664		5	146	162	180	198	1	258	5,8	10,8	
1N 5664 A		5	154	171	180	189	1	246	6,1	10,8	
1N 5665		5	162	180	200	220	1	287	5,2	10,8	
1N 5665 A		5	171	190	200	210	1	274	5,5	10,8	
1,5 KW / 1 ms expo.											
	1N 6040	10	8,5	9,9	11	12,1	1	16,2	93	7,5	DO 13 metal (CB-37)
	1N 6040 A	10	9,0	10,5	11	11,6	1	15,6	96	7,5	
	1N 6041	5	9,0	10,8	12	13,2	1	17,3	87	7,8	
	1N 6041 A	5	10,0	11,4	12	12,6	1	16,7	90	7,8	
	1N 6042	5	10,0	11,7	13	14,3	1	19	79	8,1	
	1N 6042 A	5	11,0	12,4	13	13,7	1	18,2	82	8,1	
	1N 6043	5	11,0	13,5	15	16,7	1	22	68	8,4	
	1N 6043 A	5	12,0	14,3	15	15,8	1	21,2	71	8,4	
	1N 6044	5	12,0	14,4	16	17,6	1	23,5	64	8,6	
	1N 6044 A	5	13,0	15,2	16	16,8	1	22,5	67	8,6	
	1N 6045	5	14,0	16,2	18	19,8	1	26,5	56,5	8,8	
	1N 6045 A	5	15,0	17,1	18	18,9	1	25,2	59,5	8,8	
	1N 6046	5	16,0	18	20	22	1	29,1	51,5	9	
	1N 6046 A	5	17,0	19	20	21	1	27,7	54	9	
	1N 6047	5	17,0	19,8	22	24,2	1	31,9	47	9,2	
	1N 6047 A	5	18,0	20,9	22	23,1	1	30,6	49	9,2	
	1N 6048	5	19,0	21,6	24	26,4	1	34,7	43	9,4	
	1N 6048 A	5	20,0	22,8	24	25,2	1	33,2	45	9,4	
	1N 6049	5	21,0	24,3	27	29,7	1	39,1	38,5	9,6	
	1N 6049 A	5	22,0	25,7	27	28,4	1	37,5	40	9,6	
	1N 6050	5	24,0	27	30	33	1	43,5	34,5	9,7	
	1N 6050 A	5	25,0	28,5	30	31,5	1	41,4	36	9,7	
	1N 6051	5	26,0	29,7	33	36,3	1	47,7	31,5	9,8	
	1N 6051 A	5	28,0	31,4	33	34,7	1	45,7	33	9,8	
	1N 6052	5	29,0	32,4	36	39,6	1	52	29	9,9	
	1N 6052 A	5	30,0	34,2	36	37,8	1	49,9	30	9,9	
	1N 6053	5	31,0	35,1	39	42,9	1	56,4	26,5	10	
	1N 6053 A	5	33,0	37,1	39	41	1	53,9	28	10	
	1N 6054	5	34,0	38,7	43	47,3	1	61,9	24	10,1	
	1N 6054 A	5	36,0	40,9	43	45,2	1	59,3	25,3	10,1	
	1N 6055	5	38,0	42,3	47	51,7	1	67,8	22,2	10,1	
	1N 6055 A	5	40,0	44,7	47	49,4	1	64,8	23,2	10,1	
	1N 6056	5	41,0	45,9	51	56,1	1	73,5	20,4	10,2	
	1N 6056 A	5	43,0	48,5	51	53,6	1	70,1	21,4	10,2	
	1N 6057	5	45,0	50,4	56	61,6	1	80,5	18,6	10,3	
	1N 6057 A	5	47,0	53,2	56	58,8	1	77	19,5	10,3	
	1N 6058	5	48,0	55,8	62	68,2	1	89	16,9	10,4	
	1N 6058 A	5	53,0	58,9	62	65,1	1	85	17,7	10,4	
	1N 6059	5	55,0	61,2	68	74,8	1	98	15,3	10,4	
	1N 6059 A	5	58,0	64,6	68	71,4	1	92	16,3	10,4	

* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

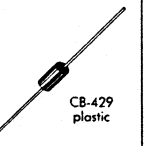
note : 1N 6036,A → 1N 6039,A, on request.

TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL"

Types		I_{RM} @ V_{RM}		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{PP} max 1 ms expo		α_T max	Case
Unidirectional	Bidirectional	(μA)	(V)	min	nom	max	(mA)	(V)	(A)	(10^{-4}/°C)	
1,5 KW / 1 ms expo.											
	1N 6060	5	60,0	67,5	75	82,5	1	108	13,9	10,5	DO 13 metal (CB-37)
	1N 6060 A	5	64,0	71,3	75	78,8	1	103	14,6	10,5	
	1N 6061	5	66,0	73,8	82	90,2	1	118	12,7	10,5	
	1N 6061 A	5	70,0	77,9	82	86,1	1	113	13,3	10,5	
	1N 6062	5	73,0	81,9	91	100,1	1	131	11,4	10,6	
	1N 6062 A	5	75,0	86,5	91	95,5	1	125	12	10,6	
	1N 6063	5	81,0	90	100	110	1	144	10,4	10,6	
	1N 6063 A	5	82,0	95	100	105	1	137	11	10,6	
	1N 6064	5	90,0	99	110	121	1	158	9,5	10,7	
	1N 6064 A	5	94,0	105	110	116	1	152	9,9	10,7	
	1N 6065	5	95,0	108	120	132	1	176	8,5	10,7	
	1N 6065 A	5	100	114	120	126	1	168	8,9	10,7	
	1N 6066	5	105	117	130	143	1	191	7,8	10,7	
	1N 6066 A	5	110	124	130	137	1	182	8,2	10,7	
	1N 6067	5	121	135	150	165	1	223	6,7	10,8	
	1N 6067 A	5	128	143	150	158	1	213	7,0	10,8	
	1N 6068	5	137	153	170	187	1	258	5,8	10,8	
	1N 6068 A	5	145	162	170	179	1	245	6,1	10,8	
	1N 6069	5	145	162	180	198	1	274	5,5	10,8	
	1N 6069 A	5	150	171	180	189	1	261	5,7	10,8	
	1N 6070	5	155	171	190	210	1	292	5,1	10,8	
	1N 6070 A	5	160	181	190	200	1	278	5,4	10,8	
	1N 6071	5	165	180	200	220	1	308	4,9	10,8	
	1N 6071 A	5	170	190	200	210	1	294	5,1	10,8	
	1N 6072	5	175	198	220	242	1	344	4,3	10,8	
	1N 6072 A	5	185	209	220	231	1	328	4,6	10,8	
5 KW / 1 ms expo.											**I_{FSM} = 500A - 10 ms for unidirectional**
BZW 50-8V2		50	8,2	9,1	10,1	11,1	1	15,3	327	7,3	AG plastic (CB-257)
BZW 50-10		5	10	11,1	12,4	13,6	1	18,8	266	7,8	
BZW 50-12	BZW 50-12B	5	12	13,3	14,8	16,3	1	22	227	8,4	
BZW 50-15	BZW 50-15B	5	15	16,6	18,5	20,4	1	26,9	186	8,8	
BZW 50-18	BZW 50-18B	5	18	20	22,2	24,4	1	32,2	155	9,2	
BZW 50-22	BZW 50-22B	5	22	24,4	27,1	29,8	1	39,4	127	9,6	
BZW 50-27	BZW 50-27B	5	27	30	33,3	36,6	1	48,3	103	9,8	
BZW 50-33	BZW 50-33B	5	33	36,6	40,7	44,7	1	59	85	10	
BZW 50-39	BZW 50-39B	5	39	43,3	48,1	53	1	69,4	72	10,1	
BZW 50-47	BZW 50-47B	5	47	52	57,8	63,6	1	83,2	60,1	10,3	
BZW 50-56	BZW 50-56B	5	56	62,2	69,1	76	1	99,6	50	10,4	
BZW 50-68	BZW 50-68B	5	68	75,6	84	92,4	1	121	41	10,5	
BZW 50-82	BZW 50-82B	5	82	91	101,2	111	1	145	34	10,6	
BZW 50-100	BZW 50-100B	5	100	111	123,5	136	1	179	28	10,7	
BZW 50-120	BZW 50-120B	5	120	133	148,1	163	1	215	23	10,8	
BZW 50-150	BZW 50-150B	5	150	166	185,2	204	1	269	19	10,8	
BZW 50-180	BZW 50-180B	5	180	200	222	244	1	322	16	10,8	

* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.

5 VOLTS TRANSIENT VOLTAGE SUPPRESSORS "TRANSIL" FOR MICROPROCESSOR, INTEGRATED CIRCUIT, C-MOS, MOS PROTECTION

Unidirectional type	I_{RM} @ V_{RM}		$V_{(BR)}$* @ I_R min		$V_{(CL)}$ @ I_{PP} max 1 ms expo		$V_{(CL)}$ @ I_{PP} max 1 ms expo		$V_{(CL)}$ @ I_{PP} max 1 ms expo		α_T max	Case
	(μA)	(V)	(V)	(mA)	(V)	(A)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	
1,5 KW / 1 ms expo.												I_{FSM} = 250A - 10 ms
P 1N 5908	300	5	6,0	1	7,6	30	8,0	60	8,5	120	5,7	 CB-429 plastic

* Pulse test $t_p \leq 50$ ms $\delta < 2\%$.
P : Preferred device.

1N 5907 (1.5 KW / 1 ms expo. DO 13) : on request.

cross reference

THOMSON SEMICONDUCTEURS PART N° SERIES	INDUSTRY PART N° SERIES (Similar replacement)
PLASTIC PACKAGES	
BZW 04	TZB
P6KE	P6SE
1.5 KE	1N 6267→1N 6303
1.5 KE	1.5 SE
BZW 50	5 KP
BZW 50	TZV
METAL PACKAGE	
1N 5629→1N 5665 A	1,5 K

«TRISIL»

CROWBAR TYPE PROTECTION DIODE

A. BERNABE · J.P. NOGUIER · P. RAULT

September 1986

I · INTRODUCTION

In the field of parallel protection, the devices used have two main functions in transit operation : **to limit the voltage and to deviate the surge current.**

If the first function is perfectly carried out by an avalanche junction, confirmed by the success of the TRANSIL series, the second is limited by voltage permanently present across the diode terminals.

Utilization of increasingly sophisticated but fragile electronic components and publication of new standards do not allow the use of diodes TRANSIL in certain applications.

This recent problem is solved by the use of a **semiconductor device** with **two conducting states** such as the thyristor (or the triac in the bidirectional version).

From 1983, **THOMSON SEMICONDUCTEURS** has developed this type of component under the trade name of **TRISIL.**

This booklet is meant to explain its operation and applications and help to choose the model which is most suitable to each ones specific requirements.

II · TRISIL CHARACTERISTICS

II.1 · ELECTRICAL CHARACTERISTIC

The electrical characteristic of the TRISIL is similar to that of a TRIAC (Figure 1) except that the component has only two outputs. Triggering in this case is not done via a gate but by **an internal mechanism dependent on the current flowing through it.**

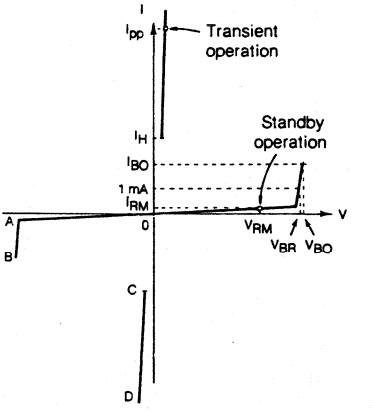


Figure 1 - I / V characteristic of a Trisil

II.2 - OPERATION SEEN FROM THE OUTSIDE

At rest, the TRISIL is biased at a voltage lower than or equal to the standby voltage (V_{RM}). At that point of the characteristic, the leakage current is about ten nanoamperes and the presence of the TRISIL connected across the equipment to be protected does not disturb its operation.

The characteristic data at this point includes : **the leakage current, the electrical capacity and the reliability of the component in blocking.**

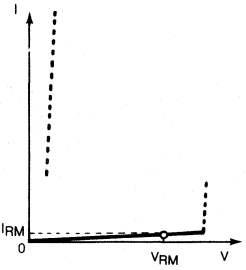


Figure 2 - Low level characteristics

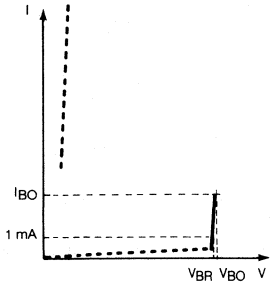


Figure 3 - Avalanche characteristic of the Trisil

During the increase in voltage, the TRISIL impedance drops from practically infinite to a few ohms. The TRISIL remains biased at its avalanche voltage and its operation is then identical to that of a TRANSIL diode.

The characteristic parameters at this level are **the limiting voltage** (breakover voltage of the component, V_{BO}) **and the response time for switching between the blocked and conducting states.**

For current values higher than I_{BO}, the voltage across the TRISIL drops to a few volts and the high currents permitted without damage are possible due to the low value of this voltage, since the physical limit is dependent on the dissipated power.

The characteristic parameters are then the possibility **of withstanding surge currents** (peak-point current, I_{pp}).

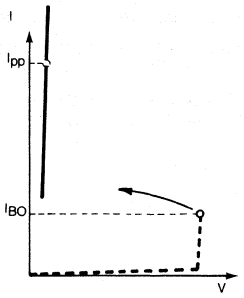


Figure 4 - Triggering characteristics

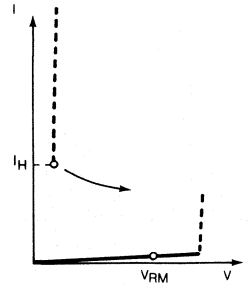


Figure 5 - Return to standby operation

Return to standby operation by turning off the TRISIL takes place when the current flowing through it drops below the **hold current** (I_H) which is the characteristic parameter for switching from the conducting to the blocked state.

The surge current associated with the disturbance is deviated to the TRISIL as soon as it begins to operate in the avalanche mode (Figure 3) and the limiting results from the electrical characteristic at this point. The behaviour of the TRISIL is thus identical to that of the TRANSIL. The difference depends on the level of the breakover current, I_{BO}, where the triggering proper to the thyristor structures take place. This phenomenon results in absolute limiting independent of the current level, on one hand, and a capacity to deviate currents much higher than those possible for an avalanche diode (TRANSIL), and on the other hand, this is done independently of its voltage.

II.3 - LIMITING PROPERTY

Because of its operating mode, the TRISIL results in **absolute limiting, independent of the surge current level** (Figure 6) **and of the slope of the applied voltage ramp** (Figure 7).

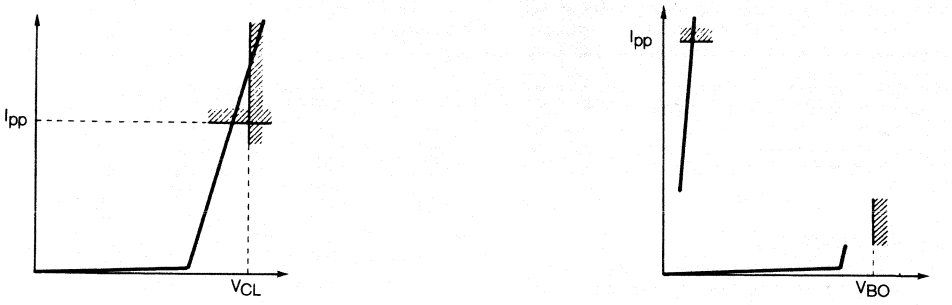


Figure 6 - Correlation between the voltage and the surge current

In particular, if the surge current is higher than the guaranteed value in the catalogue, without however exceeding the physical limits of the component, the voltage across the TRANSIL could reach the critical value destroying the equipment to be protected where as for the TRISIL this risk is excluded.

Finally, for a surge current much higher than the guaranteed value, destruction of the TRISIL always results in a short-circuit thus providing absolute protection for the equipment located downstream.

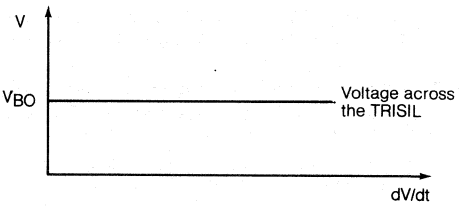


Figure 7 - Correlation between the limiting voltage and the surge voltage ramp

II.4 - BEHAVIOUR IN CASE OF CURRENT SURGES

The ability of semiconductor components to withstand high currents in transient operation is limited for pulses longer than 10 nano-seconds by a second breakdown due to heat. This phenomenon, although not destructive, is considered as the normal utilization limit in so far as the behaviour of the component depends on the external circuit.

The temperature rise within the semiconductor is thus the parameter which defines the behaviour of the component and its capacity to withstand current surges. It is given by equation (1) :

$$T_j = T_a + Z_{th} V_{on} \times I_{RS} \quad (1)$$

With T_j : instant temperature at the junction level

T_a : ambient temperature

Z_{th} : transient thermal impedance (as a function of the duration of the pulse)

V_{on} : voltage across the terminals of the component in the conducting state

I_{RS} : transient current flowing through the component.

This equation clearly shows the advantage of the TRISIL : decrease in the voltage across its terminals enables it to conduct a **much higher current** than the avalanche diode, for example, for the same junction temperature. Besides, since the voltage to be taken into consideration for the calculation is that in the conducting state, the permitted current levels in transient operation are independent of the avalanche voltage and the **guaranteed values are identical for all the types of a given series** (Figure 8).

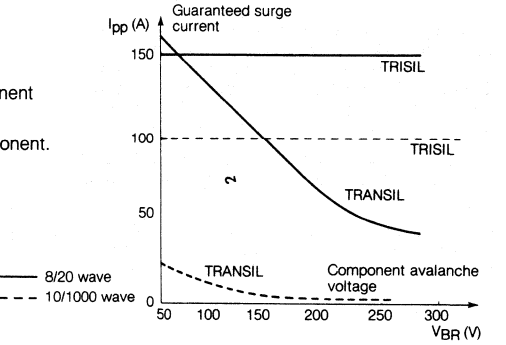


Figure 8 - Comparison of the limit transient currents for a Transil and a Trisil in the same case (CB-429)

The maximum junction temperature taken into account in transient operation is not that given in the catalogues (junction temperature in operation or in storage) but corresponds, with a certain safety margin, to the second breakdown due to thermal causes, i.e. about 350 - 400°C.

This high current capacity can be applied in AC operation at the 50 Hz industrial frequency (Figure 9), a field which is particularly interesting in telephony where equipment should be protected against overvoltages resulting from accidental coupling of the telephone line with the power distribution network. This type of protection is required by certain standards used in telecommunications (Standard RLM 88 - Type II).

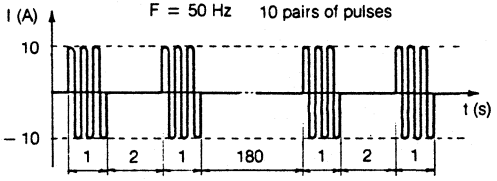


Figure 9 - Long duration overload test (Standard RLM 88 - Type II)

II.5 - RESPONSE SPEED

The response speed of the component is the time **required by it to limit the voltage.** From this point of view the TRISIL has exactly the same behaviour as a TRANSIL. The time is that required to switch from the standby operating point to the avalanche voltage. This is **quasi instantaneous.**

This time should not be confused with that required to pass from the breakover point (V_{BO}) to the conducting characteristic. This time is longer but does not influence the limiting.

II.6 - OPERATION WITHIN THE AVALANCHE AREA

This paragraph concerns the segment AB (Figure 1) of the TRISIL characteristic between the blocked state and the conducting state at low V_{on}.

This portion of the characteristic is identical to that of an avalanche diode. Thus within this area, DC, AC or pulse-type operation are permitted. The currents are limited depending on the possibilities of junction-ambient air heat dissipation. The maximum current is defined by the following inequality (2) :

$$\boxed{T_j = T_a + R_{th}\, V_{BO}\, I_{max} \leqslant T_{jmax} = 150°C} \quad (2)$$

and inequality (3) defining when the TRISIL is not triggered :

$$\boxed{I_{max} < I_{BO}} \quad (3)$$

The main differences from equation (1) are the maximum junction temperature which is now that given by the catalogue, i.e. 150°C, the voltage which is that of the avalanche mechanism and the continuous thermal resistance replacing the transient thermal impedance.

In AC operation, although the equation holds good, the voltage-current diagram as a function of the time (Figure 10) is more clear.

The value of the breakover current (I_{BO}) plays an important part in the capacity of the device in avalanche operation.

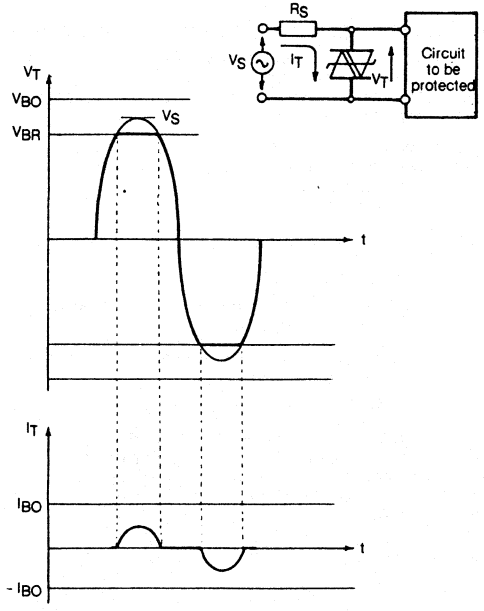
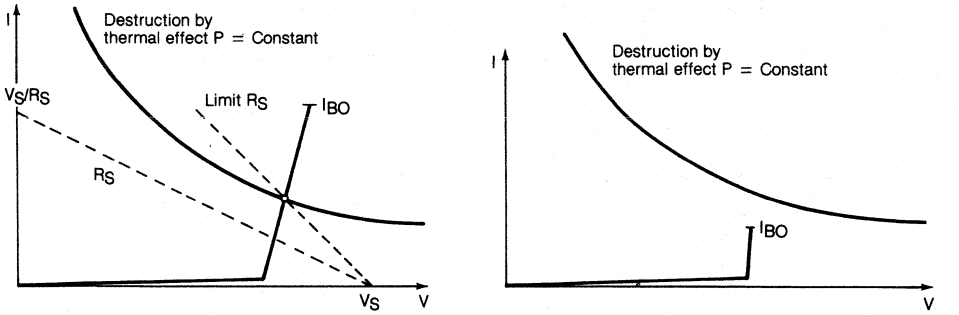


Figure 10 - AC operation in the avalanche mode

If this value is high (Figure 11.a), the current in the component must be limited by a suitable series resistor. For lower values, avalanche operation takes place without destruction whatever the external circuit.

THOMSON SEMICONDUCTEURS has designed a structure with a typical I_{BO} of 70 mA. This value is sufficiently low to enable continuous operation in the avalanche mode, for most applications, and without untimely triggering at the disturbance.



a - Case in which the current should be limited by the external circuit R_S > limit R_S

b - Correct operation whatever the external circuit

Figure 11 - Conditions for non destructive operation in the avalanche mode

II.7 - TRANSIL - TRISIL COMPARISON

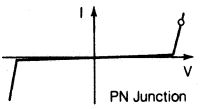
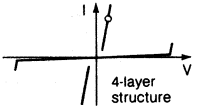
COMPONENT	TRANSIL	TRISIL
IDENTICAL CRITERIA	**Semiconductor component based on PN junctions**	
	I by V characteristic at low level ($I \leqslant I_{BO}$)	
	Limiting time	
	Destruction by short-circuiting for values much higher than those guaranteed	
	Reliability depending on the PN junctions	
	Bi-directional component	
DIFFERENT CRITERIA	**I by V characteristic at high level** 	
	Limiting power Limiting as a function of the current level	Absolute limiting at V_{BO}
	Permitted surge current Decreases as a function of the avalanche voltage $V_{CL} \times I_{PP}$ = Constant	Independent of the avalanche voltage Greater for the same area of silicon
	Voltage range Larger range of voltages, from 6.2 V to 400 V and higher	Limited range with the lower values missing, 62 V to 270 V

Table I - Transil - Trisil Comparison

II.8 - TRISIL - LIGHTNING ARRESTER COMPARISON

COMPONENT	LIGHTNING ARRESTER	TRISIL
IDENTICAL CRITERIA	**Bi-directional component with two states, one blocked and the other conducting** **«Crowbar» type protection**	
DIFFERENT CRITERIA	**Technology**	
	Gas type arrester	Semiconductor component
	Limiting power	
	Limiting depends on the slope of the disturbance voltage	Absolute limiting at V_{BO}
	Limiting time	
	About 1 microsecond	About 1 nanosecond
	Reliability	
	Problem of ageing	High reliability due to semiconductor properties
	Permitted surge current	
	Higher for any given volume	Limited today to 150 A for a standard 8/20 wave

Table II - Trisil - Lighting-arrester comparison

III - TECHNOLOGY

The TRISIL inherits its silicon chip from the medium power thyristor and its setup from the diode with axial wire leads.

III.1 - SILICON CHIP STRUCTURE

The structure resulting in the electrical characteristics of the TRISIL is a SCHOCKLEY diode with 4 NPNP layers in a bidirectional version (Figure 12).

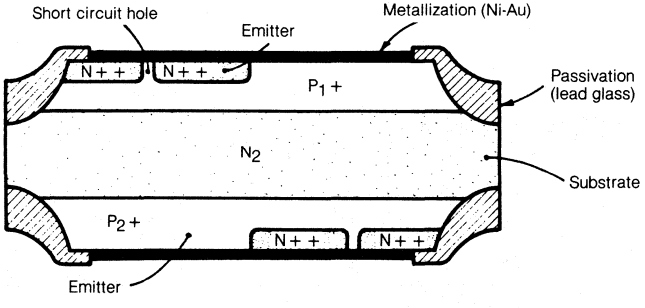
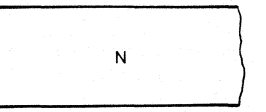


Figure 12 - Silicon chip structure

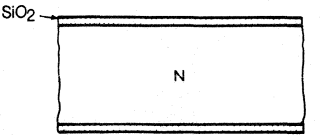
III.2 - MANUFACTURING PROCESS

The component is produced according to the maufacturing process sequence represented in (Figure 13).

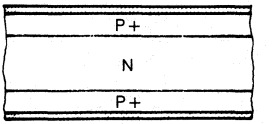
- Selection of the substrate
  Resistivity depending on the voltage required



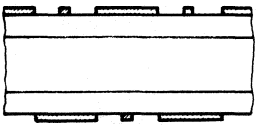
- Thermal oxidation



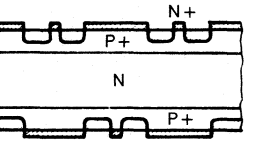
- P diffusion in a sealed tube



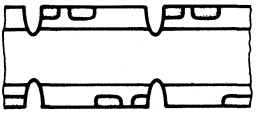
- Opening of the oxide coating to localize the N diffusion



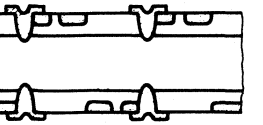
- N diffusion



- Termination of the junction
  . Chemical etching of grooves



- Passivation
  . Lead glass
  Sintering temperature : 860°C



- Metallization

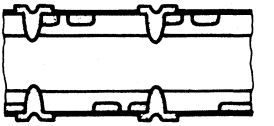


Figure 13 - Diagram of the Trisil structure manufacturing sequence

III.3 - DESCRIPTION OF THE ASSEMBLY

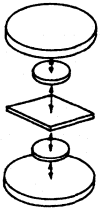
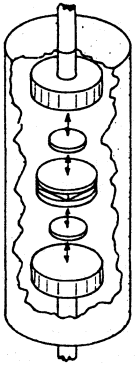
Construction of a sandwich			Case	
			F 126	CB 429
	Aluminium distributor	Ø	1.7 mm	3.3 mm
		thickness	400 µm	400 µm
	Preformed PbSn Fusion T 320°C			
	Silicon chip	length	1.5 mm	2.3 mm
Construction of the diode				
	Copper lead	Ø min.	0.76 mm	
		Ø max.	0.80 mm	1.06 mm
		min. length	26 mm	26 mm
	Preformed SnSb Fusion T 210°C			
	Plastic coating	Ø max.	3.05 mm	5.1 mm
		max. length	6.35 mm	9.8 mm
TRISIL reference			TPA	TPB

Table III - Diagram of the assembly of a diode with axial wire leads

III.4 - OPERATION SEEN FROM WITHIN

The TRISIL in fact consists of two thyristors connected in parallel head-to-tail. It is enough to explain the operation of one. The other operates in the same way if the voltage across the component is reversed.

Application of a negative voltage on cathode N + + results in direct biasing of junctions J_1 and J_2 and reverse biasing of J_2.

The current observed is thus the leakage current of junction J_2.

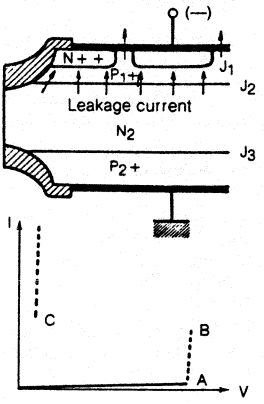


Figure 14 - Operation in the blocked mode

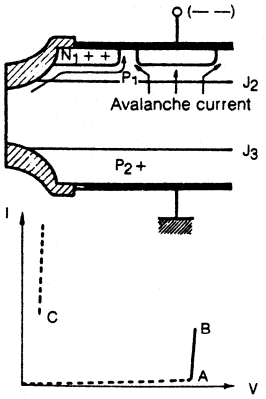


Figure 15 - Operation in the avalanche mode

When the voltage exceeds a certain value, junction J_2, which is reverse biased, begins to operate in the avalanche mode. Because of the profile of the groove associated with the type of passivation, this mechanism operates by priority in the area around the junction.

The structure up to this current level operates like a diode (junction J_2).

The side current biases the P_1 layer next to the N_1 part of the emitter. The highly dopped N_1 layer has the same potential.

The P_1 area coming to the surface is placed at the same potential as the N_1 region by metallization.

The J_1 junction around the groove is biased by the lateral current.

While increasing the avalanche current this difference of potential can reach the threshold of 0.6 V, a value which is sufficient to create injection of electrons from the cathode towards the P_1 area and then trigger thyristor N_1 P_1 N_2 P_2.

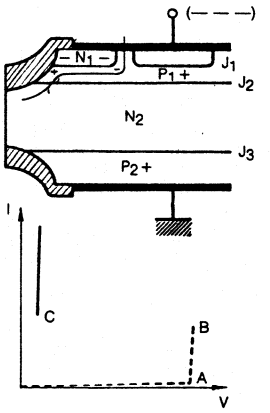


Figure 16 - Thyristor effect of the Trisil

The electrons thus injected into P_1 in fact will reach J_2 by diffusion, and cross it under the effect of the electrical field operating in the space charge of the reverse biased J_2 junction.

In N_2, the electrons help to reduce the potential of this area compared with P_2 and as a result inject holes from P_2 towards N_2. These holes travel in the reverse direction because of their polarity. When they arrive at P_2 they help to increase the potential of P_1 with respect to N_1, this time resulting in the injection of electrons from N_1 to P_1.

The procedure is cumulative. The excess electrons in N_2 and the holes in P_1 will compensate the fixed charges of the space charge and will thus suppress it. Junction J_2 will act as a directly biased junction and the voltage across the component will drop.

IV - APPLICATIONS

IV.1 - APPLICATIONS IN TELEPHONY

The TRISIL was initially developed to meet the problems of protecting new telephone equipment.

Figures 17 and 18 illustrate typical examples of utilization at the switching exchange and subscriber set levels.

In these different configurations, the TRISIL enables the telephone equipment to be in conformity with international CCITT standards, or the national standards derived from them: VDE 0433/3 for Germany and RLM 88 for France.

These examples given by the application laboratory of the Tours plant show the possibilities offered by the TRISIL in solving the problems specific to each.

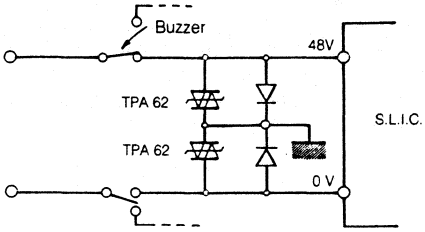


Figure 17 - Protection of the switching exchange SLIC integrated circuit

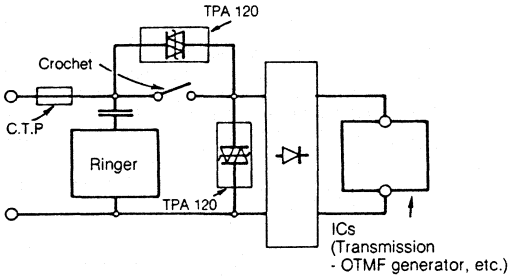


Figure 18 - Protection of subscriber set circuits

IV.2 - DC APPLICATIONS

The TRISIL can also be used outside the field of telephony. If a circuit is powered by a DC supply, it is absolutely necessary to ensure that the **hold current is higher than the maximum current available** (the case of a short-circuit).

Although the TRISIL is normally triggered in both cases, return to normal after the disturbance is not the same.

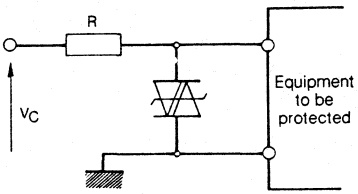
In the case of figure 19, the current does not drop below the hold current. The TRISIL cannot return to the blocked state and thus remains as a quasi short-circuit preventing operation of the equipment to be protected.

In the case of figure 20, the current drops below the value of the hold current and the internal mechanism of the TRISIL enables it to return to the blocked state after the current surge.

Since the TRISIL voltage at the conducting state is low, the condition can be expressed by inequality (4):

$I_H > (V_C/R)$

$$I_H > \frac{V_C}{R} \quad (4)$$



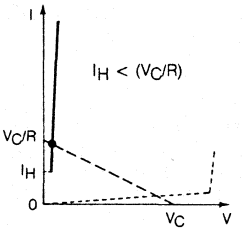


Figure 19 - Wrong choice of the Trisil for DC operation

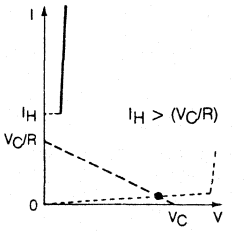


Figure 20 - Right choice of the Trisil DC operation

IV.3 - AC APPLICATIONS

If a circuit is powered by an AC supply, the problem met previously does not arise since the current returns to zero at the end of each half-wave. However, the TRISIL should be rated to withstand the mains current for a half-wave (10 ms), a long period compared with that of the disturbance (Figure 21).

At the occurence of the surge, the TRISIL is normally triggered and begins to conduct, but because of the alternating current, the current flowing through the component does not fall below the hold level (I_H) before the end of the half-wave.

The TRISIL thus has to withstand two currents : the first, of about a hundred amperes for a short period (condition for non destruction : $I_{RS} < I_{PP}$), the second a more moderate current of perhaps ten amperes but for a longer period (condition for non destruction : $V_{rms}\sqrt{2}/R < I_{TSM}$).

The component used should thus be selected as a function of the more stringent condition.

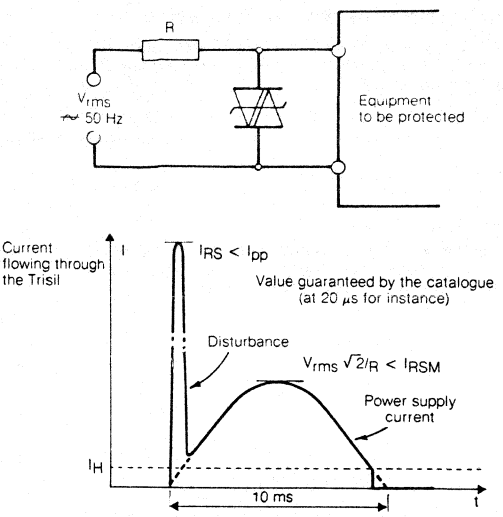


Figure 21 - Operation of a Trisil in an AC circuit

V - RELIABILITY

The TRISIL is manufactured according to two technological processes perfectly mastered by THOMSON SEMICONDUCTEURS and thus benefits from their reliability. This is confirmed by the first results available on this component.

The tests mentioned in this paragraph concern the TPA 120 B series.

V.1 - STORAGE

300°C is the limit temperature for detorioration of the component. It corresponds to the fusion temperature of the PbSn joint between the silicon chip and the aluminium leads. Once they have melted, the hard solder flows over and short-circuits the PN junction(s). **Before this physical parameter is reached, there is no deterioration.**

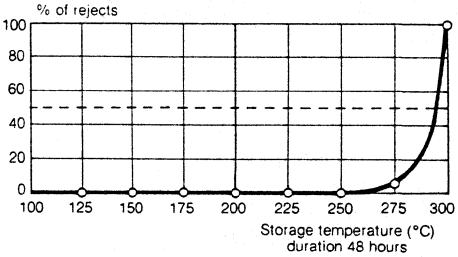


Figure 22 - Results of storage at high temperature

V.2 - BLOCKING

Mastery of the chemical etching, due to the quality of the passivation and a lead glass made by ourselves, give very stable interface qualities. As a result, the TRISIL behaves faultlessly in AC blocking up to at least 200°C.

Parallely, in a long duration test for AC blocking at 117 V for an avalanche voltage of 120 V (TPA 120 B) at a temperature of 125°C no fault has occurred after 15 000 component hours. The test was continued.

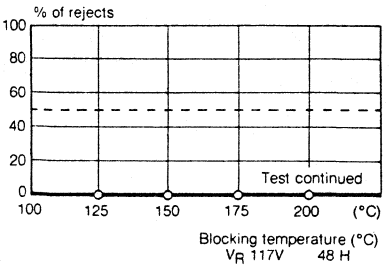


Figure 23 - Results of blocking at high temperature

V.3 - RAPID TEMPERATURE VARIATION

The V_{RTA} test at — 55 + 150°C repeated 100 times and meant to reveal any faults of the glass did not result in any reject. This proves the mastery of the technology acquired over several decades on increasing large batches.

V.4 - DAMP HEAT

The various tests in damp heat, by the absence of faults, show that the passivation (lead glass) and case (organic resin) is leak-proof.

Conditions	Duration of the test	Number of faults
T = 40°C 90 % HR	168 hours	0
	1000 hours	0
T = 85°C 85 % HR	168 hours	0
	1000 hours	0
T = 85°C 85 % HR Biasing at V_{RM}	168 hours	0

Table IV - Results in damp heat

V.5 - REPETITIVE OVERLOADS

Since the overloads to which the component should be subjected are not well defined, it is important for the latter to withstand repeated overloads at the specified current value.

The I_{pp} current guaranteed in the catalogue can be withstood more than 1000 times by the TRISIL. This excellent behaviour is due to the quality of the joints which are put to heavy use in this test.

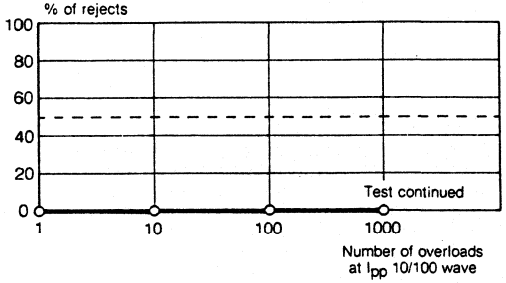


Figure 24 - Results of repetitive overloads

V.6 - CERTIFICATION

The structure with :

- chemical etching
- passivation with lead glass
- soldering with a low-melting-point PbSn joint
- plastic coating

uses a sound technology which perfectly meets the requirements of tests such as storage and blocking at high temperature, rapid temperature variations, damp heat and repetitive overloads.

These good results have **led in France to the certification of the TRISIL by the CNET :**

TPA and TPB are on the LNZ list approved for the PTT department.

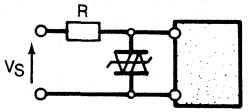
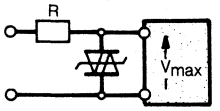
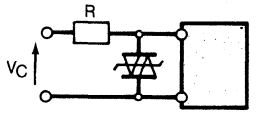
Abroad the TRANSIL has been certified by many suppliers who apply the standards in force in their countries.

VI - CONCLUSIONS

Because of the switching from a blocked state (at rest) to a conducting state with a low voltage drop (transient operation when handling overloads) the TRISIL, a SEMICONDUCTOR component, can be used to protect circuits from high surge currents while avoiding all risks of overvoltage across the circuit being protected.

This booklet enables you to understand the working of such a device and to deduce its applications.

TRISIL CATALOGUE

Operating conditions	Selection of the TRISIL parameter	Corresponding TRISIL reference
 Maximum operating voltage	$V_{RM} > V_S$ where, by definition, $V_{RM} = 0.9\ V_{BR}$ V_{BR} is provide in the TRANSIL reference	TPX V_{BR} X XX
Maximum permitted voltage V_{max} to ensure protection of the equipment 	$V_{BO} < V_{MAX}$ Make sure to consider the influence of the temperature $[V_{BO}]_T = [V_{BO}]_{25°C} [1 + \alpha T\ (T\text{-}25)]$ V_{BO} is indicated by a suffix : A or B $V_{BO} = \frac{V_{BR}}{0.75}$ for index A $V_{BO} = \frac{V_{BR}}{0.82}$ for index B	TPX V_{BR} A XX or TPX V_{BR} B XX
For DC operation 	$I_H > V_C/R$ Caution : the hold current decreases with the temperature The I_H is indicated by the last suffix 12 I_H = 120 mA at 25°C 18 I_H = 180 mA at 25°C	TPX V_{BR} A 12 TPX V_{BR} A 18 TPX V_{BR} B 12 TPX V_{BR} B 18

See the rest of the table for the sturdiness of the component

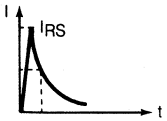
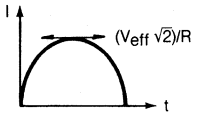
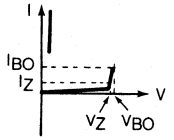
Operating condition	Selection of the TRISIL parameter		Reference suffix TRISIL TPX V_{BR} A or B - 12 or 18			
			A	B	C	D
Capacity to withstand short overloads 	$I_{RS} < I_{PP}$ Standard waves 8/20 µs 10/1000 µs	I_{PP} 8/20 I_{PP} 10/1000	100 A 50 A	150 A 100 A	100 A 50 A	150 A 100 A
Capacity to withstand longer overloads 	$\frac{V_{eff}\sqrt{2}}{R} < I_{TSM}$ In the case of AC at 50 Hz	I_{TSM}	30 A	50 A	30 A	50 A
Maximum dissipation in avalanche operation 	$V_Z I_Z \leqslant P$	P	1.3 W	5 W	20 W	20 W

Table V - Selection of the correct Trisil for a given application

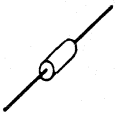
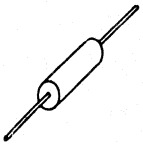
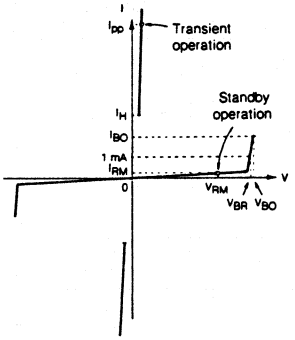
Case	 F 126	 CB 429
Reference	TPA	TPB
Component	Bidirectional TRISIL	Bidirectional TRISIL
Power dissipation on an infinite heat sink Ta = 50°C	1.3 W	5 W
Thermal resistance on an infinite heat sink (L = 10 mm)	75°C/W	20°C/W
Peak current (I_{pp}) 8/20 wave	100 A	150 A
Peak current (I_{pp}) 10/1000 wave	50 A	100 A
Non-repetitive surge current (I_{TSM}) t = 20 ms	30 A	50 A
Avalanche voltage (V_{BR})	62 V at 270 V	62 V at 270 V
Break-over voltage (V_{BO})	Series at 121 or 133 % of V_{BR}	Series at 121 or 133 % of V_{BR}
Hold-current (I_H)	120 mA or 180 mA min.	120 mA or 180 mA min.
Capacitance at 1 V (C)	Typ. 90 pF	Typ. 150 pF

Table VI - Selection guide

TRISIL TP TELEPHONE PROTECTION

- **Bidirectional** device used to **telephone protection.**
- Characteristic of stand-off and breakdown voltage similar to a Transil (V_{off}).
- High flowout capability because of its breakover characteristic (V_{on}).

Current-voltage characteristic



Bidirectional types	I_{RM} @ V_{RM}		$V_{(BR)}$ min @ I_R		$V_{(BO)}$ max	$I_{(BO)}$ max	I_H	Case
	(μA)	(V)	(V)	(mA)	(V)	(mA)	(mA)	
I_{pp} = 100 A (8-20 μs expo.)								
TPA 62A - 12 or 18	2	56	62	1	82	300		
TPA 62B - 12 or 18	2	56	62	1	75	300		
TPA 68A - 12 or 18	2	61	68	1	90	300		
TPA 68B - 12 or 18	2	61	68	1	82	300		
TPA 75A - 12 or 18	2	67	75	1	100	300		
TPA 75B - 12 or 18	2	67	75	1	91	300		
TPA 82A - 12 or 18	2	74	82	1	109	300		
TPA 82B - 12 or 18	2	74	82	1	99	300		
TPA 91A - 12 or 18	2	82	91	1	121	300		
TPA 91B - 12 or 18	2	82	91	1	110	300		
P TPA 100A- 12 or 18	2	90	100	1	133	300		
TPA 100B- 12 or 18	2	90	100	1	121	300		
TPA 110A- 12 or 18	2	99	110	1	147	300		
TPA 110B- 12 or 18	2	99	110	1	133	300	12 suffix for 120 mA	
P TPA 120A- 12 or 18	2	108	120	1	160	300		
TPA 120B- 12 or 18	2	108	120	1	145	300		
P TPA 130A- 12 or 18	2	117	130	1	173	300		F 126 plastic (CB-210)
TPA 130B- 12 or 18	2	117	130	1	157	300		
TPA 150A- 12 or 18	2	135	150	1	200	300	18 suffix for 180 mA	
TPA 150B- 12 or 18	2	135	150	1	181	300		
TPA 160A- 12 or 18	2	144	160	1	213	300		
TPA 160B- 12 or 18	2	144	160	1	193	300		
TPA 180A- 12 or 18	2	162	180	1	240	300		
TPA 180B- 12 or 18	2	162	180	1	217	300		
P TPA 200A- 12 or 18	2	180	200	1	267	300		
TPA 200B- 12 or 18	2	180	200	1	241	300		
P TPA 220A- 12 or 18	2	198	220	1	293	300		
TPA 220B- 12 or 18	2	198	220	1	265	300		
P TPA 240A- 12 or 18	2	216	240	1	320	300		
TPA 240B- 12 or 18	2	216	240	1	289	300		
P TPA 270A- 12 or 18	2	243	270	1	360	300		
TPA 270B- 12 or 18	2	243	270	1	325	300		

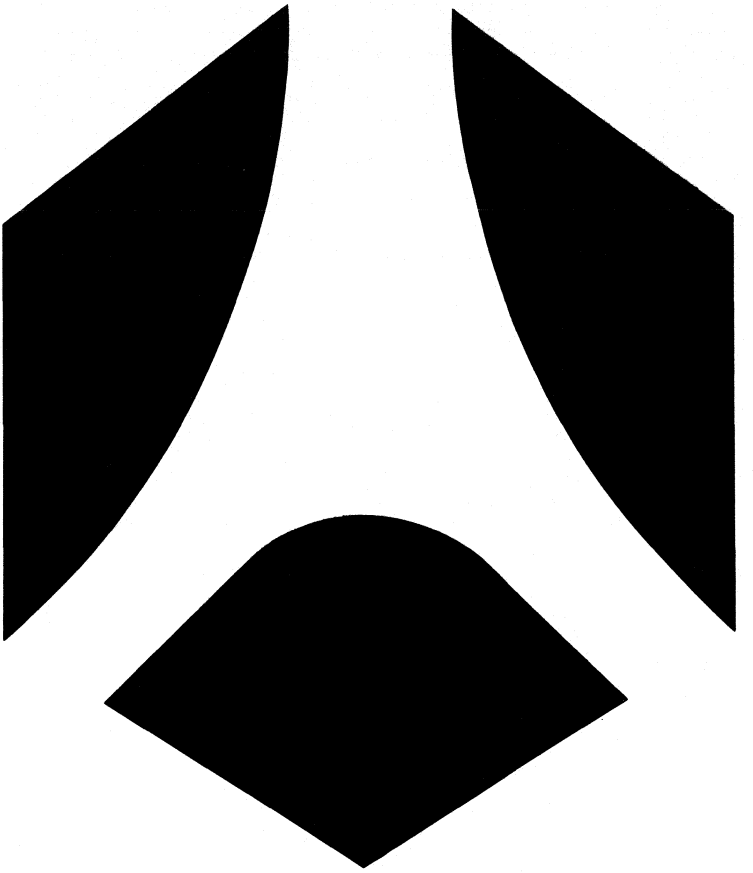
P-: Preferred device.

TRISIL TP TELEPHONE PROTECTION

Bidirectional types	I_{RM} @ V_{RM}		$V_{(BR)}$ min @ I_R		$V_{(BO)}$ max	$I_{(BO)}$ max	I_H	Case
	(μA)	(V)	(V)	(mA)	(V)	(mA)	(mA)	
I_{pp} = 150 A (8-20 μs expo.)								
TPB 62A - 12 or 18	2	56	62	1	82	300		
TPB 62B - 12 or 18	2	56	62	1	75	300		
TPB 68A - 12 or 18	2	61	68	1	90	300		
TPB 68B - 12 or 18	2	61	68	1	82	300		
TPB 75A - 12 or 18	2	67	75	1	100	300		
TPB 75B - 12 or 18	2	67	75	1	91	300		
TPB 82A - 12 or 18	2	74	82	1	109	300		
TPB 82B - 12 or 18	2	74	82	1	99	300		
TPB 91A - 12 or 18	2	82	91	1	121	300		
TPB 91B - 12 or 18	2	82	91	1	110	300		
TPB 100A- 12 or 18	2	90	100	1	133	300		
TPB 100B - 12 or 18	2	90	100	1	121	300		
TPB 110A- 12 or 18	2	99	110	1	147	300		
TPB 110B - 12 or 18	2	99	110	1	133	300		
P TPB 120A- 12 or 18	2	108	120	1	160	300	12 suffix for 120 mA	
TPB 120B - 12 or 18	2	108	120	1	145	300		
P TPB 130A- 12 or 18	2	117	130	1	173	300		
TPB 130B - 12 or 18	2	117	130	1	157	300		
TPB 150A- 12 or 18	2	135	150	1	200	300	18 suffix for 180 mA	
TPB 150B - 12 or 18	2	135	150	1	181	300		
TPB 160A- 12 or 18	2	144	160	1	213	300		
TPB 160B - 12 or 18	2	144	160	1	193	300		
TPB 180A- 12 or 18	2	162	180	1	240	300		
TPB 180B - 12 or 18	2	162	180	1	217	300		
P TPB 200A- 12 or 18	2	180	200	1	267	300		
TPB 200B - 12 or 18	2	180	200	1	241	300		
P TPB 220A- 12 or 18	2	198	220	1	293	300		
TPB 220B - 12 or 18	2	198	220	1	265	300		
TPB 240A- 12 or 18	2	216	240	1	320	300		
TPB 240B - 12 or 18	2	216	240	1	289	300		
TPB 270A- 12 or 18	2	243	270	1	360	300		
TPB 270B - 12 or 18	2	243	270	1	325	300		

CB-429 plastic

P : Preferred device.



Microcomputers - Microprocessors - Peripherals & Memories

4 BITS: ET9400 FAMILY

PART Nber	TECHNOLOGY	ROM x 8	RAM x 4	INSTRUCTION CYCLE (µs)	SUPPLY (V)	ALT. SOURCE	Nb PINS
ETL 9410/11/13	NMOS Low Power	512	32	15-40	4.5-6.3	COP410L/11L/13L	24/20
ETC 9410/11/13	CMOS	512	32	4-DC	2.4-5.5	COP410C/11C/13C	24/20
ET 9420/21/22	NMOS	1024	64	4-10	4.5-6.3	COP420/21/22	28/24/20
ETL 9420/21/22	NMOS Low Power	1024	64	15-40	4.5-6.3	COP420L/21L/22L	28/24/20
ETC 9420/21/22	CMOS	1024	64	4-DC	2.4-5.5	COP424C/25C/26C	28/24/20
ETL 9444/45	NMOS Low Power	2048	128	15-40	4.5-6.3	COP444L/45L	28/24
ETC 9444/45	CMOS	2048	128	4-DC	2.4-5.5	COP444C/45C	28/24
TS 941120/44	NMOS	512 to 2048	32 to 128	4-15	4.5-5.5.	—	24/28
TS 94104	NMOS	ROMLESS	128	4-15	4.5-5.5	—	64

Common features : software compatible (same instruction set). Pin compatible. Three levels of stack. 8 bidirectional tristate I/O. Serial I/O and internal counter, interrupt programmable I/O. All devices are with plastic package (DIL) and also available with extended temperature range (– 40°C to + 85°C) : ET 93XX or ETC 93XX.

8 BITS: EF6801 FAMILY

PART Nber	TECHNOLOGY	ROM x 8	RAM x 8	I/O	FEATURES	ALT. SOURCE	Nb PINS
EF6801	HMOS	2048	128	31	SCI, Timer, stand-by RAM	MC6801 HD6801-S0	40
EF6801-U4	HMOS	4096	192	31	Enhanced SCI and Timer Stand-by RAM	MC6801-U4 HD6801-V0	40
EF68HC11A8*	HCMOS	4096	256		SCI-SPI-EEPROM ADC-Enhanced Timer Real Time Inter. Watchdog	MC68HC11A8	48/52

Common features: 8 x 8 multiply instruction. Timer. 64K byte addressing space. Serial communication interface. All devices available in DIL ceramic or plastic package and plastic chip carrier (PLCC)/ – 40 °C to + 85 °C).

8 BITS: EF6804 FAMILY

PART Nber	TECHNOLOGY	ROM x 8	RAM x 8	I/O	ALT. SOURCE	Nb PINS
EF 6804P2	HMOS	1024	32	20	MC 6804 P2	28
EF 6804J2	HMOS	1024	32	12	MC 6804 J2	20
EF 68HC04J3*	HCMOS	2048	124	12	—	20
EF 68HC04P3	HCMOS	2048	124	20	MC 68HC04 P3	28

Available in plastic, ceramic, DIL packages or chip-carriers. All software compatible. Timer.

8 BITS: EF6805 FAMILY

PART Nber	TECHNOLOGY	ROM x 8	RAM x 8	I/O	FEATURES	ALT. SOURCE	Nb PINS
EF 6805P2	HMOS	1100	64	20	—	MC 6805P2- HD 6805S1	28
EF 6805P6	HMOS	1796	64	20	—	MC 6805P6	28
EF 6805R2	HMOS	2048	64	32	A/D Converter	MC 6805R2	40
EF 6805R3	HMOS	3776	112	32	A/D Converter	MC 6805R3- HD 6805W0	40
EF 6805U2	HMOS	2048	64	32	—	MC 6805U2	40
EF 6805U3	HMOS	3776	112	32	—	MC 6805U3	40

Available in plastic, ceramic, DIL packages or chip-carrier. Ext. temp range (– 40°C, + 85°C). All software compatible. Interrupt capabilities. Timer.

* To be introduced.

8 BITS: MK3870 FAMILY

PART Nber	TECHNOLOGY	ROM × 8	RAM × 8	I/O	FEATURES	ALT. SOURCE	Nb PINS
MK2870/10	NMOS	1024	64	20	—	M2872	28
MK3870/10	NMOS	1024	64	32	—	M3872	40
MK3870/20	NMOS	2048	64	32	—	M3870.2	40
MK3870/22	NMOS	2048	128	32	—	M3872	40
MK3870/40	NMOS	4096	64	32	—	M3872	40
MK3870/42	NMOS	4032	128	32	—	M3872	40
MK3873/22	NMOS	2048	128	29	SI, SO, SLCK	M38730,33	40
MK3875/22	NMOS	2048	128	29	SI, SO, SLCK	M3875	40
MK3875/42	NMOS	4032	128	29	SI, SO, SLCK	M3875	40

Common features: Software compatible (same instruction set), timer, interrupt capabilities, parallel I/O (TTL compatible).
All devices are with plastic or ceramic package (DIL). PLCC package to be introduced mid 1986.
Also available with extended temperature range.

16 BITS: MK68200 FAMILY

PART Nber	TECHNOLOGY	SPEED MHz	ROM × 8	RAM × 8	I/O	FEATURES	ALT. SOURCE	Nb PINS
MK68201/04-4	NMOS	4	0	256		68000 BUS	—	48
MK68201/04-6		6				ROMLESS		
MK68201/44-4	NMOS	4	4096	256		68000 BUS	—	48
MK68201/44-6		6				Masked Version		
MK68E201/04-4	NMOS	4	0	256		68000 BUS ROMLESS	—	84
MK68E201/04-6		6				and Private BUS		
MK68211/04-4	NMOS	4	0	256		General Purpose BUS	—	48
MK68211/04-6		6				ROMLESS		
MK68211/44-4	NMOS	4	4096	256		General Purpose BUS	—	48
MK68211/44-6		6				Masked Version		
MK68E211/04-4	NMOS	4	0	256		General Purpose BUS	—	84
MK68E211/04-6		6				Romless and Private BUS		
MK68HC200*	HCMOS	8	4096	256		HCMOS version of 68200 Family	—	48

Packaging: DIL 48 Plastic and Ceramic, PLCC 84, Ceramic LCC 84

STANDARD: MK3870 (97xxx) FAMILY

PART Nber	TECHNOLOGY	ADDRESSABLE ROM × 8	ON CHIP RAM × 8	I/O	FEATURES	SUPPORT	Nb PINS
MK97400	NMOS	4096	128	32	TTL Ports	4K EPROM	40 (24/28)
MK97403	NMOS	4096	128	32	TTL Ports	4K EPROM	40 (24/28)
MK97410	NMOS	4096	128	32	Open drain ports	4K EPROM	40 (24/28)
MK97501	NMOS	65472	128	32	TTL ports	8K EPROM	40 (28)
MK97521	NMOS	65472	128	32	Open drain and TTL ports	8K EPROM	40 (28)

Common features: EPROM version of MK3870, piggyback ceramic package accepts 24 or 28 pins memories, pin to pin compatible with 3870.

HIGH SPEED DATA CONVERSION

PART Nber	FUNCTION	SAMPLING RATE	SUPPLY	Nb PINS
TS 8306	6-bit flash ADC	15 MHz	+5 V	16
TS 8307	7-bit flash ADC	15 MHz	+5 V	20
TS 8308	8-bit flash ADC	15 MHz	+5 V	24
TS 8328	8-bit flash ADC (min. version of TS 8308)	15 MHz	+5 V	20
UA 1005	4-bit flash ADC	30 MHz	+5 V	24
TS 8408	8-bit voltage output DAC	25 MHz	+5 V	16
TS 8428	8-bit voltage output DAC	25 MHz	+5 V	16

* To be introduced

THOMSON COMPONENTS SEMICONDUCTEURS

TS68HC04F

8-BIT MICROCOMPUTERS

PRODUCT PREVIEW

HCMOS

The TS68HC04 F microcontroller is a member of the TS68HC04 family of very low cost and low power single chip microcontrollers. The TS68HC04F3 microcontroller is dedicated to telephone application. It includes the 68HC04 CPU, on-chip clock, ROM, RAM, I/O, timer, melody generator and DTMF.

HARDWARE FEATURES

- 8-bit architecture
- Single 2.0 to 5.5 volts power supply
- Low power HCMOS (run CPU only : 0.5 mA max/3.5 volts/1 MHz)
  (run CPU + DTMF : 2 mA max/3.5 volts/1 MHz)
  (STOP mode : 0.5 uA)
- Extensive self check capability allowing complete functional test of the chip including ROM content.
- 3.7 K Bytes of user ROM
- 192 Bytes data RAM
- 64 Bytes data ROM
- 23 I/O (28 pins PLCC package)
- 36 I/O (44 pins PLCC package)
- DTMF synthetisor (similar to TS7189)
- Melody generator with 160 Bytes data ROM
- 8 bit timer with 7 bit prescaler
- V_{CC} standby supply pin
- Serial shift regiter output

SOFTWARE FEATURES

- Similar to 6800 family
- Bit efficient instruction set
- Easy to program
- True bit manipulation
- Stop, wait and bit manipulation instructions
- Bit test and branch instructions
- Versatile interrupt handling
- Separate flags for normal and interrupt processing
- True LIFO 4 levels stack eliminatig stack pointer
- Maskable timer interrupt
- Versatile indirect registers
- Conditional branches
- 9 powerfull adressing modes

CASE

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Ref.:DSTS68HC04F

Printed in France

PRODUCT PREVIEW

HCMOS

The TS68HC04 D1/D2/D3 HCMOS microcontrollers belong to the TS68HC04 family. The TS68HC04 family microcontrollers include on the same chip the enhaust 68HC04 CPU and peripherals chosen in the TS68HC04 library standard cells.

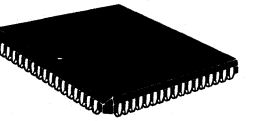
The peripherals of the TS68HC04 D1/D2/D3 products are: a LCD controller, a 8-bit timer and a 8-bit input/output shift register. Thanks to these peripherals, the TS68HC04 D family is well swited for applications like: scales, microwaves oven, telephon set, dask board, ect... Besides the TS68HC04 D1/D2/D3 microcontrollers includes also special devices and I/O's such as: power supply supervisa, digital watchlog, 2 high currents outputs, a zero-crossing detector and a triggered input for the timer. Thanks to these devices, the TS68HC04 D1/D2/D3 allow an important external components savings and improve the realibility of the application.

HARDWARE FEATURES

- CPU
  - 8-bit architecture
  - Low power HCMOS
  - Single 2.0 to 6.0 volt power supply
  - Fully static operation, stop and wait modes
- Memories
  - 1K/2K/3,5K Bytes of ROM
  - 48/96/124 Bytes of data RAM
  - 120/480/960 Bytes of data ROM
- I/O's
  - 12/16/28 TTL/CMOS compatible bidirectional I/O's including 2 high current option outputs
  - 8 of these I/O's (port A) can be configured by Mask Option as LCD segments (SEG25/SEG32)
  - 16/20/24 LCD segments outputs
  - 4 commons pins (direct drive, bi/tri/quadriplex)
  - 1 external IRQ pin
  - 1 external Timer pin
- Peripherical
  - LCD controller with DMA to the RAM
  - 8-bit timer with a 7-bit software programmable prescaler
  - 8-bit input/output shift register (SIO)
- Devices
  - Power supply supervisor
  - Digital watchdog
  - Master reset
  - On-chip clock generator

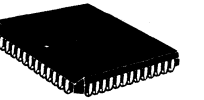
CASES

TS68HC04D3



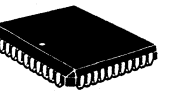
PLCC

TS68HC04D2



PLCC

TS68HC04D1



PLCC

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SOFTWARE FEATURES

- Similar to EF6800 family
- Easy to program
- Byte efficient instruction set
- Bit test and Branch instruction
- Stop, wait and bit manipulation instruction
- True LIFO 4 level stack
- 9 powerfull addressing modes
- The accumulator, the X and Y registers are mapped in the RAM
- All the data and control registers of peripherals are mapped in the RAM

DEVELOPMENT TOOLS

- The development tool of the TS68HC04D family consists in the INICE 4-8 and the cumulator probe TSTMUP4D, connected on a IBM PC.
- TS68HC704D eprom version is available.

Printed in France

Ref.DSTS68HC04DFAMILY

4 BITS: 2900 FAMILY

PART Nber	FUNCTION	ALT. SOURCE	Nb PINS
TS 2901B TS 2901C	4-bit bipolar microprocessor slice Improved speed 4 Bit microprocessor slice	Am2901B Am2901C	40 40
TS 2902A	High speed look-ahead carry generator	Am2902A	16
TS 2909A	Microprogram sequencer	Am2909A	28
TS 2910	Microprogram controller	Am2910	40
TS 2911A	Microprogram sequencer	Am2911A	20
TS 2914	Vectored priority interrupt controller	Am2914	40
TS 2915A	Quad 3-State Bus Transceiver with interface logic	Am2915 A	24
TS 2917A	Quad 3-State Bus Transceiver with interface logic	Am 2917A	20
TS 2918	Quad D register with standard and 3-State Outputs	Am2918	16
TS 2919	Quad D register with Dual 3-State Outputs	Am 2919	20

8 BITS: 6800 FAMILY

PART Nber	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	Nb PINS
EF 6800 EF 68A00 EF 68B00	NMOS	1 1.5 2	8-bit microprocessor. 16-bit addresses. 72 instructions	MC 6800 MC 68A00 MC 68B00	40
EF 6802 EF 68A02 EF 68B02	NMOS	1 1.5 2	6800 MPU. 128 bytes of RAM. On-chip oscillator	MC 6802 MC 68A02 MC 68B02	40
EF 6803 EF 68A03 EF 68B03	HMOS	1 1.5 2	8-bit microp., 16-bit add. bus. Multiply. RAM: 128b. SCI-Timer	MC 6803 MC 68A03 MC 68B03	40
TS 6303R* TS 63A03R* TS 63B03R*	HCMOS	1 1.5 2	8-bit CMOS microprocessor. 16-bit add. bus. multiply. RAM: 128b. SCI. timer. compatible with EF 6803	HD 6303R	40
EF 6803U4 EF 68A03U4 EF 68B03U4	HMOS	1 1.5 2	Same as above but RAM: 192b. enhanced timer	MC 6803U4 MC 68A03U4 MC 68B03U4	40
EF 68HC05E2*	HCMOS		8-bit microprocessor. 16-bit addresses	MC 146805E2	40
EF 6808 EF 68A08 EF 68B08	NMOS	1 1.5 2	6800 MPU. on chip oscillator	MC 6808 MC 68A08 MC 68B08	40
EF 6809 EF 68A09 EF 68B09	HMOS	1 1.5 2	High performance 8-bit MPU. 6800 compatible. On-chip oscillator	MC 6809 MC 68A09 MC 68B09	40
EF 6809E EF 68A09E EF 68B09E	HMOS	1 1.5 2	High performance 8-bit MPU. 6800 compatible. External clock	MC 6809E MC 68A09E MC 68B09E	40
TS 68008-8 TS 68008-10 TS 68008-12	HMOS	8 10 12.5	16-bit microprocessor with 8-bit data bus	MC 68008-8 MC 68008-10 MC 68008-12	48

Available in plastic, ceramic, cerdip DIL packages and plastic or ceramic chip-carriers.

8 BITS: MK3880 (Z80™) FAMILY

PART Nber	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	Nb PINS
MK3880-00 MK3880-04 MK3880B-06	NMOS	2 4 6	Z80 Central Processing Unit	Z8400 Z8400A Z8400B	40
MK3831 MK3835	CMOS	4.19	MCU - Real Time Clock/RAM MCU - Real Time Clock	—	8

* To be introduced

16 BITS: 68000 FAMILY

PART Nber	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	Nb PINS
TS68000-8		8		MC68000-8	
TS68000-10	HMOS	10	16-bit microprocessor	MC68000-10	64
TS68000-12		12.5	with 32-bit internal structure	MC68000-12	
TS68000-16		16		—	
TS68008-8		8		MC68008-8	
TS68008-10	HMOS	10	TS68000 8-bit bus version	MC68008-10	48
TS68008-12		12.5		MC68008-12	

Also available in ceramic DIL packages, pin-grid arrays and ceramic or plastic chip-carrier.

8 BITS: 6800 FAMILY

PART Nber	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	Nb PINS
EF6821 EF68A21 EF68B21	NMOS	1 1.5 2	Peripheral Interface Adapter (PIA)	MC6821 MC68A21 MC68B21	40
EF6840 EF68A40 EF68B40	NMOS	1 1.5 2	Programmable Timer Module (PTM)	MC6840 MC68A40 MC68B40	28
EF6850 EF68A50 EF68B50	NMOS	1 1.5 2	Asynchronous Communication Interface Adapter (ACIA)	MC6850 MC68A50 MC68B50	24
EF6852 EF68A52 EF68B52	NMOS	1 1.5 2	Synchronous Serial Data Adapter (SSDA)	MC6852 MC68A52 MC68B52	24
EF6854 EF68A54 EF68B54	NMOS	1 1.5 2	Advanced Data-Link Controller (ADLC)	MC6854 MC68A54 MC68B54	28
EF6810 EF68A10 EF68B10	NMOS	1 1.5 2	12 × 8 S-RAM	MC6810 MC68A10 MC68B10	24
EF9345	HMOS		Single chip alphanumeric and semigraphic display processor 25/21 rows of 40 or 80 char. Multipage memory. Color and B/W		40
EF9367	HMOS		Graphic display coprocessor. Up to 512 × 1024 Interlaced 50/60 Hz-Color and B/W		40

Available in plastic, ceramic and cerdip DIL packages as well as plastic and ceramic chip-carriers.

8 BITS: MK3880 (Z80) FAMILY

PART Nber	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	Nb PINS
MK3881-00 MK3881-04	NMOS	2.5 4	Parallel Input/Output Controller (PIO)	Z8420 Z8420A	40
MK3882-00 MK3882-04	NMOS	2.5 4	Counter timer circuit (CTC)	Z8430 Z8430A	28
MK3883-00 MK3883-04	NMOS	2.5 4	Direct Memory Access (DMA)	Z8410 Z8410A	40
MK3884-00 MK3884-04	NMOS	2.5 4	Async/Sync Serial Input/Output	Z8440 Z8440A	40
MK3885-00 MK3885-04	NMOS	2.5 4	SIO-1 Channel Sync/Async	Z8441 Z8441A	40
MK3887-00 MK3887-04	NMOS	2.5 4	SIO-2 Channel Sync/Async	Z8442 Z8442A	40
MK3801-00 MK3801-04 MK3801-06	NMOS	2.5 4 6	Serial Timer Interrupt (STI)	— — —	40

Available with plastic (N) or ceramic (P) dual in-line package

16 BITS: 68000 FAMILY

PART Nber	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	Nb PINS
MK68230-8 MK68230-10	HMOS	8 10	Parallel interface/timer	MC68230-8 MC68230-10	48
TS68483	HMOS	15	High performance graphic processor	MK68483	64
MK68564	HMOS	3-4-5	Serial I/O	MK68564	48
TS68HC901*	HCMOS	4	CMOS multifunction peripheral		48
MK68901	HMOS	4, 5	Multifunction peripheral	MK68901	48
TS68930*	HMOS2	6.25	High performance digital signal processor with internal program ROM 160 μs cycle time, 2 × 128 × 16-bit internal RAM	—	48
TS68931*	HMOS2	6.25	ROMLESS version of TS68930 64K addressing range	—	84
MK68451-8 MK68451-10 MK68451-12*	NMOS	8 10 12.5	Memory management unit	MC68451-8 MC68451-10 MC68451-12	64

Available in plastic, ceramic DIL package and plastic or ceramic chip-carrier.
* To be introduced

ZEROPOWER™ AND TIMEKEEPER™

PART Nber	DESCRIPTION	ORGANIZATION	ACCESS TIME	I_{CC}	I_{SB}	TEMPERATURE RANGE	Nb PINS
MK48T02(B)-12*	TIMEKEEPER SRAM	2K × 8	120 ns	80 mA	3 mA	C	24
MK48T02(B)-15*	TIMEKEEPER SRAM	2K × 8	150 ns	80 mA	3 mA	C	24
MK48T02(B)-20*	TIMEKEEPER SRAM	2K × 8	200 ns	80 mA	3 mA	C	24
MK48T02(B)-25*	TIMEKEEPER SRAM	2K × 8	250 ns	80 mA	3 mA	C	24
MK48Z02(B)-15	ZEROPOWER SRAM	2K × 8	150 ns	80 mA	1 mA	C	24
MK48Z02(B)-20	ZEROPOWER SRAM	2K × 8	200 ns	80 mA	1 mA	C	24
MK48Z02(B)-25	ZEROPOWER SRAM	2K × 8	250 ns	80 mA	1 mA	C	24

BATTERY BACK-UP RAMs

PART Nber	DESCRIPTION	ORGANIZATION	ACCESS TIME	I_{CC}	I_{BAT}	TEMPERATURE RANGE	Nb PINS
MK48C02(N)-15	Bat. Back-up SRAM	2K × 8	150 ns	80 mA	50 µA	C	28
MK48C02(N)-20	Bat. Back-up SRAM	2K × 8	200 ns	80 mA	50 µA	C	28
MK48C02(N)-25	Bat. Back-up SRAM	2K × 8	250 ns	80 mA	50 µA	C	28
MK48C02L(N)-15	Bat. Back-up SRAM	2K × 8	150 ns	80 mA	1 µA	C	28
MK48C02L(N)-20	Bat. Back-up SRAM	2K × 8	200 ns	80 mA	1 µA	C	28
MK48C02L(N)-25	Bat. Back-up SRAM	2K × 8	250 ns	80 mA	1 µA	C	28

BIPORT™ DEVICES

PART Nber	DESCRIPTION	ORGANIZATION	ACCESS TIME	CYCLE	I_{CC}	TEMPERATURE RANGE	Nb PINS
MK4501(N)-80	BiPORT FIFO	512 × 9	80 ns	100 ns	80 mA	C	28
MK4501(N)-10	BiPORT FIFO	512 × 9	100 ns	120 ns	80 mA	C	28
MK4501(N)-12	BiPORT FIFO	512 × 9	120 ns	140 ns	80 mA	C	28
MK4501(N)-15	BiPORT FIFO	512 × 9	150 ns	175 ns	80 mA	C	28
MK4501(N)-20	BiPORT FIFO	512 × 9	200 ns	235 ns	80 mA	C	28
MK4501(E)-80	BiPORT FIFO	512 × 9	80 ns	100 ns	80 mA	C	32
MK4501(E)-10	BiPORT FIFO	512 × 9	100 ns	120 ns	80 mA	C	32
MK4501(E)-12	BiPORT FIFO	512 × 9	120 ns	140 ns	80 mA	C	32
MK4501(E)-15	BiPORT FIFO	512 × 9	150 ns	175 ns	80 mA	C	32
MK4501(E)-20	BiPORT FIFO	512 × 9	200 ns	235 ns	80 mA	C	32
MK4501(K)-80*	BiPORT FIFO	512 × 9	80 ns	100 ns	80 mA	C	32
MK4501(K)-10*	BiPORT FIFO	512 × 9	100 ns	120 ns	80 mA	C	32
MK4501(K)-12*	BiPORT FIFO	512 × 9	120 ns	140 ns	80 mA	C	32
MK4501(K)-15*	BiPORT FIFO	512 × 9	150 ns	175 ns	80 mA	C	32
MK4501(K)-20*	BiPORT FIFO	512 × 9	200 ns	235 ns	80 mA	C	32
MK4511(N)-12	BiPORT RAM	512 × 9	120 ns	150 ns	50 mA	C	28
MK4511(N)-15	BiPORT RAM	512 × 9	150 ns	190 ns	50 mA	C	28
MK4511(N)-20	BiPORT RAM	512 × 9	200 ns	250 ns	50 mA	C	28
MK4511(K)-12*	BiPORT RAM	512 × 9	120 ns	150 ns	50 mA	C	32
MK4511(K)-15*	BiPORT RAM	512 × 9	150 ns	190 ns	50 mA	C	32
MK4511(K)-20*	BiPORT RAM	512 × 9	200 ns	250 ns	50 mA	C	32

* To be introduced

Temperature range C = 0 C to +70 C

STATIC RAMs

PART Nber	DESCRIPTION	ORG.	ACCESS TIME	I_{CC}	I_{SB}	TEMP. RANGE	PKG.	Nb PINS
MK4801A(x)-55	Fast SRAM	1K × 8	55 ns	110 mA	—	C	N, P, J	24
MK4801A(x)-70	Fast SRAM	1K × 8	70 ns	110 mA	—	C	N, P, J	24
MK4801A(x)-90	Fast SRAM	1K × 8	90 ns	110 mA	—	C	N, P, J	24
MK4801A(x)-1	Fast SRAM	1K × 8	120 ns	110 mA	—	C	N, P, J	24
MK4801A(x)-2	Fast SRAM	1K × 8	150 ns	110 mA	—	C	N, P, J	24
MK4801A(x)-3	Fast SRAM	1K × 8	200 ns	110 mA	—	C	N, P, J	24
MK4801A(x)-4	Fast SRAM	1K × 8	250 ns	110 mA	—	C	N, P, J	24
NOTE: (x) = Package Type P, J, or N								
MK6116(N)-15	CMOS SRAM	2K × 8	150 ns	70 mA	2 mA	C	N	24
MK6116(N)-20	CMOS SRAM	2K × 8	200 ns	70 mA	2 mA	C	N	24
MK6116(N)-25	CMOS SRAM	2K × 8	250 ns	70 mA	2 mA	C	N	24
MK6116L(N)-15	CMOS SRAM	2K × 8	150 ns	60 mA	100 µA	C	N	24
MK6116L(N)-20	CMOS SRAM	2K × 8	200 ns	60 mA	100 µA	C	N	24
MK6116L(N)-25	CMOS SRAM	2K × 8	250 ns	60 mA	100 µA	C	N	24
ET2147HJ-3	Fast SRAM	4K × 1	55 ns	180 mA	30 mA	C, V, M	J	18
ET2147HJ-2	Fast SRAM	4K × 1	45 ns	180 mA	30 mA	C, V, M	J	18
ET2147HJ-1	Fast SRAM	4K × 1	35 ns	180 mA	30 mA	C	J	18
ETL2147HJ	Fast SRAM	4K × 1	70 ns	140 mA	15 mA	C	J	18
ETL2147HJ-3	Fast SRAM	4K × 1	55 ns	140 mA	15 mA	C	J	18
ETL2128N-4	NMOS SRAM	2K × 8	200 ns	70 mA	10 mA	C, V, M	N	24
ETL2128N-3	NMOS SRAM	2K × 8	150 ns	70 mA	10 mA	C, V, M	N	24

VERY FAST STATIC RAMs

PART Nber	KEY FEATURES	ORG.	ACCESS TIME	V_{CC}	I_{CC}	I_{SB}	TEMP. RANGE	PKG.	Nb PINS
MK41H66(x)-xx*	Fast $\overline{CS}$ Access	16K × 1	20, 25, 35 ns	5.0V	110 mA	—	C	N, P, E	20
MK41H67(x)-xx*	$\overline{CE}$ Power-down	16K × 1	20, 25, 35 ns	5.0V	110 mA	50 µA	C	N, P, E	20
MK41H68(x)-xx*	$\overline{CE}$ Power-down	4K × 4	20, 25, 35 ns	5.0V	110 mA	50 µA	C	N, P, E	20
MK41H69(x)-xx*	Fast $\overline{CS}$ Access	4K × 4	20, 25, 35 ns	5.0V	110 mA	—	C	N, P, E	20
MK41H77(x)-xx*	$\overline{CE}$/$\overline{OE}$ & Flash Clr	16K × 1	20, 25, 35 ns	5.0V	110 mA	50 µA	C	N, P, E	22
MK41H78(x)-xx*	$\overline{CE}$/$\overline{OE}$	4K × 4	20, 25, 35 ns	5.0V	110 mA	50 µA	C	N, P, E	22
MK41H79(x)-xx*	$\overline{CE}$/$\overline{OE}$ & Flash Clr	4K × 4	20, 25, 35 ns	5.0V	110 mA	50 µA	C	N, P, E	22
MK41L66(x)-xx*	Fast $\overline{CS}$ Access	16K × 1	25, 35 ns	3.3V	55 mA	—	C	N, P, E	20
MK41L67(x)-xx*	$\overline{CE}$ Power-down	16K × 1	25, 35 ns	3.3V	55 mA	50 µA	C	N, P, E	20
MK41L68(x)-xx*	$\overline{CE}$ Power-down	4K × 4	25, 35 ns	3.3V	55 mA	50 µA	C	N, P, E	20
MK41L69(x)-xx*	Fast $\overline{CS}$ Access	4K × 4	25, 35 ns	3.3V	55 mA	—	C	N, P, E	20
MK41L77(x)-xx*	$\overline{CE}$/$\overline{OE}$ & Flash Clr	16K × 1	25, 35 ns	3.3V	55 mA	50 µA	C	N, P, E	22
MK41L78(x)-xx*	$\overline{CE}$/$\overline{OE}$	4K × 4	25, 35 ns	3.3V	55 mA	50 µA	C	N, P, E	22
MK41L79(x)-xx*	$\overline{CE}$/$\overline{OE}$ & Flash Clr	4K × 4	25, 35 ns	3.3V	55 mA	50 µA	C	N, P, E	22

* To be introduced

NOTE: (x) = Package Type N, P, or E
-xx = -20, -25, -35 for 20 ns, 25 ns, 35 ns Access Times

NMOS EPROMs

PART Nber	ORGANIZATION	ACCESS TIME	CONSUMPTION	TEMPERATURE RANGE	Nb PINS
ET 2716Q	2 K x 8	450 ns	525/132 mW	C, V, M	24
ET 2716Q-1	2 K x 8	350 ns	525/132 mW	C, V	24

CMOS EPROMs

PART Nber	ORGANIZATION	ACCESS TIME	CONSUMPTION	TEMPERATURE RANGE	Nb PINS
ETC 2716Q-5	2 K x 8	550 ns	25/0.5 mW	C, E, V, M	24
ETC 2716Q	2 K x 8	450 ns	25/0.5 mW	C, E, V	24
ETC 2716Q-1	2 K x 8	350 ns	25/0.5 mW	C	24
ETC 2732Q-55	4 K x 8	550 ns	25/0.5 mW	C, V, M	28
ETC 2732Q-45	4 K x 8	450 ns	25/0.5 mW	C, E, V	28
ETC 2732Q-35	4 K x 8	350 ns	25/0.5 mW	C, E, V	28
TS 27C64-30.Q	8 K x 8	300 ns	50/2.5 mW	C, V, M	28
TS 27C64-25.Q	8 K x 8	250 ns	50/2.5 mW	C, V, M	28
TS 27C64-20.Q	8 K x 8	200 ns	50/2.5 mW	C, V	28
TS 27C64-15.Q	8 K x 8	150 ns	50/2.5 mW	C, V	28
TS 27C256-45.Q*	32 K x 8	450 ns	100/2.5 mW	C, V, M	28
TS 27C256-30.Q*	32 K x 8	300 ns	100/2.5 mW	C, V, M	28
TS 27C256-25.Q*	32 K x 8	250 ns	100/2.5 mW	C, V, M	28
TS 27C256-20.Q*	32 K x 8	200 ns	100/2.5 mW	C, V	28
TS 27C256-15.Q*	32 K x 8	150 ns	100/2.5 mW	C, V	28

ONE-TIME PROGRAMMABLE EPROMs

PART Nber	ORGANIZATION	ACCESS TIME	CONSUMPTION	TEMPERATURE RANGE	Nb PINS
TS27C64-25CP	8K x 8	250 ns	50/2.5 mW	C	28
TS27C256-25CP	32K x 8	250 ns	100/2.5 mW	C	28

ONE TIME PROGRAMMABLE OTP ROMs

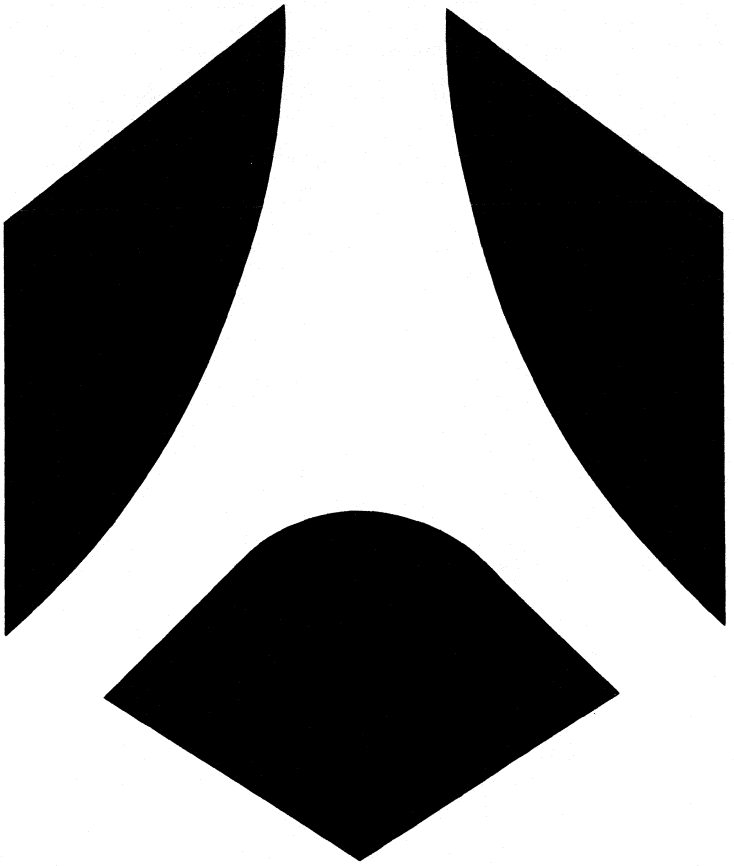
PART Nber	ORGANIZATION	ACCESS TIME	CONSUMPTION	TEMPERATURE RANGE	Nb PINS
TS 2764-45CP*	8 K x 8	450 ns	525/158 mW	C	28
TS 2764-30CP*	8 K x 8	300 ns	525/158 mW	C	28
TS 2764-25CP*	8 K x 8	250 ns	525/158 mW	C	28

* to be introducted

BIPOLAR PROMs

PART Nber	TECHNOLOGY	ORGANIZATION	OUTPUT	ACCESS TIME (t_{ACC} max)	SUPPLY	Nb PINS
TS 71180A*	H BIP II	1 K x 8	Op. Col.	45 ns	+5 V	24
TS 71181A*	H BIP II	1 K x 8	3-state	45 ns	+5 V	24
TS 71180B*	H BIP II	1 K x 8	Op. Col.	35 ns	+5 V	24
TS 71181B*	H BIP II	1 K x 8	3-state	35 ns	+5 V	24
TS 71180C*	H BIP II	1 K x 8	Op. Col.	25 ns	+5 V	24
TS 71181C*	H BIP II	1 K x 8	3-state	25 ns	+5 V	24
TS 71280A*	H BIP II	1 K x 8	Op. Col.	45 ns	+5 V	24 (Slim line)
TS 71281A*	H BIP II	1 K x 8	3-state	45 ns	+5 V	24 (Slim line)
TS 71280B*	H BIP II	1 K x 8	Op. Col.	35 ns	+5 V	24 (Slim line)
TS 71281B*	H BIP II	1 K x 8	3-state	35 ns	+5 V	24 (Slim line)
TS 71280C*	H BIP II	1 K x 8	Op. Col.	25 ns	+5 V	24 (Slim line)
TS 71281C*	H BIP II	1 K x 8	3-state	25 ns	+5 V	24 (Slim line)
TS 71190A	Advanced TTL	2 K x 8	Op. Col.	60 ns	+5 V	24
TS 71191A	Advanced TTL	2 K x 8	3-state	60 ns	+5 V	24
TS 71190B	Advanced TTL	2 K x 8	Op. Col.	45 ns	+5 V	24
TS 71191B	Advanced TTL	2 K x 8	3-state	45 ns	+5 V	24
TS 71190C	Advanced TTL	2 K x 8	Op. Col.	35 ns	+5 V	24
TS 71191C	Advanced TTL	2 K x 8	3-state	35 ns	+5 V	24
TS 71290C	H BIP II	2 K x 8	Op. Col.	35 ns	+5 V	24 (Slim line)
TS 71291C	H BIP II	2 K x 8	3-state	35 ns	+5 V	24 (Slim line)
TS 71321B*	H BIP II	4 K x 8	3-state	55 ns	+5 V	24
TS 71321C*	H BIP II	4 K x 8	3-state	45 ns	+5 V	24
TS 71641*	H BIP II	8 K x 8	3-state	55 ns	+5 V	24

* to be introducted



Surface mounted devices

THOMSON SEMICONDUCTEURS is a combination of strategies, technologies, technical services and production means providing answers to the multiple challenges facing to day's electronics industry.
The Bipolar Integrated Circuits, MOS and Discrete divisions of THOMSON SEMICONDUCTEURS are devoted to the development and production of advanced technology components, answering the growing needs of Surface Mounted Devices.
Through these divisions, THOMSON SEMICONDUCTEURS has developed a complete range of Surface Mount packages.
These packages have been entirely designed by THOMSON SEMICONDUCTEURS research and development centers of the various divisions, and are mass producted through fully automated state-of-the-art assembly equipments.

SURFACE MOUNTED DEVICES: today's solution for state-of-the-art system designs.
Today's trend toward light weight system designs with high component density allows Surface Mounting Technology to revolutionize manufacturing in the Electronics industry.
Reduction in board assembly cost by as much as 40% and in board size by as much as 50% is a goal that can be reached through the utilization of Surface Mounted Devices: Active Semiconductors (SO IC's, SOT, MELF, MINIMELF, "SM" and Chip Carrier) as well as passive components.
Today system designers can select package outlines that meet state-of-the-art weight/space ratio requirements while enhancing electrical performance.
By 1990, through widely accepted data, one can foresee about 50% of the world wide demand to be Surface Mounted Devices.

Compared to conventional packages, Surface Mount packages propose the following features.

- Compact design enabling high packing density and significant reduction in board size and weight, for instance in consumer electronics, telecommunications and automotives.
- Easy and low cost handling through automated high speed pick and place machinery.
- Available in tape and reels for easy automation and high volume assembly.
- Density and performance in circuit complexity.
- Mounting capability on both sides of all types of substrats (Ceramic of PC boards) using all current methods, such as wave soldering or reflow (IR or vapor-phase) technics.
- Same electrical characteristics (same dice) as conventional packages, with improved high frequency, high speed switching performances due to lower lead inductance and capacitance.
- Optimized way to package VLSI circuits by utilizing plastic chip carrier along with SO packages, leading to a major advantage over chip and wire assembly processes.

TELEPHONE SET ICs

Part number	Function	Package	Page
TEA3046FP	Telephone set transmission and DTMF generation circuit	SO28	2-5
TEA7037FP	Telephone set transmission and DTMF generation circuit	SO28	2-39
TEA7047FP	Telephone set transmission and DTMF generation circuit (european standard)	SO28	2-19
TEA7050FP	Telephone set transmission	SO24	2-63
TEA7031FP	Monitor amplifier/ringer	SO28	3-5
TEA7531FP	Monitor amplifier	SO16	3-23
TEA7540FP	Handsfree	SO24	3-35

8-BIT MICROCOMPUTERS

Reference	Characteristic		Function
EF 6804P 2	High on-chip feature integration well suited for additional 4-bit application extensions. • RAM: 32 bytes • ROM: 1 K byte • 20 bidirectional I/O lines (8 LED compatible)	• Self check mode • 8-bit timer with 7-bit software programmable prescaler • Emulation and development on DEVICE®	LOW COST MCU
EF 68HC04P3	• RAM: 124 bytes • ROM: 2 K bytes	Dedicated to power and data saving applications or requiring protection against mains failures. • Pin to pin and software compatible with EF 6804P2 • 20 bidirectional I/O lines • Self check mode • 8-bit timer with 7-bits software programmable prescaler • Emulation and development on DEVICE®	LOW POWER MCUs
EF 6805P2	• RAM: 64 bytes • ROM: 1 K byte • 20 I/O lines (8 LED compatible)	General purpose MCUs covering a wide range of applications such as electronic ignition, key board encoding, home appliantes, electronic games,... • Self check mode • 8-bit timer with 7-bit programmable prescaler • Emulation and development on DEVICE®	PROCESS CONTROL MCUs
EF 6805P6	• RAM: 64 bytes • ROM: 1796 bytes • 20 I/O lines (8 LED compatible)		
EF 6805U2	• RAM3 64 bytes • ROM: 2 K bytes • 32 I/O lines: -24 bidirectional (8 LED compatible) -8 input only		
EF 6805U3	• RAM: 112 bytes • ROM: 3776 bytes • 32 I/O lines: -24 bidirectional (8 LED compatible) -8 input only		
EF 6805R2	• RAM: 64 bytes • ROM: 2 K bytes • Mask programmable prescaler	Dedicated MCUs for industrial process control and applications where low cost analog signal computing is required such as automotive motor control • 32 I/O lines: -24 bidirectional (8 LED compatible) -8 in put only • Self check mode • 8-bit timer with 7-bit programmable prescaler • A/D converter with 8-bit conversion and 4 multiplexed anelog inputs • Emulation and development on DEVICE®	A/D CONVERSION MCUs
EF 6805R3	• RAM: 112 K bytes • ROM: 3776 bytes • Software programmable prescaler		
EF 6801	• RAM: 128 bytes (64 standby) • ROM: 2 K bytes	Dedicated MCUs for applications where high computing facilities are required such as persona/ home computers, injection/ trip computers, date transmission computers. • 8 × 8 multiply instruction • 29 I/O lines and 2 control lines • 16-bit programmable timer • Single-chip or expansed operation up to 64 K byte addressing space • Serial Communication interface (SCI) • Emulation and development on DEVICE®	HIGH PERFORM-ANCE MCUs
EF 6803	• RAM: 128 bytes (64 standby)		
EF 6801U4	• RAM: 192 bytes (32 standby) • ROM: 4 K bytes		
EF 6803U4	• RAM: 192 bytes (32 standby)		

BIPOLAR OPERATIONAL AMPLIFIER

Characteristics	Symbol	Unit	Single						Dual					Quad				
Power supply voltage	V_{CC}max.	V	±20	±18	±18	±20	±18	±18	±16 or 32	±18	±18	±13 or 26	±18	±16 or32	±18	±13 or26	±18	±18
Input offset voltage	V_{IO} max.	mV	0.8	7.5	7.5	10	6	6	7	3.5	6	±7	6	7	6	7	10	6
Input offset current	I_{IO} max.	nA	20	50	1	200	200	25	±50	50	200	±50	200	50	50	50	50	100
Input impedance	Z_I min.	MΩ	200 typ	0.5	10	0.5	0.3	5 typ	—	0.5 typ	0.2	—	0.3	8	0.8	8	0.3	1 typ
Bias current	I_B max.	nA	150	250	7	500	500	50	250	300	500	250	500	250	200	250	500	250
Output slew rate	S_{VO}	V/μS	—	—	—	50 min	0.5 typ	0.8 typ	—	1 typ	0.8 typ	—	1 min	—	—	—	—	0.4 typ
Supply voltage rejection ratio	S_{VR} min.	dB	96	70	80	65	76	74	65	86	76	50	76	65	77	—	76	74
Bandwidth	B	MHz	—	—	—	15 typ	—	—	—	1.5 min	—	—	2 min.	—	1 typ	—	1 typ	0.5 min
Short-circuit current	I_{SC}	mA	—	—	—	—	25 typ	12 typ	60 max	23 typ	—	—	40 max	60 max	25 typ	60 max	45 max	30 max
Voltage gain	$A_V$min	V/mV	100	25	25	25	20	50	25	20	20	—	20	25	25	—	20	50
Continuous input voltage	(Vmax) min.	V	—	±12	±14	±11.5	±12	±10	0 to V+1.5	±10	±12	0 to V+2	±12	0 to V+1.5	±12	0 to V+2	+13 to V	+13
			LM 111CFP	LM 301AFP	LM 308FP	LM 318FP	UA 741CFP	UA 776CFP	LM 358FP	TEB 1033FP	LM 1458FP	LM 2904FP	MC 4558CFP	LM 324FP	LM 348FP	LM 2902FP	MC 3403FP	LM 346FP
SO 8			●	●	●	●	●	●	●	●	●	●	●					
SO 14														●	●	●	●	
SO 16																		●

J - FET OPERATIONAL AMPLIFIERS

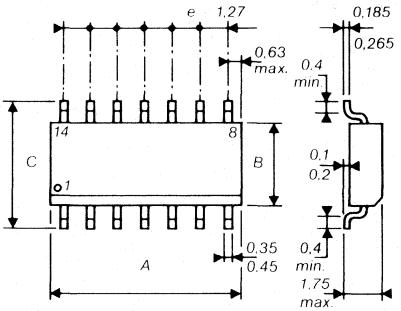
Characteristics	Symbol	Unit	Single				Dual				Quad		
Power supply voltage	V_{CC} max	V	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18
Input offset voltage	V_{IO} max	mV	15	10	15	10	15	10	15	10	15	10	15
Input offset current	I_{IO} max.	0.2	0.05	0.2	0.1	0.2	0.05	0.2	0.1	0.2	0.05	0.2	
Input impedance	Z_I min	10^6 MΩ	1 typ	1 typ	1 typ	1 typ	1 typ	1 typ	1 typ	1 typ	1 typ	1 typ	1 typ
Bias current	I_B max	nA	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4
Output slew rate	S_{VO}	V/μs	3.5 typ	13 typ	13 typ	13 typ	13 typ	13 typ	13 typ	13 typ	13 typ	13 typ	13 typ
Supply voltage rejection ratio	S_{VR} min	dB	70	70	70	70	70	70	70	70	70	70	70
Bandwidth	B	MHz	1 typ	3 typ	3 typ	4 typ	1 typ	3 typ	3 typ	4 typ	1 typ	3 typ	3 typ
Voltage gain	A_V min	V/mV	3	25	25	25	3	25	25	25	3	25	25
Continuous voltage	(V_I max) min	V	± 10	± 10	± 10	± 11	± 10	± 10	± 10	± 11	± 10	± 10	± 10
			TL 061CFP	TL 071CFP	TL 081CFP	LF 351FP	TL 062CFP	TL 072CFP	TL 082CFP	LF 353FP	TL 064CFP	TL 074 CFP	TL 084CFP
SO 8			●	●	●	●	●	●	●	●			
SO 14											●	●	●

COMPARATORS

Characteristics	Symbol	Unit	LM 319FP	LM 339FP	LM 2901FP	LM 393FP	LM 311FP
Power supply voltage	V_{CC} max.	V	36	± 18 or 36	± 18 or 36	± 18 or 36	36
Input offset voltage	V_{IO} max.	mV	8	± 5	± 7	± 5	7.5
Input bias current	I_B max.	nA	1000	250	250	250	250
Input offset current	I_{IO} max.	nA	200	± 50	± 50	± 50	50
Voltage gain	A_V typ.	V/mV	40	200	100	200	200
Low level output voltage	V_{OL}	V	1.5	0.4	0.4	0.4	1.5
Response time	t_r typ.	µs	0.08	1.3	1.3	1.3	0.2
	SO8					●	●
	SO14		●	●	●		

VOLTAGE REGULATORS

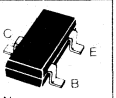
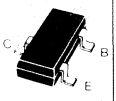
Characteristics	Symbol	Unit	UA 723CFP
Input voltage range	V_I	V	9.5 to 40
Output voltage range	V_O	V	2 to 37
Line regulation	K_{VI} max.	%/ V_O	0.1
Load regulation	K_{VO} max.	%/ V_O	
Long term stability	K_{VH}	$\frac{\%}{1000H}$	0.1
	SO14		●



Top view

	A mm	B mm	C mm
SO8	4.75/ 4.95	3.9/ 4.0	5.9/ 6.2
SO14	8.55/ 8.75	3.9/ 4.0	5.9/ 6.2
SO16	9.8/ 10.0	4.3/ 4.4	6.3/ 6.6
SO24	15.2/ 15.6	7.4/ 7.6	10.0/ 10.65
SO28	17.7/ 18.1	7.4/ 7.6	10.0/ 10.65

RADIO FREQUENCY TRANSISTORS

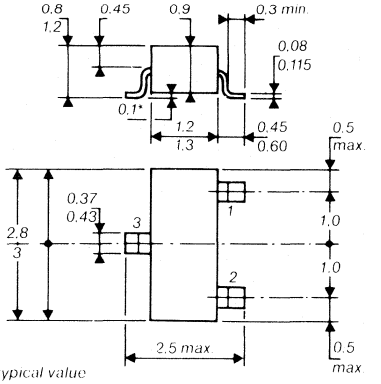
Types	Polarity	Maximum ratings		Characteristics at 25°C									Marking*	Pin out
		P_{tot}	V_{CEO}	f_T @ I_C min		C_{CB} @ V_{CB} C_{22b}* max		G_{PE} @ I_C - f G_{UM}* min			F @ I_C - f max			
		(mW)	(V)	(MHz)	(mA)	(pF)	(V)	(dB)	(mA)	(MHz)	(dB)	(mA)	(MHz)	
★SO 918 (1)	N	250	15	600	4	1,7*	10	15	6	200	6	1	60	N10	
★BFS 17 (R) (1)	N	250	15	1300	25	0,6 §	10	16 *§	10	500	2 §	2	500	E1 (E4)	N
★BFR 92A (R) (1)	N	250	15	5000§	14	0,35§	10	16 *§	14	800	1,8§	4	800	P2 (P5)	
★BFR 93A (R) (1)	N	250	12	5000§	30	0,6 §	5	14 *§	30	800	1,6§	4	800	R2 (R5)	
BFS 18 (R)	N	250	20	200§	1	0,85§	10				4 §	1	100	F1 (F4)	
★BFS 19 (R)	N	250	20	260§	1	0,85§	10				4 §	1	100	F2 (F5)	
★BFS 20 (R)	N	250	20	275§	5	0,35§	10							G1 (G4)	(R)

§ Typical value.

★ Preferred device.

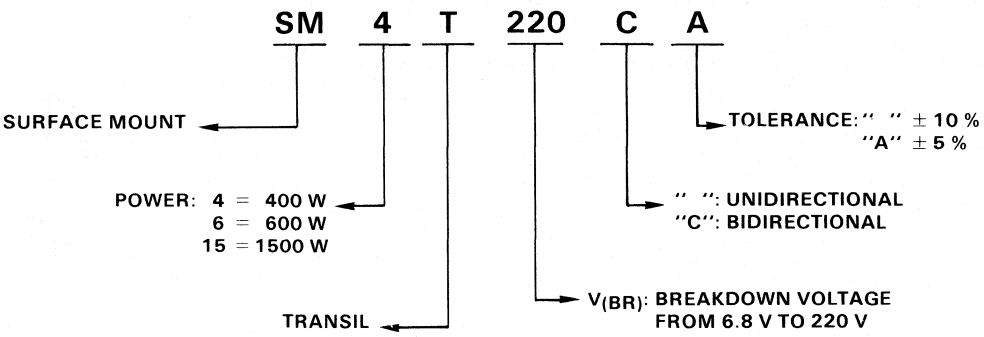
(1) Can be delivered according to CNET specification.

* Marking into brackets, refer to reverse pin configuration R.



* typical value

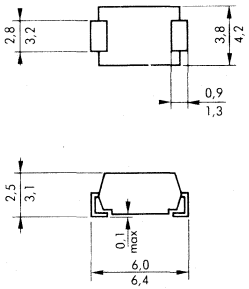
TRANSIL



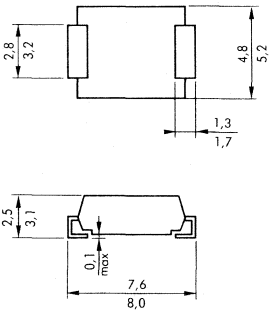
Ex: SM4T 220 CA = 400 W bidirectional transil with 220 V breakdown voltage and 5 % tolerance

Power \ Package	CB472	CB473
400 W	●	
600 W	●	
1500 W		●

CB472



CB473



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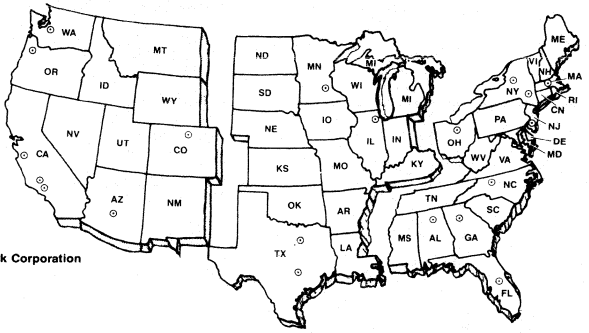

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FAX 215/362-1293

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Longmont, CO 80501
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